An experimental evaluation of SiC switches in soft-switching converters

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Abstract—Soft-switching converters equipped with insulated gate bipolar transistors (IGBTs) in silicon (Si) have to be dimensioned with respect to additional losses due to the dynamic conduction losses originating from the conductivity modulation lag. Replacing the IGBTs with emerging silicon carbide (SiC) transistors could reduce not only the dynamic conduction losses but also other loss components of the IGBTs. In the present paper, therefore, several types of SiC transistors are compared to a state-of-the art 1200 V Si IGBT. First, the conduction losses with sinusoidal current at a fixed amplitude (150 A) are investigated at different frequencies up to 200 kHz. It was found that the SiC transistors showed no signs of dynamic conduction losses in the studied frequency range. Second, the SiC transistors were compared to the Si IGBT in a realistic soft-switching converter test system. Using a calorimetric approach, it was found that all SiC transistors showed loss reductions of more than 50%. In some cases loss reductions of 65 % were achieved even if the chip area of the SiC transistor was only 11% of that of the Si IGBT. It was concluded that by increasing the chip area to a third of the Si IGBT, the SiC vertical trench junction field effect transistor could yield a loss reduction of approximately 90 %. The reverse conduction capability of the channel of unipolar devices is also identified to be an important property for loss reductions. A majority of the new SiC devices are challenging from a gate/base driver point-of-view. This aspect must also be taken into consideration when making new designs of soft-switching converters using new SiC transistors.

***Index Terms*— IGBT, resonant converters, soft switching, conductivity modulation, silicon carbide, MOSFET, JFET, BJT.**

I. Introduction

Technological changes resulting in material savings are key factors for reducing cost in most power electronics equipment. One of the most effective ways to achieve such material savings is to increase the switching frequency of the converter. With metal oxide-semiconductor field-effect transistors (MOSFETs), on the one hand, switching frequencies of several hundred kilohertz are possible with hard-switching converters [1]. In applications where the maximum voltage rating of high-performance MOSFETs is not sufficient, on the other hand, insulated gate bipolar transistors (IGBTs) are usually chosen, and the upper limit of the

switching frequency in this case is approximately 10-20 kHz for hard-switching converters. The reason to this limitation is that the switching losses increase with the switching frequency. In the continuous trend towards ever more compact converters various soft-switching [2]-[10] technologies have, therefore, been suggested, as these technologies, at least theoretically, can perform switching transitions without any significant losses. One of the most popular soft-switching converters is the series-loaded resonant (SLR) converter [11]-[13]. A circuit diagram of this converter is shown in Fig. 1. If this converter is operated above the resonant frequency using capacitive snubbers, soft-switching conditions should be possible to achieve at both turn-on and turn-off. However, regardless if frequency control [11], [12], [14], phase-shift control [15], or dual control [16] is used, it is never possible to eliminate the switching losses. This is partly due to the *tail current* [17]- [19]. Another important source of additional losses at high switching frequencies are the losses associated with the *conductivity modulation lag* [18], [20], [21]. These losses are simply a result of that a certain time is necessary for the device to be brought into deep saturation. At high switching frequencies this phenomenon cannot be disregarded as the time constant of the conductivity modulation lag approaches the same order of magnitude as the cycle time. In [22], therefore, an extensive experimental investigation involving several types of IGBTs was performed. Both tail-current and conductivity-modulation-lag effects were covered. From the results it was obvious that different types of IGBTs had very different performance with respect to the aforementioned dynamic phenomena. Additionally, it was found that even the best type of 1200 V IGBTs had significant dynamic losses at switching frequencies above 30 kHz.

Recently, another possibility to proceed has been enabled by the introduction of several types of power transistors in silicon carbide (SiC). Initially, the SiC MOSFET was believed to be the high-speed replacement for Si IGBTs. The problems with manufacturing and stability of the oxide layer were, however, probably underestimated. The first active switch to be available in series production was instead the normally-on junction field effect transistor (JFET). Due to the normally-on property [23], [24] of this device many engineers did not perceive this device as a reasonable replacement for a Si IGBT as the additional requirements on the gate drivers, the main circuit, and the overall control system were unreasonably high to fulfill for safe operation of the system. This spurred a great activity of development and since recent years both MOSFETs [25], bipolar junction transistors (BJTs) [26], and normally-off JFETs [27] have also been available in series-production. It has to be mentioned that the normally-on SiC JFET is not the only SiC device having a *driver problem* [23]. The BJT requires a continuous base current as long as it is in the on-state [26]. More surprising, however, is that the normally-off JFET has the same problem [27]. The reason to this is that the gate-source junction has to be forward biased in the same way as in a BJT, and with the existing designs this implies a significant continuous gate current during the on-state. As SiC devices have the potential to be operated at high temperatures, the temperature dependence is also an important aspect to be kept in mind. It is not surprising that

the on-state resistances of JFETs and MOSFETs have a positive temperature dependence. The temperature dependences of the forward-biased gate/base junctions of the normally-off JFET and the BJT are, however, not obvious. Additionally, since carrier injection occurs in both cases, dynamic effects cannot be disregarded without a proper investigation. Taking all the aforementioned aspects into consideration it seems fruitful to compare SiC MOSFETs, JFETs, and BJTs for use in a soft-switching application. At first sight, it may seem sufficient to investigate only the aforementioned dynamic effects of the new SiC devices. However, since these power semiconductors should operate in a series-loaded resonant converter, various other aspects must also be considered in order to find the best device solution for the actual application. Obviously, the conduction losses should be one of the dominating loss contributions when the switching losses have been reduced. The magnitude of the conduction losses and the temperature dependence of these losses must, therefore, also be compared. From a systems aspect, it is also important to consider the complexity and reliability of the gate/base drivers. These units represent, in a sense, one of the core technologies in a new converter design, and any anomalies or adverse phenomena related to the gate/base drivers may imply a failure from a systems perspective.

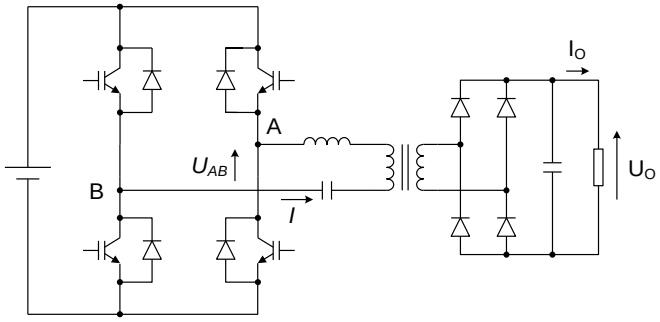


Fig. 1. Circuit diagram of a series-loaded resonant converter

This paper is organized as follows. In Section II the conduction losses with sinusoidal current excitation for different SiC devices are compared. For reference, an Si IGBT and an Si MOSFET are included. Moreover, Section II also presents experimental results on the temperature dependency of the on-state resistances for different types of SiC field-effect transistors. In Section III the performance of a 25 kHz, 60 kW series-loaded resonant converter test system is evaluated. The total losses using different SiC switches are measured and compared to the reference case with an Si IGBT. In Section IV the test results are discussed, and Section V provides a conclusion of the work performed.

II. CONDUCTION LOSSES

As already mentioned in the preceding section, the conductivity modulation lag of state-of-the-art 1200 V Si IGBTs has a significant impact on the conduction losses at switching frequencies above 30 kHz, [22]. Unipolar devices in SiC such as the MOSFET and normally-ON JFET should, at least theoretically, not exhibit this property because no carrier injection is involved in the conduction mechanism. However, it cannot be taken for granted that BJTs and normally-OFF JFETs in SiC are free from dynamic effects in the ON-state voltage drop, as these devices are not pure majority carrier devices (due to the forward-biased base-emitter and gate-source junctions). A comparison of the dynamic properties of the ON-state voltage drop of all 1200 V SiC devices described above will therefore be performed. A 1200 V Si IGBT and 1200 V Si MOSFET are used as reference cases. The test is performed such that the device under test (DUT) is conducting a half-period of a sinusoidal current. The waveform of the voltage drop across the DUT is then analysed with respect to dynamic effects.

A. Methodology

The dynamic properties of the on-state voltage are studied under a sinusoidal current excitation. The experiments are performed at different temperatures and frequencies. The results for different test objects are compared.

The test circuit shown in Fig. 2 is used. It consists of two half-bridges connected to a series-resonant tank. The switches T_1/D_1 and T_2/D_2 are used to initiate an oscillation in the resonant tank. The switch T_4/D_4 serves as the D.U.T. and is continuously in the on-state. The on-state voltage U_{CE} and the conducted current I_E of T_4/D_4 are recorded.

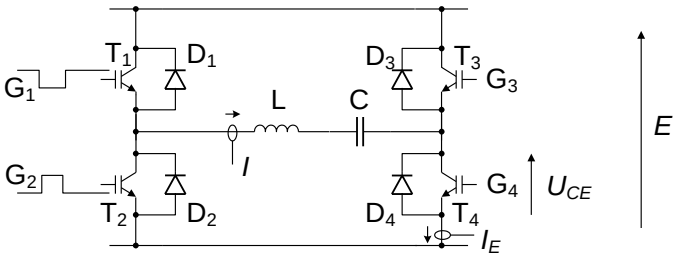


Fig. 2. Test circuit for investigation of the dynamic properties of the on-state voltage drops of SiC switches.

The switch T_3/D_3 is continuously in the off-state. The voltage, E, is used to control the amplitude of the current and the resonant tank (L and C) determines the frequency.

Figs. 3 and 4 show oscillograms from measurements in the test circuit. Fig. 3 shows the oscillation of the tank current. The duration of the current is in the range of 1 ms. In order not to, significantly, heat the chip the oscillations are repeated at a low

repetition frequency of 0,5 Hz. The junction temperature, T_j, is kept constant during the tests. T_j is controlled by controlling the temperature of the heat sink.

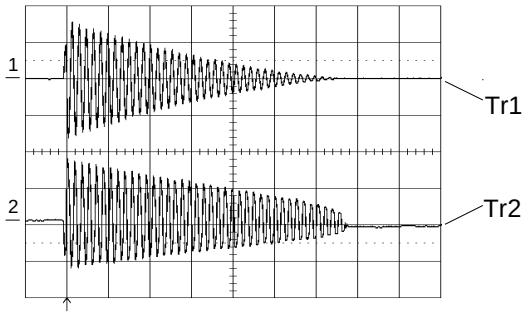


Fig. 3. Excitation of resonant tank, Tr1: I_E (100 A/div), Tr2: U_{CE} (2 V/div), time: 0,2 ms/div

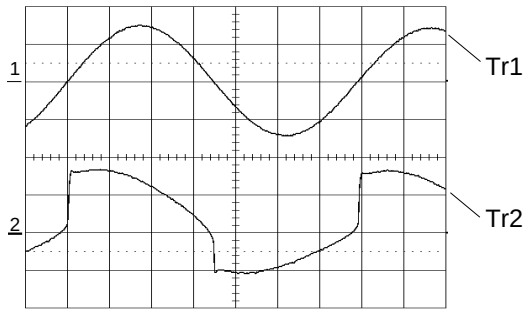


Fig. 4. Measurement of $u_{CE}(t)$ and $i_E(t)$, Tr1: $i_E(t)$ (100 A/div), Tr2: $u_{CE}(t)$ (2 V/div), time: 5 µs/div

Fig. 4 shows $i_E(t)$ and $u_{CE}(t)$ during one of the periods of the oscillation. The voltage $u_{CE}(t)$ is measured at the power terminals of the module. E is adjusted such that the peak value of I_E, $\hat{i}_E$, is 150 A. This value is kept constant for all measurements. In order to minimize the errors in the power loss calculation it is vital to keep the difference in delays between the recorded values of $i_E(t)$ and $u_{CE}(t)$ low. Since the on-state voltage is measured at the power terminals of the module it has to be compensated for the voltage drop of the stray inductances of the module in order to reflect the on-state voltage of the chip, [22]. If a conductivity modulation lag is present, the on-state voltage of the chip will differ when comparing the same current at rising and falling interval of the half cycle.

The proposed method benefits from the fact that the dynamic measurement range is adapted to the measured signal (D.U.T continuously in the on-state), in contrast to the case when the D.U.T is turned on and off, where the voltage range of the measurement is governed by the high voltage in the off-state. With the proposed method, therefore, a much higher accuracy can

be achieved. Additionally, the switching transients are avoided. Nevertheless, small inaccuracies originating from the voltage and current measurements, the compensation procedure, variations in temperature measurements, and additional potential adverse oscillation modes in the test circuits cannot be avoided. The inaccuracy has been estimated to be within +/- 5% of the measurement range.

B. Test devices

Table I lists the different devices used for the tests. Ref 1 and Ref 2 are Si components used as references for the SiC devices A, B, C, D, and E. The test devices are evaluated with respect to on-state voltage, dynamic conduction losses, and the actual chip area. For comparison reasons the total chip area of the switch is used. Ref 1(Si IGBT) is used as a relative reference for the chip area, Ref 1=100%.

The unipolar JFET and MOSFET can conduct current in the reverse direction (on-state), which is not possible with bipolar devices such as the BJT. In off-state, some of the devices offer an anti-parallel intrinsic body diode (Devices A and E) which may be useful in some applications.

Fig. 5 shows the typical outline and structure of a 1200 V Si IGBT power module in a half-bridge configuration. The actual power module in Fig. 5 is rated 1200 V. The module has the power terminals on the top and the heat is conducted from the bottom. The SiC test devices are all in the discrete power transistor package TO-247. The discrete components are mounted in a structure shown in Fig. 6, which has the same mechanical interface as the Si IGBT power module shown in Fig. 5. This arrangement enables a direct replacement in the test circuitry for accurate comparisons of the performance of the different devices.

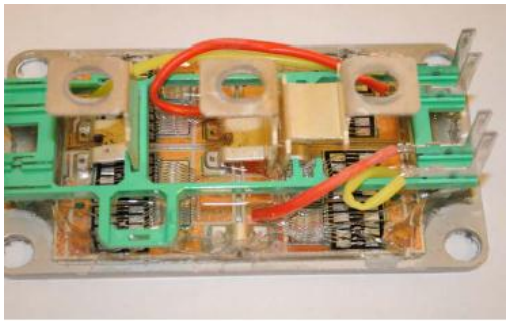
Table I

Test devices for conduction loss measurements

Device	Technology	Area (mm^2)	Area (%)	Type	Supplier
Ref 1	Si IGBT	512	100	SKM400GB125D	Semikron
Ref 2	Si MOSFET	371	72	IXFH12N100Q	IXYS
A	SiC MOSFET	101	20	CMF20120D	CREE
B	SiC Bipolar	110	21	BT1220AC	Transic /Fairchild
C	SiC JFET	54	11	SJEP120R063	SemiSouth

	(n-OFF) VTJFET				
D	SiC JFET (n-ON) DGJFET	61	12	-	Denso
E	SiC JFET (n-ON) LCJFET	82	16	IJY120R07	Infineon

(a)



(b)

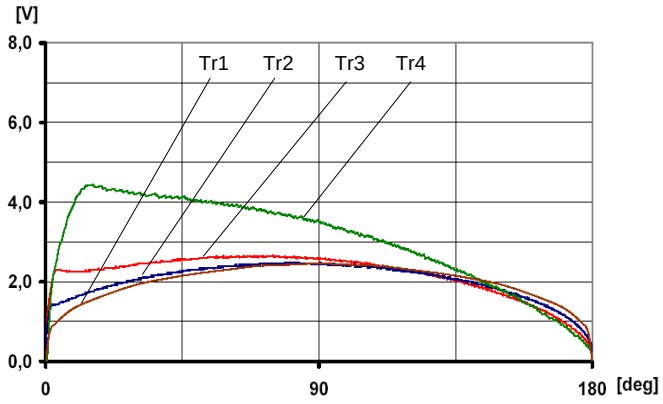
Fig. 5. IGBT module; (a) housing, (b) internal structure

Fig. 6. Test device, mechanical layout

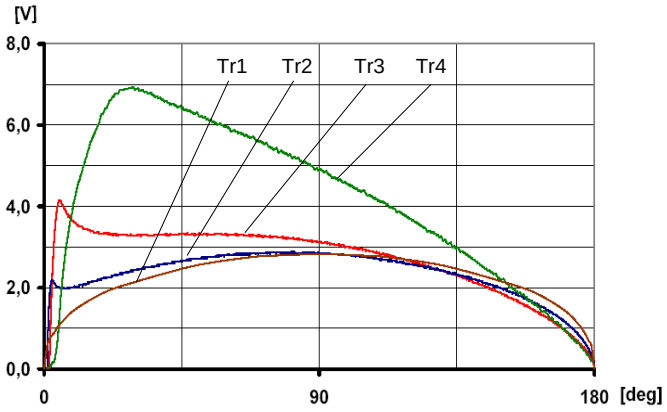
C. Experimental results

The on-state voltage is measured using the method described in the previous section. Fig. 7 shows the results for a Si IGBT (Ref 1) at different frequencies and temperatures. The results are normalized to the period time in order to compare the impact of the rate of change of the current. Fig. 7 (a) and Fig. 7 (b) depict the results at two different junction temperatures (T_J), 25°C and 125°C respectively. Comparing the results from different frequencies shows clearly the presence of the dynamic effects impacting the on-state voltage at higher frequencies, i.e. on-state voltage shows a higher value for a rising current when compared to a falling current of the same value. It is also observed that this effect is more severe at higher temperatures. The cause of this effect is the lag of the conductivity modulation which is present in bipolar Si power devices. A thorough investigation of dynamic effects in Si IGBTs is presented in [22]. The conductivity modulation lag is a limiting factor for highly efficient high-frequency operation of soft-switching converters.

Fig. 8 shows the results of an Si MOSFET (Ref 2). Due to the unipolar design the dynamic effects have no significance at the measured frequency (33 kHz). However, because of the resistivity of the drift region the magnitude of R_{DSon} is high (≈10 times IGBT), which is typical for high-voltage Si MOSFETs (1200 V).

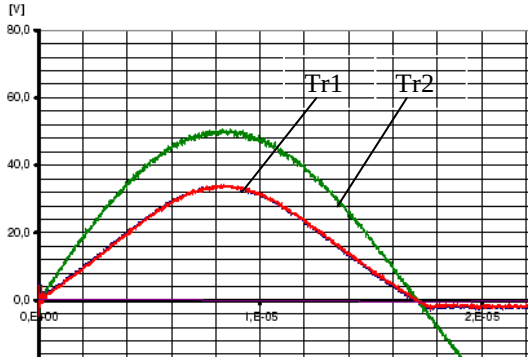


(a)

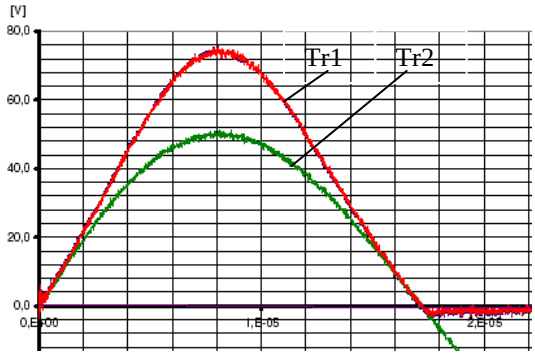


(b)

Fig. 7. Test results Si IGBT (Ref 1), $U_{CE,}$ Tr1: DC eqv, Tr2: 7,5 kHz, Tr3: 30 kHz, Tr4: 104 kHz, (a): T_j 25 ºC, (b): T_j 125 ºC



(a)



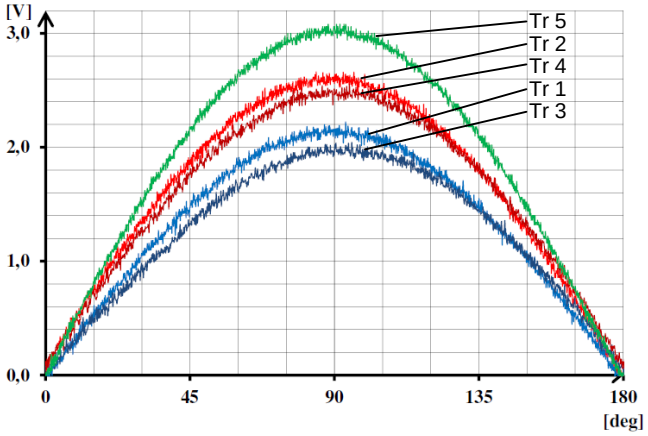
(b)

Fig. 8. Test results; Si MOSFET (Ref 2): U_{CE} (Tr1), I_E (Tr2, 3 A/V), 33 kHz; a; T_J 25 ºC, b; T_J 125 ºC,

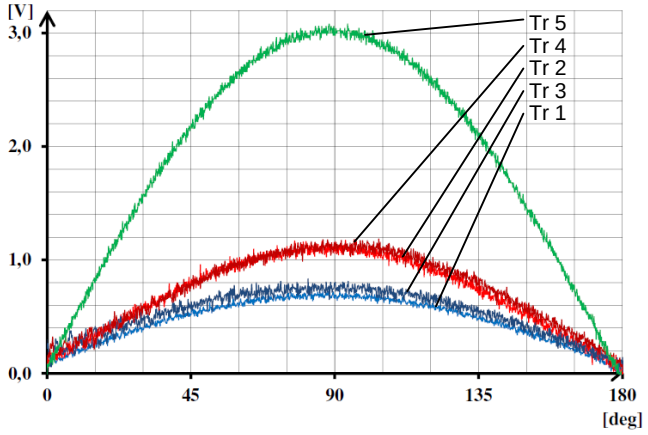
Fig. 9 shows the test results for the different SiC devices as described in Table I. From the measured results it is clear that no dynamic on-state effects can be observed for the SiC devices (Device A-E). This follows from the fact that the on-state voltage depends linearly on the conducted current, i.e. the on-state voltage has the same waveform as the current. These results were not supringsing for the unipolar devices (Device A, C-E). However, it is noticable that also for the bipolar device (Device B) there is no sign of any dynamic on-state effects in the applied frequency range (200 kHz). From an application point-of-view this means

that all the tested SiC power devices (including the BJT) can be used without significant additional conduction losses up to 200 kHz.

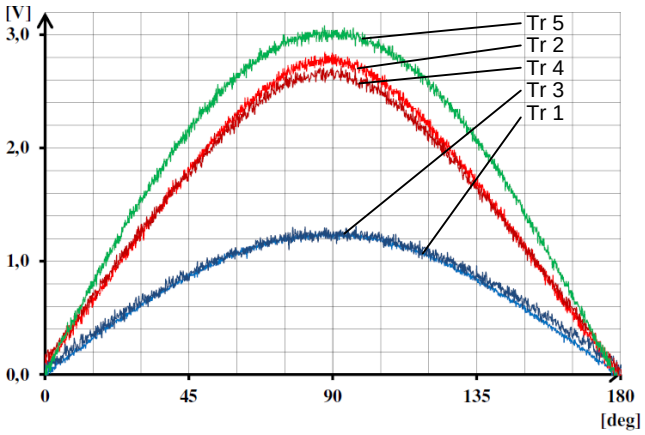
In some cases the two waveforms, for same temperature but different frequency, have a sligthly different magnitude. This difference is, however, within the estimated inaccuracy as described in Section II A.



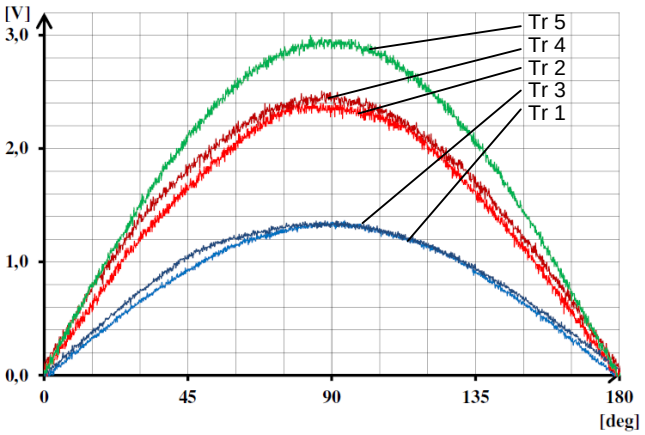
(Device A)



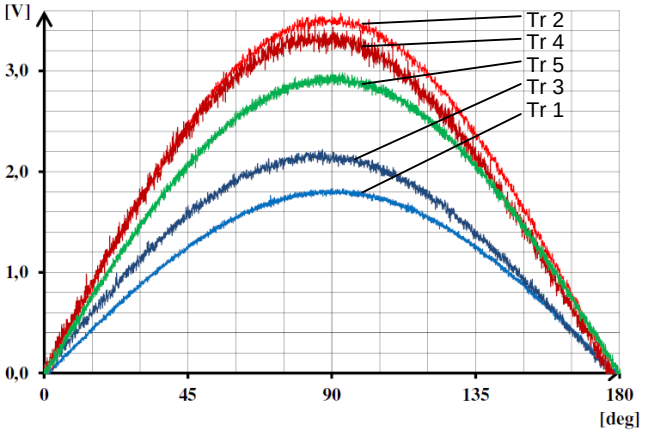
(Device B)



(Device C)



(Device D)



(Device E)

Fig. 9. U_{DS} at sinusoidal current excitation, î = 150 A, f = 30 resp. 200 kHz, T_J = 25 ºC resp. 125 ºC.

U_{DS} Tr 1;30 kHz, 25 ºC; Tr 2; 30 kHz. 125 ºC; Tr 3; 200 kHz. 25 ºC; Tr 4; 200 kHz. 125 ºC; Tr 5; I_D (50 A/V)

Table II lists the experimental results where J_{REL} is the peak current density (at 150 A) with the given total chip area from Table I, R_{DSon} (Actual) is calculated for the two different junction temperatures from the peak value of the current and the corresponding on-state voltage, R_{DSon} (Specific) is the on resistance normalized to the total chip-area, and *K* is a figure of merit, $K = \frac{R_{DSon}(125°C)}{R_{DSon}(25°C)}$, which is used to evaluate the temperature dependency of the on-state resistance. R_{DSon} (Actual) is calculated from the average value of the peak on-state voltage for the two excitation frequencies 30 kHz and 200 kHz.

Table II

Test results from conduction loss measurements

Device	Technology	J_{REL}	R_{DSon}, T_J=25 ºC		R_{DSon}, T_J=125 ºC		*K*
		(A/cm^2)	Actual (mΩ)	Specific (mΩ·cm^2)	Actual (mΩ)	Specific (mΩ·cm^2)	(%)
A	MOSFET	149	13,4	13,5	16,9	17,1	126
B	Bipolar	136	4,7	5,1	7,3	8,1	155
C	JFET (n-OFF) VJFET	278	8,0	4,3	18,0	9,7	225
D	JFET (n-ON) DGJFET	246	8,7	5,3	16,0	9,8	184
E	JFET (n-ON) LCFET	183	13,0	10,7	22,7	18.6	175

From Table II it is found that Device C has the lowest specific R_{DSon} at T_J=25 ºC (4,3 mΩ·cm$^{2.}$). Devices B and D have slightly higher values with 5,1 mΩ·cm^2 and 5,3 mΩ·cm^2, respectively. At T_J=125 ºC Device B has the lowest value of specific R_{DSon} (8,1 mΩ·cm$^{2.}$). Devices C and D have slightly higher values with 9,7 mΩ·cm^2 and 9,8 mΩ·cm^2, respectively.

Device A has the lowest relative increase of R_{DSon} from 25 ºC to 125 ºC (*K*=126%) while Device C has the value *K*=225%.

D. Temperature dependency of R_{DSon} for normally-on and normally-off VJFETs

The VJFET is available in two different versions, normally-off (Device C) and normally-on. In [28] these two are compared and the normally-on version is stated to have 15% lower R_{DSon} for the same chip area when compared to the normally-off, at T_J=25 ºC. Moreover, the temperature dependency is also lower for the normally-on design [28] indicating an even higher advantage at elevated operating temperatures. In [28] the temperature dependency for the normally-off VJFET is presented as a function of the gate-voltage. However, it is recommended to instead control the normally-off VJFET from the gate current. In order to be able to compare the potential of the normally-on and the normally-off VJFETs at higher values of T_J (up to 150 ºC), R_{DSon} as function T_J has been measured for these devices.

Due to the different operating principles of these transistors, two modified versions of the experimental setup were used as shown in Figs. 10(a) and (b) respectively. The vital part of the circuit is mainly the same for both cases. It consists of a direct voltage source V_{dc}, a dc-link capacitor, C, and an auxiliary switch, M (Si MOSFET). A control circuit is used to turn the auxiliary switch on and off. In Figs. 10(a) and (b), the stray inductance L_s and the resistance R of the cable connections are also included in the circuit diagram. Moreover, it must be noted that it is only the device under test (DUT) which is placed into the temperature chamber. The rest of the experimental setup is placed outside the chamber, in order to minimize the effect of the parasitic components on the measurements. When the auxiliary MOSFET is turned on, the current is flowing through the DUT causing a certain voltage drop across it. Since there is no external resistance connected in the circuit, the current of the DUT can be adjusted by properly selecting the value of V_{dc}. The drain-source voltage V_{DS} and the drain current I_{DS} of the DUT have been measured at elevated temperatures using a non-isolated voltage probe and an isolated current probe, respectively. Thus, the on-state resistance can easily be calculated using ohm's law.

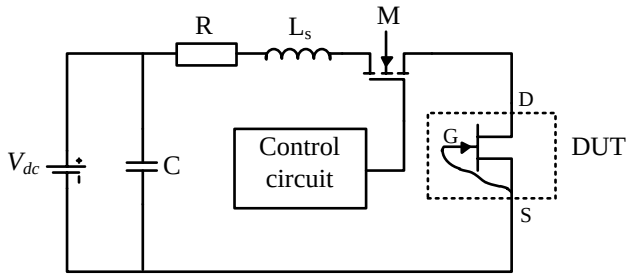
The duration when the auxiliary MOSFET is in the on-state must be chosen with care in order to avoid any self-heating phenomena of the DUTs on the one hand, and on the other hand to reach a certain time period where any possible resonances of V_{DS} and I_{DS} have decayed. A graphical illustration of the expected performance of these two quantities is shown in Fig. 11. The on-state resistances of the DUTs have been measured considering the average values of U_{DS} and I_{DS} from t_1 to t_2 where U_{DS} and I_{DS} have reached their steady-state values.

In order to measure the temperature dependence of the on-state resistance of the normally-ON SiC JFET, the circuit schematic shown in Fig. 10 (a) has been used. The gate of the JFET is directly connected to the source pin of the component such that the DUT is continuously kept in the on-state. It is, therefore, the auxiliary MOSFET which turns on for approximately 10 µs and controls the current flow through the DUT. On the contrary, the normally-OFF SiC JFET requires a positive gate-source current in order to turn-on. Thus, a simple gate-driver was designed as shown in Fig. 10 (b). It consists of a gate-resistor R_g and it is

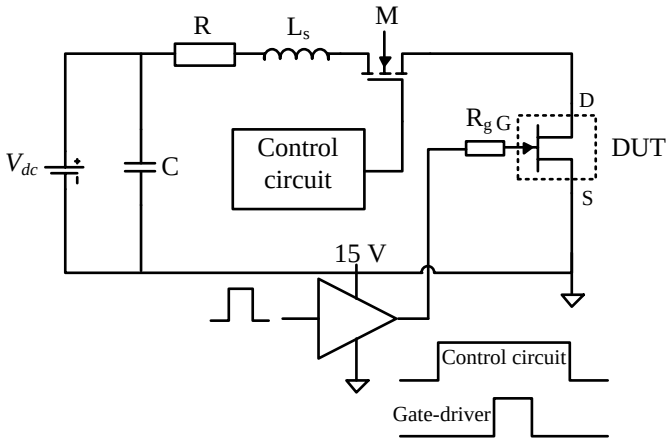
supplied from a 15 V voltage source. A special control sequence was utilized for the case of normally-OFF JFET as shown Fig. 10 (b). While the auxiliary MOSFET is turned-on for approximately 100 µs, the DUT is only turned on for approximately 10 µs.

Fig. 11 shows typical waveforms of the measurement, U_{DS} and I_{DS}. The initial oscillations originate from the step-response of the voltage source, U_{DC}, due to the fast rise of its load current. The data is recorded during the measurement interval, t_1- t_2. This interval is selected such that the influence of the initial oscillations can be neglected.

The measurements were performed at elevated temperatures starting from room temperature (25°C) up to 150 °C. Before recording the voltage and current data, it was secured that the temperature of the DUT had settled at the desired value. This was done by using a PT-100 temperature sensor attached to the heatsink of the DUT.



(a)



(b)

Fig. 10. Circuit schematics of the experimental setup for (a) normally-on VJFET and (b) normally-off VJFET.

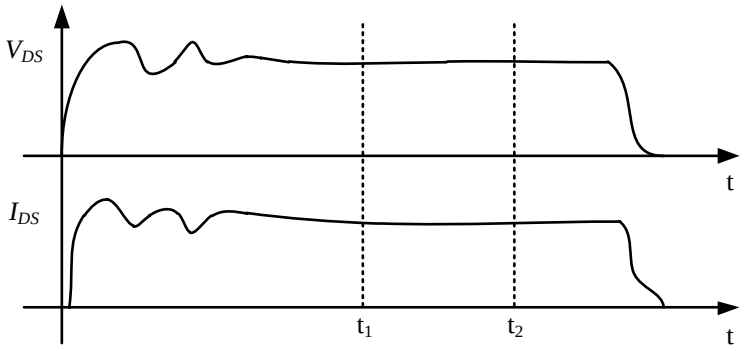


Fig. 11. Typical waveforms; U_{DS} and I_{DS} and measurement interval; t_1, t_2.

The results of the measurements are shown in Fig. 11. The measured values of R_{DSon} are normalized to the value at 25 °C and plotted versus the actual temperature. It is found that the normally-off VJFET has a stronger temperature dependency compared to the normally-on VJFET. It is also noted that the temperature dependence of the on-state resistance of the normally-on device is in agreement with temperature dependency of the electron mobility of the drift region as given in [29], i.e.

$$\frac{R_{DSon}(T_1)}{R_{DSon}(T_0)} = \left(\frac{T_1}{T_0}\right)^{2,15}, \tag{1}$$

where T_0 and T_1 are arbitrary temperatures in kelvin. This indicates that the resistance of the drift region is the dominating contribution to the on-state resistance in the normally-on VJFET. The *K*-values determined from measurements for the normally-on and the normally-off VJFETs are presented in Table III.

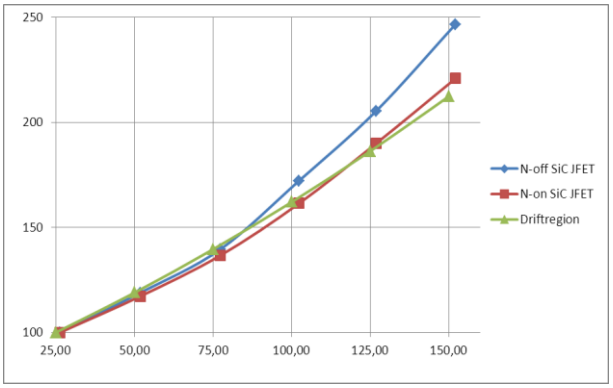


Fig. 12. R'$_{DSon}$ vs Tj for SJEP120R63 (normally-off) and SJDP120R085 (normally-on).

Table III

Temperature dependency VJFET

Device	K (%)
SJEP120R63 Normally-off	203
SJDP120R085 Normally-on	187

E. Discussion on trends and recently released components.

The testing of conduction losses of SiC switches as presented in this paper has been ongoing since several years. The first test, with Device A, was performed 2010 while the most recent ones (Devices D and E) date from 2012. The occasion for the different tests has been determined by the availability of test samples. In the context of a rapid development of the different technologies, this enables a risk to make wrong conclusions from the test results since older components are compared to more recently designed devices. In order to mitigate this risk and better understand the present position of the actual technologies, recently released components are compared based on supplier data. It is considered fair to use supplier data since the experimental results presented in Section II are in good agreement with the data given from the different suppliers. The components used for the comparison are listed in Table IV. The chip area and R_{DSon} at 25 °C are given from the suppliers. In the case of the MOSFET and BJT the *K*-value is extracted from the data sheets. In the case of the VJFET the experimental results as shown in Table III are used. The chip area of the normally-on VJFET is calculated based on [28]. From the value of R_{DSon} and the chip area the specific on-state resistance is calculated, and by using the *K*-value and the R_{DSon} at 25 °C the corresponding values for T_J=125 °C are calculated.

Table IV

Specific R_{DSon}, rated and estimated

Device	Chip area	*K*	R_{DSon}, 25 ºC		R_{DSon}, 125 ºC	
	(mm^2)	(%)	(mΩ)	(mΩ·cm^2)	(mΩ)	(mΩ·cm^2)
MOSFET CREE 25 mΩ	26	140	25	*6,5*	*35*	*9,1*
VJFET Semisouth 25 mΩ Normally-off	15	203	25	*3,8*	*51*	*7,6*

VJFET Semisouth 22 mΩ Normally-on	15	187	22	*3,3*	*41*	*6,1*
BJT Transic 17 mΩ	20	136	17	*3,4*	*23*	*4,6*

From Table IV it is found that at 25 °C the lowest specific on-state resistances are those of the BJT and the normally-on VJFET. At 125 °C the low *K*-value of the BJT results in the lowest value of the specific on-state resistance. Compared to the MOSFET, it is only ½ of the value. However, the MOSFET offers reverse conduction capability and an intrinsic body diode which may be beneficial in many applications. The normally-on VJFET is a very interesting alternative, offering a specific on-resistance similar to the BJT and reverse conduction capability. Neither the BJT, nor the normally-on VJFET include an intrinsic body diode.

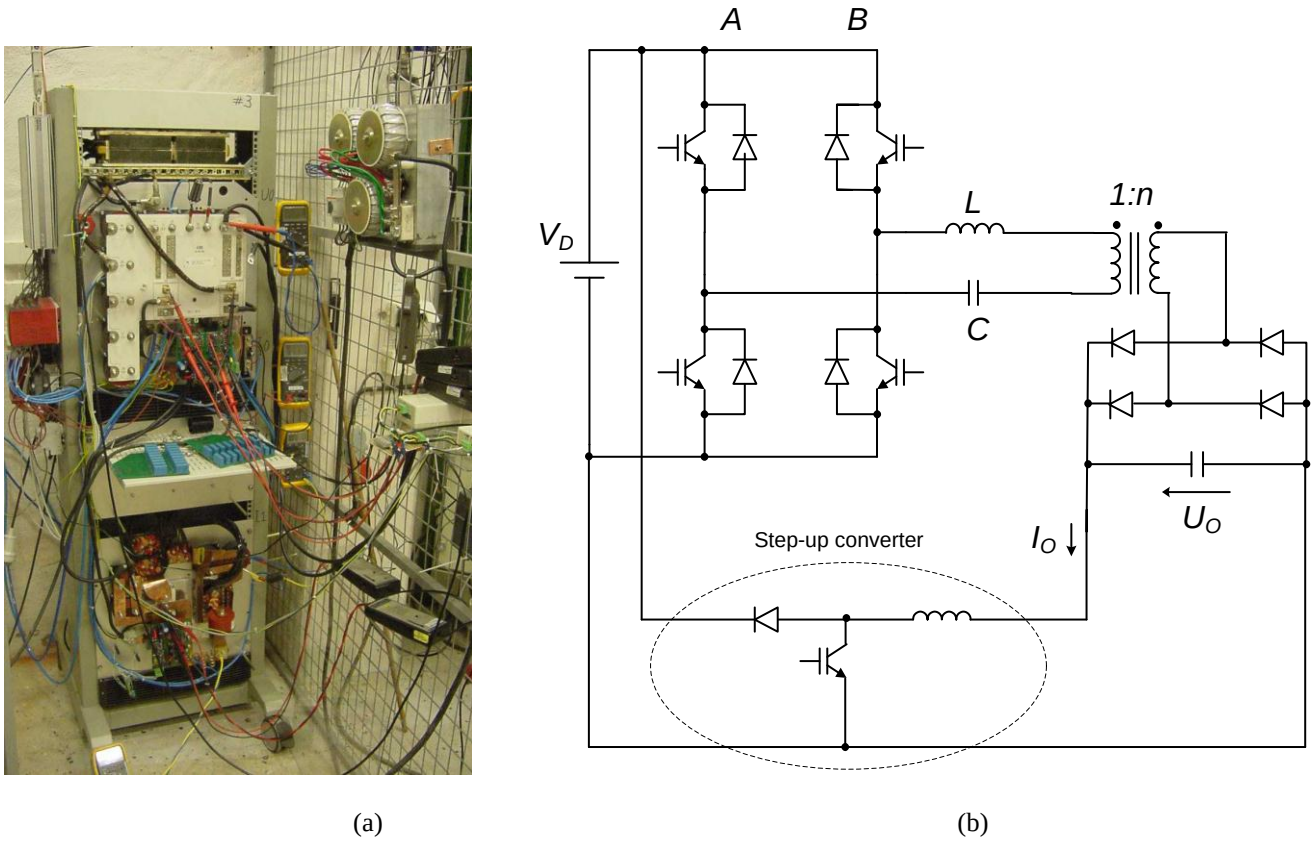
III. System Performance

Different SiC power switches have been experimentally evaluated in order to compare their efficiency in a soft-switching converter. The evaluation is performed by measuring the semiconductor losses in an SLR converter operated above the resonant frequency. In previous publications a similar method is used in order to compare the performance of Si IGBTs [22] and different control strategies [16].

A. Methodology

The test system consist of a main converter (SLR), a regenerative-load converter (step-up) and a cooling system for the power semiconductors. The main converter includes the power switches configured in an H-bridge. The test system is shown in Fig. 13. Fig. 13(a) is a photograph of the implementation and Fig. 13(b) is a circuit diagram of the test system. The main converter is controlled by means of varying the switching frequency of the power switches in the H-bridge. The two bridge legs A and B, as shown Fig.13 (b), are switched simultaneously, i.e. the upper switch in bridge leg A is made to turn-on at the same occasion as the lower switch in bridge leg B and the lower switch in bridge leg A is made to turn-on at the same occasion as the upper switch in bridge leg B. This control strategy ensures that the bridge legs A and B are operating under the same conditions. During the test, bridge leg A is using an Si IGBT for reference measurements and bridge leg B is using the SiC power switches to be evaluated. The output current, I_O, of the main converter is controlled by adjusting the switching frequency, while the output voltage, U_O, is controlled by the duty ratio of the step-up converter and the supply voltage, V_D. In order to find the maximum

losses in any point of operation the losses are measured at the maximum output current at different output voltages ranging from zero to the maximum value. The power loss is measured by means of a calorimetric method utilizing the cooling system.



(a) (b)

Fig. 13. Test system: (a) Implementation, (b) Schematic diagram

1) Test circuit

In order to obtain soft-switching of the power switches both bridge legs are equipped with capacitive snubbers [30], i.e. a snubber capacitor, C_S, is connected in parallel to each of the switches. The use of capacitive snubbers enables zero-voltage switching (ZVS) both at turn-on and turn-off in the selected mode of operation where the switching frequency, f_S, is higher than the natural frequency, f_0, of the resonant tank.

The parameter values for the SLR converter of the test system are listed in Table V. The actual parameter values yield f_0=22 kHz and f_S is expected to be in the range of 25-30 kHz. The lower frequency for high output voltages and the higher frequency for low output voltage (0 V). The parameter values for the test circuit correspond to an industrial power supply rated at 60 kW when supplied from a 3*400 VAC network.

Table V

Parameter	Value

V_D	400 V
L	30 μH
C	1,75 μF
C_S	390 nF
d	0,9
n	1
I_O	100 A

The system is operated at a constant output current, I_0, and the output voltage is varied such that $0 < U_O < d \cdot V_D$. The conversion factor, d, defines the maximum output voltage in relation to the input voltage, V_D. The power losses, P_L, of bridge legs A and B respectively, are measured. The bridge legs are cooled by means of a liquid cooling system. The power losses are measured using a calorimetric method, as described in the next sub-section.

2) Power loss measurements

A direct measurement by means of a multiplication and integration of power transistor current and voltage is efficient but suffers from a limited accuracy due to the high dynamics and bandwidth of the signals.

In order to achieve a sufficient accuracy a specific calorimetric method has been developed. It is based on a liquid cooling system (water), where the bridge legs A and B are mounted on separate cooling blocks as shown in Fig. 14. P_L can be calculated using the temperature rise of the cooling water when passing through the cooling block. Accordingly,

$$P_L = c \cdot m' \cdot (T_{OUT} - T_{IN}) \tag{2}$$

where c is the heat capacity and m' is the mass flow of the liquid, and T_{OUT} and T_{IN} are the outlet and inlet temperatures of the cooling water, respectively. Major sources of inaccuracies from (2) would be the measurement of m' and offset errors in T_{OUT} and T_{IN}. By the definition of $\Delta T = T_{OUT} - T_{IN}$ and $k = c \cdot m'$, (2) can be written as

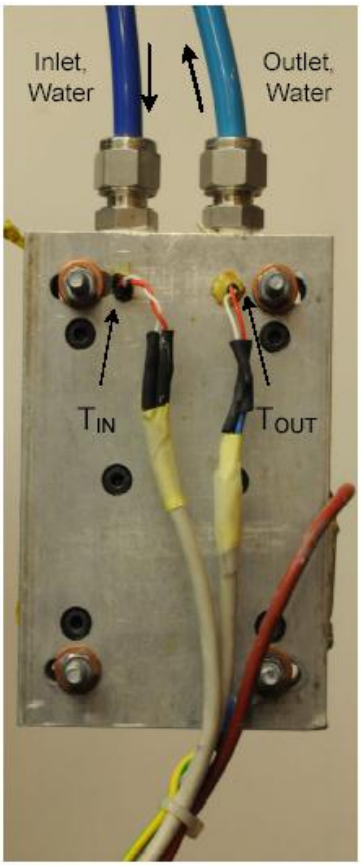
$$P_L = k \cdot \Delta T \quad . \tag{3}$$

In order to address the error sources two measures are taken: the flow rate is not measured but kept constant during the measurements and the system is calibrated at two different load points, P_{L0} and P_{L1}. This gives

$$P_L = P_{L0} + \Delta T \cdot \frac{P_{L1} - P_{L0}}{\Delta T_1 - \Delta T_0} \quad , \tag{4}$$

where ΔT_0 and ΔT_1 are the temperature rises at P_{L0} and P_{L1} respectively.

The constant flow rate is achieved by letting the liquid flow from an upper tank to a lower tank, both being on fixed elevations. The offset errors of the temperature measurements are compensated for by the calibration. The calibration is performed by operating the power transistors in the on state and applying a constant direct current. The power is determined by measuring the voltage across and the current through the power transistor bridge leg. This can be made with a high accuracy since both the voltage and the current are dc quantities. Employing the described method an inaccuracy of less than 2% at a sampling time of 2 min is obtained.



(a)

(b)

Fig. 14. IGBT cooling block: (a) Rear side, (b) Front side

B. Experimental results

The tests have been performed using the devices presented in Table VI. The mechanical layout of the test devices is the same as used for the conduction loss measurements, see Section II *B*. The selected test devices represent three different SiC technologies MOSFET (A), BJT (B), and JFET (C). Device C (VJFET) is selected from the group of JFET devices based on results of the conduction loss measurements, as presented in Table II. Device B (BJT) has a smaller total chip area compared to the conduction loss measurement. This was done in order to obtain a better comparision of the results with device C. The test devices (A-C) do all include an antiparallel SiC Schottky diode associated to each switch. The blanking time of the gate signals is kept constant at 2 μs for all tests. This means that for the test devices A and C, which are unipolar, the reverse current is conducted by the transistor and diode in parallel but for the other test devices the diode is carrying the reverse current solely. The different tests are performed under similar cooling conditions.

Table VI

Test devices for system loss measurements

Device	Technology.	Area (mm^2)	Area (%)	Type	Supplier
Ref	Si IGBT	512	100	SKM400GB125D	Semikron
A	SiC MOSFET	101	20	CMF20120D	CREE
B	SiC Bipolar	73	14	BT1220AC	Transic /Fairchild
C	SiC VJFET Normally-off	54	11	SJEP120R063	SemiSouth

Fig. 15 shows results from the power loss measurements in the system performance test. The losses are measured at a constant output current, I_0=100 A, for different output voltages, $0 < U_O < d \cdot V_D$. The results are plotted as the power losses for one bridge leg as a function of the relative output voltage ($100\% = d \cdot V_D = 360V$).

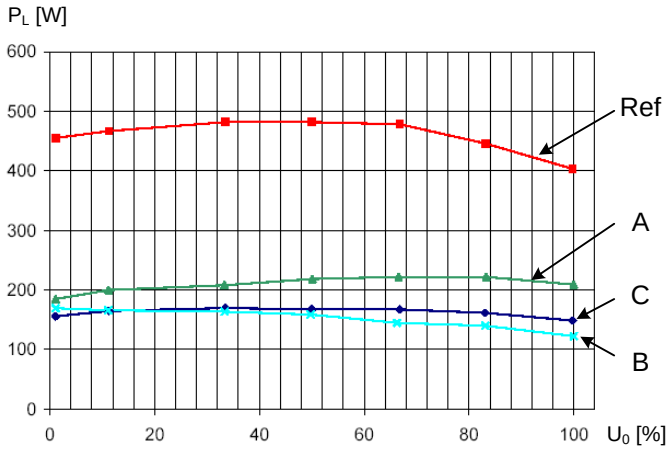


Fig. 15. Power loss measurements obtained from the system test.

From Fig. 15 it is observed that the SiC devices enable a dramatic reduction of the power semiconductor losses. Moreover, this is achieved despite the fact that less material is used. In Table VII the maximum losses for the different test devices are listed both in absolute values, P_{Lmax}, and relative the losses of the Si IGBT, P'_{Lmax}. From Table VII it is observed that the highest relative power loss for any of the SiC devices is 46%. This yields a reduction of power semiconductor loss of more than 50% when compared to the Si IGBT. The most efficient component from this test is device C which shows a loss reduction of 65% using only 11% of the chip area.

Table VII

Test results from system loss measurements

Device	Area (mm^2)	Area (%)	P_{Lmax} (W)	P'_{Lmax} (%)
Ref	512	100	480	100
A	101	20	220	46
B	73	14	170	35
C	54	11	170	35

From the traces shown in Fig. 15 it can be observed that ‘Ref’(Si IGBT) has lower losses at the higher output voltage. This originates from the fact that in this operation region the turn-off current as well as the switching frequency are the lowest, thus minimizing the switching losses. For the unipolar SiC devices (traces ‘A’ and ‘C’) a similar pattern can be observed, while bipolar device (trace ‘B’) shows a continuous decay of the losses for an increasing output voltage. This observation is partly explained by the reverse conduction capability of the unipolar devices since the reverse current is higher at lower output voltages.

Moreover, using the results from Table II and Fig. 12, and estimating T_J=80 °C, to back-calculate the losses from the current and resistance of the power switch, yields for device C P_L=140 W. This value shows a very good match when compared to the measured value as shown in Fig. 15. From this observation the conclusion is made that; in the actual test-operation (soft switching at 30 kHz) the losses are dominated by R_{DSon} of the switch and the switching losses can be neglected. Consequently, the power semiconductor losses may be further reduced by simply increasing the total chip area. Based on the test results, it seems feasible to reach a power loss reduction of 9/10 by using 1/3 of the total chip area when using device C! Both devices A and C have the same potential in loss reduction but will need more chip area to reach the same level. The same loss reductions may also be achieved with device B provided that the losses in the antiparallel diode are not significantly higher than those of the BJT. The latter, however, is challenging and remains to be shown.

IV. Discussion

From the experiments it is obvious that all the tested SiC transistors perform extremely well in the resonant-converter application compared to the best Si IGBTs available. Both the conductivity modulation lag and the tail current, as observed in Si IGBTs [22], have been eliminated by using the selected SiC transistors. From this point of view a replacement of the Si IGBTs offers a substantial loss reduction to the system. This will have an important impact on the converter system. Specifically the cooling system can be implemented at a significantly lower cost, which means that the total cost for the converter may be reduced even though the new SiC transistors are several times more costly compared to Si IGBTs.

The choice between MOSFETs, JFETs, or BJTs in SiC is, however, not obvious. Several application-dependent aspects may have to be taken into consideration. Due to the resonant operation of the circuit, the switching losses will be very low in most operation points. The conduction losses, however, can be chosen by selecting the number of parallel-connected chips per switch position. By increasing the total chip area, on the one hand, the conduction losses are reduced (for all three types of transistors) but on the other hand the cost of the switches is increased. Hence, the converter efficiency may be optimized vs cost. This can be done taking into account first cost (system cost) and operational cost (energy efficiency). Here, the specific cost for each transistor technology becomes interesting. In this aspect, the technology with the lowest cost per conductivity is the preferred choice. In addition to the component cost of the switches also the cost of gate/base drivers has to be considered. Based on the work presented in this paper the normally-ON SiC VJFET seems to be the most cost effective technology in the actual application provided that the component cost is determined by the chip area. However, this is not necessarily true in the future. In order to make such a prediction the internal transistor structures have to be reviewed. Not only the costs for the different process steps have to be evaluated, but also the production yield for each of the three transistor technologies.

The SiC MOSFET includes a gate-oxide layer which is not only hard to fabricate [31] but also may be prone to failure [32]-[34]. Additionally, the channel beneath the oxide layer has a significant contribution to the ON-state resistance. A complicated process stage with a potentially low yield may become a cost driver. The SiC BJT and the SiC VJFET technologies do not differ significantly in complexity regarding production. Moreover, they also seem to have similar conductivities, which imply that they will probably have similar costs per conductivity if both of them are mass-produced.

A closer look at the conduction losses for SiC BJTs, Normally-ON VJFETs and Normally-OFF VJFETs reveals that the dependence on temperature differs considerably, see Table IV and Fig. 12. The SiC BJT has the lowest temperature dependence, the normally-ON VJFET is intermediate, and the normally-OFF VJFET has the highest temperature dependence. From a systems perspective a small positive temperature coefficient is desirable, but the temperature dependence of the conduction losses of the normally-OFF VJFET is higher than what is necessary. Already at room temperature the normally-ON VJFET has considerably lower on-state losses than the normally-OFF JFET [35]. The VJFET can be designed to be either normally-ON or normally-OFF simply by changing the doping level of the channel region. If both designs have approximately the same high source doping, the device may be normally-ON if the gate doping moderate and normally-OFF if the gate doping is lower than for the normally-ON version. Without going into further details, the channel of the normally-ON JFET will not only be wider but also have a higher doping than the channel of the normally-OFF JFET. Unless completely new semiconductor structures are found, normally-ON JFETs will, therefore, have lower ON-state resistances. To conclude, if a choice should be made based on cost per conductivity, the choice should probably be between the SiC BJT and the normally-ON SiC VJFET.

Another important aspect that has to be considered is the antiparallel-diode function. In this context the MOSFET and JFET have a great advantage compared to the BJT. The field-effect transistors (FETs) can be operated with a negative drain current (reverse conduction), but the BJT has to rely on additional antiparallel diodes. This means that the BJT does not only have additional cost related to the diode chips, but will also suffer from diode conduction losses which may by substantially higher compared to the reverse conduction of the FET channel. This, of course, depends on the choice of current density in the FET, but in cases where the SiC switch is used to increase the efficiency, the voltage drop of the FET will be low.

So far, only conduction and switching losses have been considered. From a systems perspective, reliability and cost gate/base-drive circuits must also be considered. In this context, the SiC MOSFET is outstanding, because a slightly modified (higher voltage rating) IGBT driver is sufficient not only to operate the MOSFET, but also to achieve a certain system reliability. As a standard technology can be used, the reliability can largely be estimated based on experience from state-of-the-art IGBT technology. However, the reliability of the gate oxide of the MOSFET may still be a problem.

Both the SiC BJT, the normally-ON SiC VJFET, and the normally-OFF SiC VJFET have a *driver problem*. The problem of the normally-ON VJFET is obvious because a short-circuit of the dc link is obtained if the gate drivers do not provide the necessary negative voltage to the gate in order to keep the VJFET in the OFF-state. This problem can be solved both at the driver level [23] and at the system level [36], but it adds complexity and may reduce the reliability if not treated with meticulous care. The SiC BJT and the normally-OFF VJFET, on the other hand, are normally-OFF devices, but both of them need a significant continuous base/gate current in the ON-state [37], [27]. The power consumption of these drivers is considerably higher than those for the MOSFET or the normally-ON JFET. From an application point-of-view, however, any of the four alternatives would still be acceptable.

During the process of writing of this paper it has been announced that the supplier of the SiC VJFET devices used in the experiments, SemiSouth, is no longer in operation. How this will impact the availability of the technology is presently not clear. In a short term perspective, of course, the availability will suffer. In the long term new suppliers may appear.

V. Conclusion

From the results presented it is clear that all the tested SiC devices offer a significantly improved performance in the evaluated application when compared to an Si IGBT, i.e. lower losses and potentially higher switching frequencies. The SiC MOSFET, the SiC BJT, and the normally-ON SiC VJFET are the most promising technologies for the intended application. It has been shown that both the losses of the system and the total chip area can be significantly reduced. At room temperature the SiC VJFET shows a loss reduction (vs Si IGBT) of 65 % using only 11 % of the chip area.

From an area-per-conductivity point-of-view and taking into consideration the additional area and losses for the antiparallel diode in the BJT case, *it is concluded that the normally-ON SiC VJFET is the most promising switch candidate for the intended application*. It is also likely that this is true for many other applications where SiC technology is considered for efficiency improvements. However, if the focus is on high-temperature operation, the SiC BJT may be at least as interesting as the normally-ON SiC VJFET. The reason for this is that the normally-ON SiC JFET has a higher temperature coefficient of the ON-state voltage drop than the SiC BJT and that this compensates for the additional area of anti-parallel diode.

Acknowledgment

Mietek Bakowski is greatly acknowledged for sharing his deep knowledge in theory and design of power semiconductors. Raad

Al Sundook is acknowledged for being of great help with the experimental setup and arrangements. The suppliers of test devices are acknowledged for their support.

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