An HTS Quasi-One Junction SQUID-Based Periodic Threshold Comparator for a 4-bit Superconductive Flash A/D Converter

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Abstract—**An all high-T_c periodic threshold comparator for application in a 4-bit superconductive A/D converter has been realized and tested. The theoretical threshold curve of the comparator is calculated and compared to the measured results. Furthermore, the thermal noise immunity and the influence of flux-flow are considered, resulting in practical design constraints for the comparator circuit.**

I. Introduction

PERIODIC threshold comparators can be used to construct a flash analog-to-digital converter with only one comparator per bit. Several low-T_c periodic threshold comparators have been reported previously. The first designs were based on the periodic threshold curve of two (or more) junction SQUID's. Although these circuits could be operated at very high sampling rates, it appeared that the analog input bandwidth was severely limited by the dynamic behavior of the SQUID's [1]. Much larger analog input bandwidths can be obtained by using a comparator based on a quasi-one junction SQUID (QOS), as was first proposed by Ko [2]. So far, several low-T_c QOS-based comparator circuits have been reported [2]–[7]. An all high-T_c (HTS) design was proposed in [8]. In this design, the two Josephson junctions in the QOS were constructed at two parallel ramp-edges, which allows realization of a very small loop inductance. In this paper, this QOS structure is further analyzed. The ideal theoretical threshold curve is calculated and design constraints due to thermal noise and flux flow are considered.

In Section II the basic operation of a QOS-based comparator is discussed and the threshold curve is calculated for various circuit parameters. Thermal noise immunity and the influence of flux flow are considered in Section III. Next, in Section IV a practical implementation is discussed. Measurement results are presented in Section V.

II. Basic Operation of the QOS-Based Comparator

Fig. 1(a) shows the equivalent circuit of the basic QOS-based comparator. In this circuit the current through the digitizing junction J_0 is a periodic function of the analog input current I_a as indicated in Fig. 1(b). The critical current of J_0, I_{c0}, must be much smaller than the critical current I_{cS} of the sampling junction J_S, in order that the influence of J_S on the behavior of the QOS is small. In that case, the periodic curve of Fig. 1(b) is single valued for all values of I_a if [2]

$$\beta_L = \frac{2\pi \cdot L \cdot I_{c0}}{\Phi_0} < 1, \tag{1}$$

where Φ_0 is the flux quantum. For high frequency operation the value of β_L is preferably less than 0.5. For a 4-bit A/D converter the periodic curve should contain at least 4 full periods.

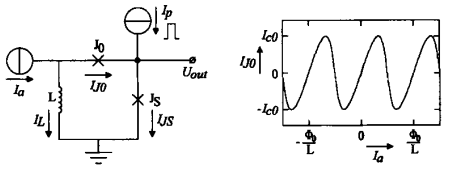

Fig. 1. (a) Equivalent circuit of QOS-based periodic threshold comparator and (b) the periodic dependence of the QOS current I_{J0} on the analog input current I_a.

Sampling pulses I_p are applied to sample the direction of the circular QOS current I_{J0}. For a properly adjusted amplitude of I_p the sampling junction J_S switches to the resistive state for 50% of the values of I_a. Each time that the sampling junction switches this results in a voltage at the output node of the circuit, which is considered to be a logical '1'. This is considered to be a logical '0' when a sampling pulse I_p does not give rise to an output voltage.

It is not simple to calculate the required amplitude of the sampling pulses I_p and the values of I_a for which the sampling junction J_S will switch, because the circular QOS current I_{J0} and the sampling pulse do not simply add up in J_S. In fact, the sampling pulse disturbs the actual value of I_{J0}. The threshold curve of the comparator, that is the value of I_p as a function of I_a that is just enough to make J_S switch, can be calculated by applying the flux quantization principle to the QOS loop

$$\Phi + \frac{\Phi_0}{2\pi} \cdot (\varphi_{J_0} + \varphi_{J_S}) = k \cdot \Phi_0, \text{ with } k = 0, \pm 1, \pm 2, \cdots \tag{2}$$

where $\Phi = -I_L \cdot L$ represents the flux contained in the loop, and φ_{J_0} and φ_{J_S} represent the phase jumps across the junctions in the loop. Taking $k = 0$ and applying Kirchhoff's

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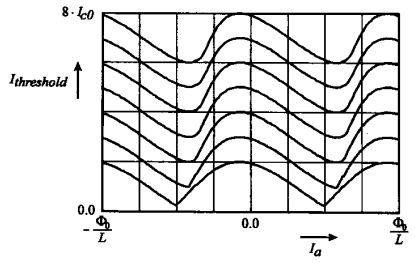


Fig. 2. Calculated QOS threshold curves for critical current ratios I_{cS}/I_{c0} changing from 1 to 7. The value of the inductance L was chosen in order that $\beta_L = \frac{2\pi L I_{c0}}{\Phi_0} = 0.5$.

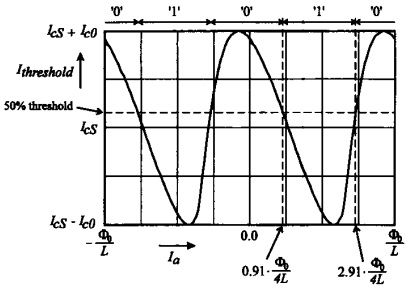


Fig. 3. Calculated threshold curve for a QOS with $I_{cS} = 4 \cdot I_{c0}$ and $\beta_L = 0.5$.

current law to the input and output nodes of the QOS, we can easily derive the following relation between the analog input current I_a, the sampling current I_p and the phase drop across the digitizing junction

$$I_p = I_{cS} \cdot \sin\left(\frac{2\pi L}{\Phi_0}\{I_a - I_{c0} \cdot \sin(\varphi_{J_0})\}\right) - I_{c0} \cdot \sin(\varphi_{J_0}). \quad (3)$$

For given values of I_a and I_p, the phase of J_0 will be adapted in order that (3) is satisfied. The value of I_p for which the sampling junction J_S will switch is reached when (3) can no longer be satisfied for any value of φ_{J_0}. Therefore, the threshold value of I_p is equal to the maximum of the righthand side of (3)

$$I_{\text{threshold}} = \max\left[I_{cS} \cdot \sin\left(\frac{2\pi L}{\Phi_0}\{I_a - I_{c0} \cdot \sin(\varphi_{J_0})\}\right) - I_{c0} \cdot \sin(\varphi_{J_0})\right] \quad \text{for } \varphi_{J_0} = 0 \cdots 2\pi. \quad (4)$$

Fig. 2 shows plots of the threshold curve (4) for several critical current ratio's I_{cS}/I_{c0} and a value of L, such that $\beta_L = 0.5$.

We see that the shape of the threshold curve does not change very much for critical current ratios of 3 and higher. For lower ratios the influence of J_S on the QOS behavior increases and for a ratio of one we obtain the well-known threshold curve of a two-junction SQUID (the slight asymmetry is caused by the fact that I_a and I_p are inserted asymmetrically).

For each of the threshold curves in Fig. 2(a) the value of $I_{\text{threshold}}$ can be calculated at which the sampling junction J_S switches for 50% of the values of I_a. This is shown in Fig. 3 for the threshold curve with a critical current ratio of 4. We see that the threshold curve is a periodic function around the critical current I_{cS} with minimum and maximum values of $I_{cS} - I_{c0}$ and $I_{cS} + I_{c0}$. However, contrary to what is stated in other publications, the value of $I_{\text{threshold}}$ at which J_S switches for 50% of the analog input values is not equal to I_{cS} due to the asymmetric shape of the threshold curve. In Fig. 3 the correct value is indicated by the horizontal dashed line. For that value the sampling junction switches in the '1' intervals and does not switch in the '0' intervals.

As mentioned previously, the main reason to use a quasione junction SQUID instead of a symmetrical two junction SQUID is the improved dynamic behavior and the resulting larger analog input bandwidth. The critical current of the sampling junction J_S should be significantly higher than the critical

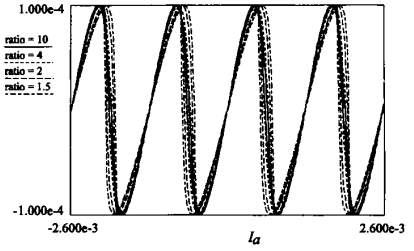


Fig. 4. JSIM simulation showing dynamic hysteresis in the circular QOS current for a sinusoidal input current I_a with a frequency of 1 GHz and an amplitude of 4 Φ_0/L. The hysteresis increases with a decreasing critical current ratio I_{cS}/I_{c0}.

current of J_0, in order that the influence of J_S on the dynamic behavior of the QOS is small. However, as will be apparent from the discussion on thermal noise and flux flow in the next section, it is also desirable to choose the critical current ratio as small as possible. From the threshold curves in Fig. 2 we can conclude that at low operating speeds a ratio of 3 would be enough. At larger ratios the shape of the curves does not change very much. The influence of the critical current ratio on the dynamic behavior of the QOS was investigated with the help of SPICE and JSIM simulations using realistic parameters based on measurements on individual junctions. At high analog input frequencies the periodic dependence of the circular QOS current on I_a as indicated in Fig. 1(b) shows a dynamic hysteresis. Fig. 4 shows the results of a JSIM simulation for a sinusoidal input current I_a with a frequency of 1 GHz and a peak-to-peak amplitude of 4 Φ_0/L, which corresponds to 4 complete periods of the threshold curve (4 periods are required for the least significant bit comparator in a 4-bit A/D converter). From these results it is clear that the dynamic hysteresis becomes larger for smaller critical current ratios, as expected. Fortunately, the increase of the hysteresis is largely nonlinear with the decrease of the critical current ratio: a change in the critical current ratio from 10 to 2 results in almost the same increase as a change from 2 to 1.5. The increase in dynamic hysteresis stays well-within acceptable limits for critical current ratios of 3 and higher.

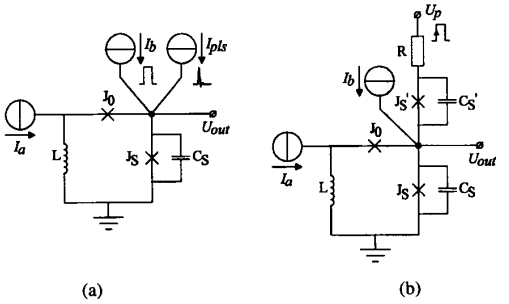
The simulations of Fig. 4 were performed for the ideal equivalent circuit of Fig. 1(a),with realistic junction parameters, but without additional parasitic capacitance or inductance. The junction I_cR_n product was 1 mV. The hysteresis shown

in Fig. 4 can be completely explained by resistive currents due to the voltages across the junctions at high signal frequencies. Thus, for a minimum hysteresis the junction normal resistance should be as high as possible. Another way to reduce the hysteresis is to reduce the parameter β_L (1), which can be accomplished by either decreasing the critical current of J_0 or by decreasing the loop inductance L. However, decreasing the critical current of J_0 is limited by the required level of thermal noise immunity—which will be discussed in the next section—and decreasing L will also decrease the input sensitivity, because the threshold period is inversely proportional to the value of L. An interesting circuit to decrease the hysteresis by decreasing the *effective* critical current of J_0 was proposed by Ko [7]. However, for the current status of the technology this circuit is too complex for a HTS realization. Instead of reducing the hysteresis itself, it is also possible to decrease its influence by using some sort of redundant coding [3], [9].

The influence of parasitic capacitance in parallel and parasitic inductance in series with the junctions was also investigated by simulations. The results showed that a parallel capacitance for the digitizing junction J_0 causes resonances and a considerable increase of the hysteresis. A capacitance in parallel with J_S, however, does not have much influence even for values of several picofarads. Additional inductance in series with the junctions causes an increase of β_L and, thus, an increase of the hysteresis. This increase can be compensated for by decreasing the loop inductance L.

Besides the dynamic hysteresis, a major source of errors at high-frequency operation is the aperture time of the converter, i.e., the time the converter needs to acquire a sample of the input signal. During this time the input signal may not change more than 0.5 lsb. For a 4-bit A/D converter and a required analog input bandwidth of several GHz, the maximum allowable aperture time is in the order of a few picoseconds. However, it is not very practical to apply picosecond sampling pulses to the basic QOS circuit of Fig. 1(a) because of the rather large required pulse amplitude and the fact that the resulting output pulses can hardly be detected. In his original design [2], [3] Ko proposes to use a short sampling pulse $I_{\rm pls}$ superimposed on a much larger, slower bias pulse I_b, as indicated in Fig. 5(a). In that case the narrow sampling pulse causes J_S to switch and the wider bias pulse causes J_S to remain switched for a time that is sufficient to detect the output pulse. Of course, in that case J_S has to be hysteretic. As our junctions are normally not hysteretic we have to apply capacitive shunting to make J_S hysteretic [10], [11]. Simulations show that in our case a value of C_S between 2 and 5 pF is sufficient.

A problem with the circuit in Fig. 5(a) is that close to a threshold level its response to a sampling pulse is rather slow. Simulations show that delays of several tens of picoseconds may occur. Therefore, we prefer an edge-triggered version of the circuit as proposed by Bradley [4]–[6]. This circuit is shown in Fig. 5(b). Instead of a current pulse a voltage pulse U_p is used for sampling. This voltage pulse is applied to the QOS through a series connection of a small resistor R and a Josephson junction J_S' which is identical to J_S. Now, at the rising edge of U_p the current through R, J_S' and J_S



(a) (b)

Fig. 5. A short aperture time can be obtained by superimposing a short sampling pulse upon a longer bias pulse (a) or by using an edge-triggered version of the circuit (b).

starts to increase, until either J_S or J_S' switches. Once one of the junctions has switched, the current through the circuit drops due to the normal resistance of this junction and the other junction is prevented from switching. Note that it is still necessary that the junctions are hysteretic, which is why capacitive shunting is needed for both J_S and J_S'. The current I_b in Fig. 5(b) is a dc-bias current which is needed because the 50% threshold (Fig. 3) is slightly larger than the critical current of J_S and to compensate for mismatch between J_S and J_S'.

III. Thermal Noise Immunity and the Influence of Flux Flow

Three energy terms have to be considered to give an estimate of the influence of thermal noise. The first is

$$E_\Phi = \frac{\Phi_0^2}{2L} \tag{5}$$

i.e., the energy barrier between two adjacent flux quantum states in a superconducting loop with inductance L. The second is the Josephson coupling energy

$$E_J = \frac{\hbar I_c}{2e}. \tag{6}$$

The third is the thermal noise energy

$$E_{\rm th} = k_B T. \tag{7}$$

The noise immunity requirement can now be expressed as $E_{\rm th} \ll E_\Phi$ and $E_{\rm th} \ll E_J$. It is easy to show that the first requirement is usually less stringent than the second one, so we will focus the discussion on the latter.

As was first shown by Ambegoakar and Halperin [12], a Josephson junction obeying RSJ characteristics and having a noise source may in the case of strong damping be treated as the Brownian motion of a particle in a tilted washboard potential. For low bias currents and hence low tilt angle the number of phase slips per second is then given by

$$f = f_A \cdot e^{-\gamma} \tag{8}$$

where $f_A = \frac{I_c R_n}{\Phi_0} \approx 10^{12}$ Hz is the attempt frequency in the case of over damped junctions using $I_c R_n = 2$ mV, and $\gamma = \frac{2E_J}{E_{\rm th}}$. Furthermore, γ has to be large in this approximation. The limits of the validity of this equation have been discussed in detail by Lee [13].

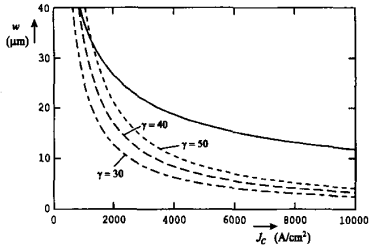


Fig. 6. Minimum (dashed lines) and maximum (solid line) junction widths as a function of the critical current density. The maximum width is defined by the requirement of RSJ-like junction behavior. The minimum junction width is defined by the noise-immunity requirement and is dependent on the required value of the noise parameter γ. All curves are calculated for a junction thickness of 100 nm and an operating temperature of 40 K.

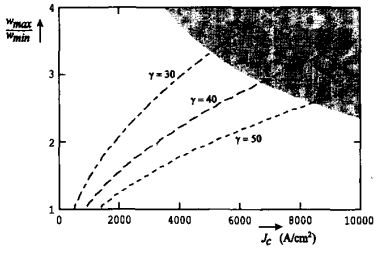


Fig. 7. Ratio between the minimum and maximum junction widths as a function of the critical current density. The shaded area indicates where the minimum junction width is smaller than 5 μm, which is the minimum feature size in our process.

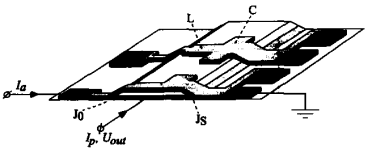


Fig. 8. Layout of the all HTS QOS design. The two junctions J_0 and J_S are situated at parallel ramps.

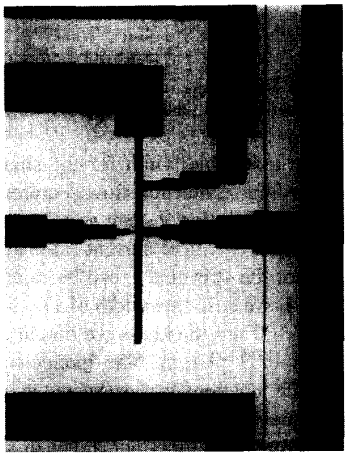


Fig. 9. Microphotograph of a realized comparator test structure. The two parallel ramp edges are clearly visible, with the smallest junction J_0 at the left and the junctions J_S and J_S' at the right side.

Specifying a minimum acceptable value for the noise parameter $\gamma \geq \gamma_0$ one may formulate a lower bound for the Josephson coupling energy E_J

$$E_J \geq \frac{1}{2}\gamma_0 E_{\text{th}}. \tag{9}$$

Substituting (6) and (7) into (9) results in a minimum value for the junction critical current

$$I_c \geq \frac{\gamma_0 e k_B T}{\hbar} \tag{10}$$

or, for a given critical current density J_c and junction thickness d, we have the following lower bound to the junction width w

$$w \geq \frac{\gamma_0 e k_B T}{\hbar d J_c}. \tag{11}$$

The requirement that the junctions can be described by the RSJ model, i.e., do not show flux flow behavior, results in an upper bound to the junction width [14], [15]

$$w \leq 4\lambda_J \tag{12}$$

where

$$\lambda_J = \left(\frac{\hbar}{4e\mu_0 J_c \lambda_L}\right)^{-1/2} \tag{13}$$

if we neglect the thickness of the junction barrier with respect to the London penetration depth λ_L.

Fig. 6 shows a plot of the minimum junction width (dashed lines) resulting from (11) and the maximum junction width (solid line) defined by (12) as a function of the critical current density J_c. The minimum junction width is plotted for three different values of γ_0. We see that only a small range of acceptable junction widths remains if both criteria have to be fulfilled. This severely limits the choice of the junction critical current ratio in the QOS comparator circuit. For a given critical current density, the largest critical current ratio is obtained if the digitizing junction J_0 has the minimum width defined by (11) and the sampling junction has the maximum width given by (12).

Fig. 7 shows a plot of the ratio between the maximum and minimum junction widths. Note that this ratio cannot be smaller than 1. The shaded area in this figure indicates where the minimum junction width is smaller than 5 μm, which is the minimum feature size in our process. We can conclude that with this minimum feature size it makes no sense to increase the critical current density above 6000 A/cm^2. With this critical current density at an operating temperature of 40 K a junction ratio of 3 is feasible with a noise parameter γ of 30.

IV. Design and Fabrication of a Practical Comparator

The layout of the all-HTS QOS is shown in Fig. 8. The two Josephson junctions are located at parallel ramps. The loop inductance L is implemented as a 11-μm wide stripline on top of the structure. The parallel capacitance of J_S, which is necessary to make this junction hysteretic, is easily implemented by the wider part at one side of the stripline.

From Fig. 7, we can conclude that for a maximum critical current ratio I_{cS}/I_{c0} we should aim at a critical current density for the junctions of 4000 to 6000 A/cm^2, which is a reasonable

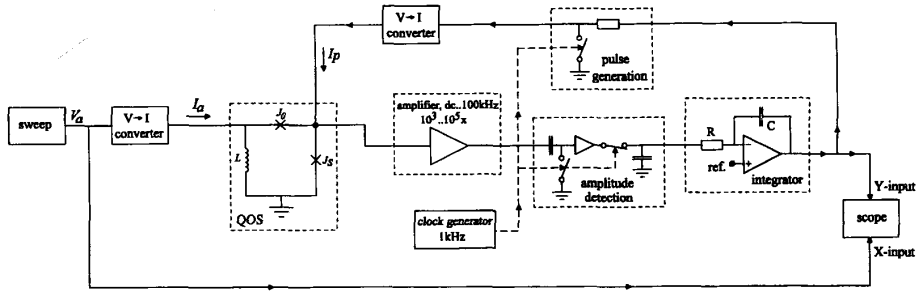


Fig. 10. Measurement setup for measurement of the QOS threshold curve. The amplitude of the sampling pulses is controlled in a feedback loop in order to keep junction J_S at the edge of switching.

value. In that case a suitable width for the smallest junction J_0 is 5 μm. According to the flux flow requirement (17) the width of the sampling junction J_S can now be chosen as large as 15 μm, resulting in a critical current ratio of 3.

The inductance of the strip line L can be calculated according to Chang [16]. For a strip line width of 11 μm and a PBCO insulation layer of 100 nm thickness we obtain an inductance per unit length of 0.07 pH/μm. The inductance due to the overlap area's of the junctions was estimated at approximately 0.6 pH, mainly due to the narrow width of the digitizing junction J_0. Thus, for a total loop inductance of about 1 pH the strip line should have a length of approximately 6 μm. Note that the influence of kinetic inductance is neglected. Therefore, in practice the inductance will be somewhat larger. The value of the capacitance C per unit area was estimated to be about 5×10^{-4} pF/μm^2.

A test chip was designed containing 12 QOS structures of various dimensions. All QOS structures have an additional junction J_S' connected to the output node to allow for edge-triggered sampling, as discussed in Section II. This additional junction is easily realized at the same ramp edge as the sampling junction J_S. In all cases the width of the digitizing junction J_0 was 5 μm. For the sampling junctions widths of 10, 15, 20, and 25 μm were used, resulting in critical current ratios of 2, 3, 4 and 5.

Fabrication of the test chip involves the following process steps [8]:

1) Sputter deposition of an YBCO/PBCO double layer.
2) Photolithography and ion-beam milling of both ramp-edges. Unlike our previously published results [8] the two ramp edges are now made simultaneously. The substrate is rotated by 180° periodically to improve the matching between the ramps.
3) Ion-beam cleaning (*in situ*) of the ramp edges, followed by sputter deposition of the PBCO junction barrier and the YBCO counter electrode.
4) Photolithography and sputter deposition of Ti/Au metal contacts by a lift-off technique.
5) Photolithography and ion-plasma etching for structuring of the YBCO top electrode.

V. Measurement Results

So far, several test chips have been fabricated. Fig. 9 shows a microphotograph of a single QOS test structure complete with the additional junction J_S' for edge-triggered sampling. Unfortunately, the majority of the test chips appeared to suffer either from shorts in the PBCO junction barriers and isolation layer or from a poor quality YBCO top electrode. From the fact that individual junctions usually worked well, i.e., show RSJ-like characteristics without excess current, we concluded that shorts in the barriers are not a major issue. By using Ga-doped PBCO the isolation between top and bottom electrodes may be increased. A further process optimization is necessary to improve the circuit yield. Nevertheless, we were able to perform some promising tests on working structures.

For measurement of the QOS threshold curve we used the measurement setup shown in Fig. 10. A square-wave current (I_p) is used for sampling of the QOS. A rather low frequency of 1 kHz was chosen because of the long cables connecting the QOS to the room-temperature circuitry. The resulting square-wave output voltage is amplified and the amplitude is detected. Next, the amplitude is compared to a reference level and the difference is integrated and used to adjust the amplitude of the sampling current I_p in a feedback loop. By adjusting the reference level to a very low value just above the noise level, the junction J_S can be kept just at the edge of switching while a sweep is applied as the analog input current I_a.

Fig. 11 shows a typical measured threshold curve of a good QOS structure. The expected periodic characteristic can be clearly recognized with a period of approximately 1.4 mA. This period corresponds to a loop inductance L of about 1.45 pH, which is somewhat larger than the calculated value of 1.2 pH. However, this can be completely explained by additional kinetic inductance, which can be quite large, especially for a poor quality YBCO top electrode. An order of magnitude estimate indicates that the kinetic inductance may be as high as 50% of the geometric inductance.

A problem with the QOS structure of Fig. 8 is that the analog input current I_a flows directly over the junctions and the associated magnetic field causes the critical currents of the junctions to be suppressed. This is clearly visible from the measured curve of Fig. 11. With an increasing value of I_a, the amplitude of the modulation decreases, due to suppression of the critical current of J_0. The entire curve is bended due to suppression of the critical current of J_S. Therefore, research now focusses on slightly different QOS structures where the magnetic field associated with the analog input current does not penetrate the junctions.

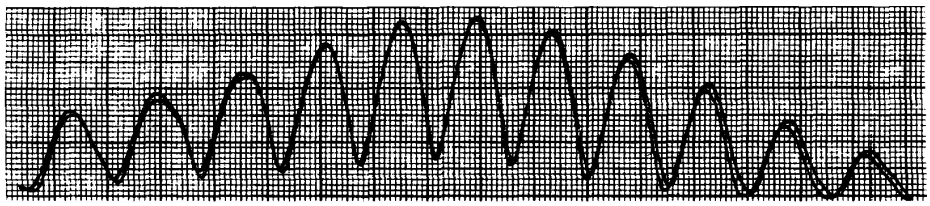


Fig. 11. Typical measured threshold curve for a QOS with a critical current ratio of 3 and a strip line length of 9 μm. The suppression of the junction critical currents due to the magnetic field associated with the input current I_a is clearly visible. Scales: horizontal I_a, 1 mA/cm, vertical I_p, 50 μA/cm.

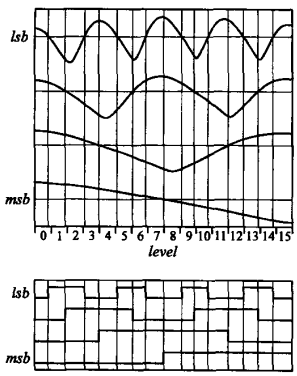


Fig. 12. Measured threshold curve of a single QOS as it is used to realize each bit in a 4-bit A/D converter. The top traces show the part of the measured threshold curve that is used. The bottom traces show the output signals of the resulting A/D converter.

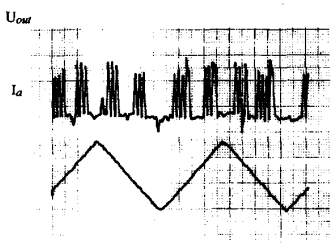


Fig. 13. Low speed digitizer test. The analog input signal I_a has a frequency of about 50 Hz. The sampling frequency is 1 kHz. The poor representation of the output pulses is due to the limited resolution of our sampling oscilloscope. Scales: U_{out}: 100 μV/cm, I_a: 1 mA/cm.

Still, the measurement results obtained so far are adequate for realization of a 4-bit A/D converter, which requires only 4 periods of the threshold curve. This is illustrated in Fig. 12, which shows the measured threshold curve of a single QOS as it would be used for each bit in the converter.

Operation of the QOS structures as a periodic comparator was demonstrated at low speeds by applying a 1 kHz square-wave signal to the sampling input. Fig. 13 shows a typical result of this test. The output pulses appear periodically as a function of the input current I_a. A digital sampling oscilloscope was used to acquire the input and output signals. The limited horizontal resolution of the oscilloscope of 256 points results in the rather poor representation of the output pulses, because only a few samples are taken per pulse.

VI. Conclusion

An all-HTS periodic threshold comparator for application in a 4-bit A/D converter has been designed, fabricated, and tested. An analysis was provided with respect to thermal noise immunity and the influence of flux flow, resulting in minimum and maximum widths for the Josephson junctions in the circuit. Several test chips were realized, each containing 12 comparator structures with various dimensions. Measurement results show that the threshold curves of the comparators have more than enough periods as required for a 4-bit A/D converter. However, in the current design it appears that the threshold curve is also directly modulated by the analog input current. Research now focusses on adapting the QOS structure to eliminate this effect. Nevertheless, operation of the comparator has been demonstrated at slow sampling speeds, indicating that an all-HTS 4-bit A/D converter based on these comparators is feasible, given the current state of the ramp type technology we used.

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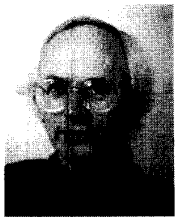

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