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AN IMPLANTABLE MIXED ANALOG/DIGITAL NEURAL STIMULATOR CIRCUIT

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ABSTRACT

This paper describes a chip for a multichannel neural stimulator for functional electrical stimulation. The chip performs all the signal processing required in an implanted neural stimulator. The power and signal transmission to the stimulator is carried out via an inductive link. From the signals transmitted to the stimulator, the chip is able to generate charge-balanced current pulses with a controllable length and amplitude for stimulation of nerve fibres. The chip has 4 output channels so that it can be employed in a cuff electrode with multiple connections to a nerve. The purpose of the functional electrical stimulation is to restore various bodily functions (e.g. motor functions) in patients who have lost them due to injury or disease.

1. INTRODUCTION

Functional electrical stimulation is the activation of physical functions through electrical stimulation of nerve tissue. It can be applied for instance to victims of spinal chord injuries who have lost control over part of their body (paralysis) or to patients suffering from foot drop. By stimulating the nerves controlling the muscles, some degree of muscular control is regained. Several implantable solutions to this problem have been described in the literature, e.g. [1, 2], each with their distinctive features. For the stimulator described here, an important consideration is the physical size and the option of having several output channels. The stimulator is an implantable unit comprising electrodes to contact the nerves, a signal processing chip to generate the stimulation pulses, and a coil (and some few other discrete devices) to provide an inductive data and
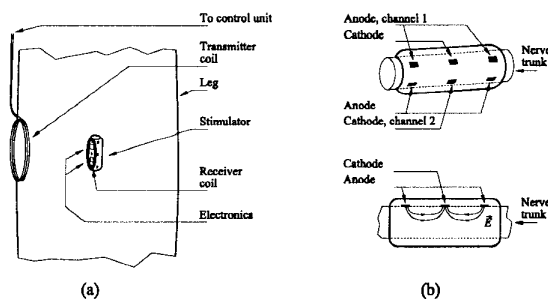

Figure 1. Placement of implanted stimulator and transmitter coil on the lower leg (a). Cuff electrode (perspective view and electric field during stimulation) (b).
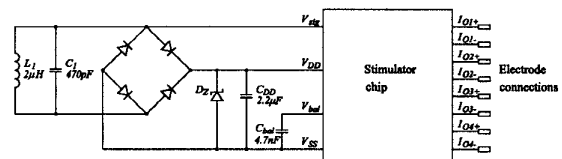

Figure 2. The stimulator components

power link to the stimulator. To keep the size small it is not only necessary to minimize the number of discrete components but also to pay attention to the size of the signal processing chip. In addition to the implanted stimulator, the system comprises a control unit and a transmitter coil placed on the surface of the skin as shown in fig. 1(a). The implanted stimulator is a small unit placed around a nerve fibre with so-called cuff electrodes to connect the stimulator outputs to the nerve tissue. Fig. 1(b) shows the cuff electrode.

2. SYSTEM SPECIFICATION

Some of the important system requirements are the following: The system must be powered via the inductive link. The stimulation pulses are current pulses which must be programmable in amplitude and duration and each stimulation pulse must be followed by a pulse in the reverse direction ensuring that no charge build-up takes place in the nerve tissue. The maximum amplitude is $2mA$ and the maximum pulse duration is $255\mu s$. The nerve tissue can be expected to exhibit an ohmic resistance of up to $5k\Omega$, implying that the stimulator must be able to generate stimulation pulses of up to $10V$ amplitude. It must be possible to direct the stimulation pulse to a selected electrode among a total number of at least 4 electrodes.

To meet these requirements a low power signal processing chip is required with a unidirectional transmission protocol to program the stimulator pulses and a carrier and modulation scheme which ensures a sufficient power supply.

Fig. 2 shows the stimulator components. In addition to the chip and the coil, a tuning capacitor, a rectifier with a filter capacitor and a capacitor for the charge balancing of the stimulation pulses are required. Also, an external zener diode, D_Z, provides a shunt regulation and overvoltage protection for the chip.

3. TRANSMISSION PROTOCOL

For the power and data transfer to the stimulator, an inductive link with a carrier frequency of $5MHz$ has been chosen. This frequency is chosen as a compromise between inductive coupling

(best at high frequencies), and small absorption of tissue and simple electronics (best at low frequencies). The carrier signal is rectified and filtered by the external diode D_1 and the capacitor C_{DD} shown in fig. 2. The supply voltage V_{DD} has been selected to $12V$ in order to be able to generate $2mA$ current pulses into a $5k\Omega$ load. The supply voltage is controlled by the external zener diode D_Z. The data signal is encoded by a pulse amplitude modulation of the carrier with on-off keying. The data rate has been selected to $100kbits/s$. This modulation has been selected because of its simplicity and robustness against imperfections in the transmission but it has the disadvantage that no clock or power is transmitted during the off keying. Hence, the clock recovery circuit must be able to maintain a stable clock frequency during the off keying intervals. For the control of pulse length and amplitude 8-bit words are chosen. Also, to select the output channel for the stimulation, an 8-bit word is chosen. This means that the same transmission protocol can be employed for stimulators with up to 255 output channels. The complete command word to the stimulator is as shown in fig. 3. In addition to the channel select, amplitude and duration control there are two start bits and a cyclic redundancy check word (CRC) for error detection.

4. THE CHIP BLOCK DIAGRAM

A simplified block diagram of the chip is shown in fig. 4. The chip comprises a number of analog circuits functions in addition to a digital control circuit and a digital to analog converter for the pulse amplitude control.

4.1. Voltage regulator

The voltage regulator contains a bandgap reference which is used to control a series regulator for a $3.3V$ supply to the digital blocks in the chip. The main reason for introducing the series regulator is to save power. The power consumption of CMOS logic increases with the square of the supply voltage. At $3.3V$ the CMOS logic is expected to draw about $80\mu A$ leading to a power consumption of about $0.26mW$. With a $12V$ power supply the consumption would be about $3.4mW$, so the series regulator provides a significant power saving even though about $0.7mW$ is dissipated in the series pass transistor of the regulator. The series regulator is fairly conventional.

4.2. Input circuit and clock recovery

The input circuit serves the purpose of extracting the carrier for the generation of the system clock and detecting the modulation for retrieving the data transmitted to the stimulator. Basically, the clock is derived directly from the input signal by taking the signal through a clipping source follower stage, followed by a couple of inverters. The clock derived in this way is of course only detected when the amplitude of the input signal is high, corresponding to a logic 1. When the input is low, no clock signal can be detected since the modulation scheme is a simple on/off keying.
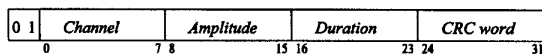
0 1	Channel	Amplitude	Duration	CRC word
0		7 8	15 16	23 24	31

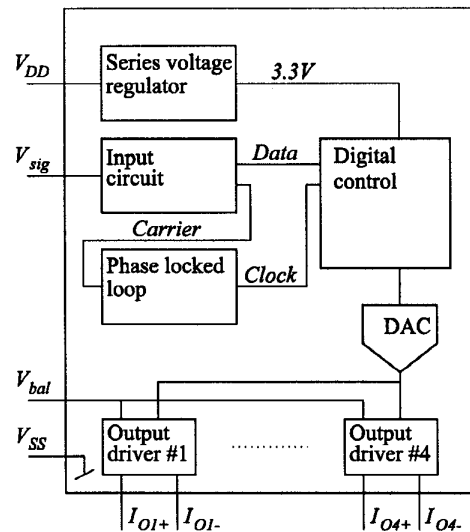**Figure 3.** The command word

Figure 4. Chip block diagram

4.3. Envelope detection

The envelope detection is done by means of the charge pump circuit shown in fig. 5. The capacitor C_{LP} is continuously discharged by the constant current source I_3. When the carrier is present (i.e. a logic 1 is transmitted), C_{LP} is charged through $M4$ and the current source I_4. The capacitor voltage is at equilibrium when the carrier duty cycle is equal to I_3/I_4 or $1/4$. When the duty cycle is higher, as when the input signal is near maximum amplitude, the capacitor voltage tends to $3.3V$ (the digital supply voltage). Conversely, when the duty cycle is lower or even zero, the capacitor voltage tends to V_{SS}. A ripple of about $\Delta V = I_3/(2C_{LP}f_{carrier})$ will be present on the capacitor when the voltage is high due to the discharge when the clock is low. By selecting proper current levels ($I_3 = 2\mu A$) and capacitor size ($1pF$) the ripple can be kept very small and it is filtered out by the current limited inverter $M5 - M6$ and the following standard digital inverter.

4.4. Phase-locked loop

The main purpose of the phase-locked loop is to provide a stable clock for the chip, and to assist in the demodulation of command word transmissions. The loop locks onto the carrier frequency during the unmodulated intervals between pulses, and during logic '1' transmissions. During logic '0' transmissions, the frequency of the loop is fixed. This is done by using a carrier detect signal to enable
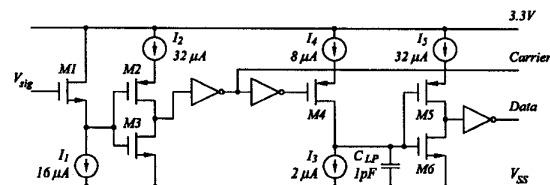
Figure 5. The data input stage

the frequency acquisiontion of the loop. The output frequency of the loop is divided by 5 to provide the $1MHz$ system clock.

The PLL is constructed in a traditional manner, with a phase-frequency detector (PFD), a charge pump filter and a G_m-C voltage controlled oscillator (VCO). A simplified diagram is shown in fig. 6. The VCO is of a type which is suitable for low-power operation at the low MHz frequencies used is this system, and features well-controlled center and operating frequencies [6].

The loop filter is a charge pump, implemented as a passive filter impedance driven by two switched current sources with opposite signs. A detailed analysis of this type of loop filter can be found in [7]. The filter impedance is of second order, making a 3rd-order loop. The main passive component of the filter is a relatively large capacitor, whose value controls the transient behavior of the loop. Simulations indicated that a suitable capacitor size is $100-300pF$, which is quite large but still integrable. An external capacitor was however used, to permit measurements with varying values.

The lock range of the loop is equal to the frequency range of the VCO, which was set to 2.5-$10.0MHz$. The loop draws an average current of $50\mu A$ from the $3.3V$ digital supply, when locked on a $5MHz$ input signal. The largest part of the supply current is used by the VCO.

The frequency memory feature of the PLL is implemented by adding an enable signal to the current sources in the charge pump. When the pump is disabled, the VCO control voltage is constant, effectively fixing the frequency.

4.5. Amplitude control and output driver

The pulse amplitude is controlled by an 8-bit command as shown in fig. 3. This means that it can be selected to one of 255 current levels ranging from $0-2mA$. The length of the pulse is also selected by an 8-bit command to be $1-255\mu s$. Each pulse is followed by a charge balancing pulse with an amplitude of $128\mu A$ and an appropriate length to achieve the charge balance.

A very simple way to achieve charge balance would be to use an ac-coupling (series capacitor) to the contacting electrodes. However, this would require an external capacitor for each of the output channels which is undesirable because of the space constraints of the stimulator. An alternative is to calculate the charge in the stimulation pulse and derive the pulse length of the charge balancing pulse from this calculation. This can be done in the digital domain from the information received about the pulse amplitude and length, but the calculation would require a good deal of (area consuming) logic and the charge balancing pulse would be quantized
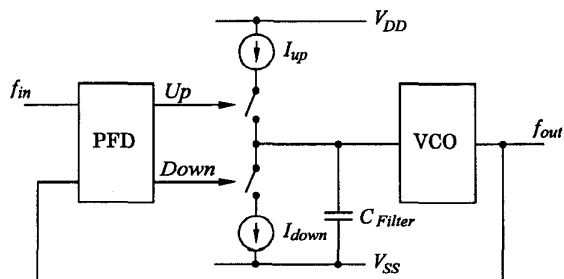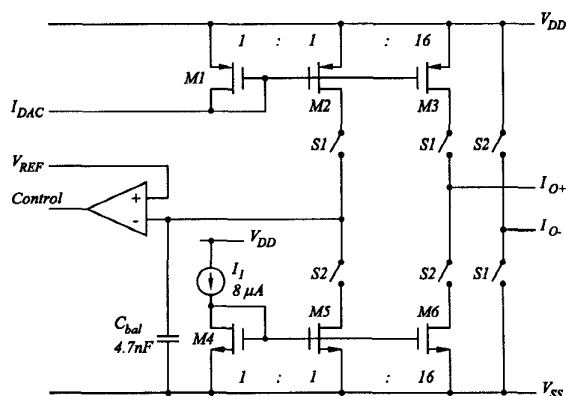
Figure 6. The phase-locked loop

Figure 7. The output driver stage

in minimum steps of $128\mu A \times 1\mu s$. As an alternative, an analog calculation described below has been selected.

A simplified schematic of an output driver stage is shown in fig. 7. The switches $S1$ are 'on' when the output driver is selected and a pulse is activated. The switches $S2$ are 'on' when a charge balancing pulse is activated. Basically, the primary pulse is generated by the current mirror $M1, M3$. The input current is derived from a digital to analog converter with an output current range of $0-128\mu A$. The current source I_1 is used for the charge balancing pulse. During the output pulse, $M2$ charges the capacitor C_{bal} with a current equal to the output current divided by 16. During the discharge pulse, the capacitor C_{bal} is discharged with the discharge current divided by 16, i.e. $8\mu A$. Thus, charge balance is obtained when the capacitor voltage is returned (by I_{D5}) to its initial, precharged value detected by a comparator. The comparator output is used by the control logic to terminate the switch control signal S_2. In the actual implementation, the current mirrors $M1-M3$ and $M4-M6$ are implemented as cascode current mirrors to improve the accuracy. The charge balancing also depends on the matching in the output current mirrors. The maximum charge delivered by an output pulse is $Q_{max} = t_{max} \times I_{max} = 255\mu s \times 2mA \simeq 0.5\mu C$. With a mismatch on the order of 5% a charge error of about $25nC$ can be expected. This can be compared to the generally accepted levels of charge accumulation of $1-3\mu C/mm^2$ reported in [4] and [5]. The charge balancing capacitor C_{bal} has a value of $4.7nF$ which is certainly not integratable. However, a single external capacitor can be used for all the output channels.

The digital to analog converter must provide a digitally controllable current output in the range $0-128\mu A$. It is implemented as an array of equally sized current sources controlled by the digital command word.

4.6. Digital control

The digital control logic comprises all the logic needed to decode the command word shown in fig. 3 to the appropriate inputs to the analog to digital converter, the output channel decoder, and the timing of the output pulse. Also, the digital control performs the CRC-8 check of the command word. This reduces the risk of issuing false stimulation pulses. No error correction has been implemented
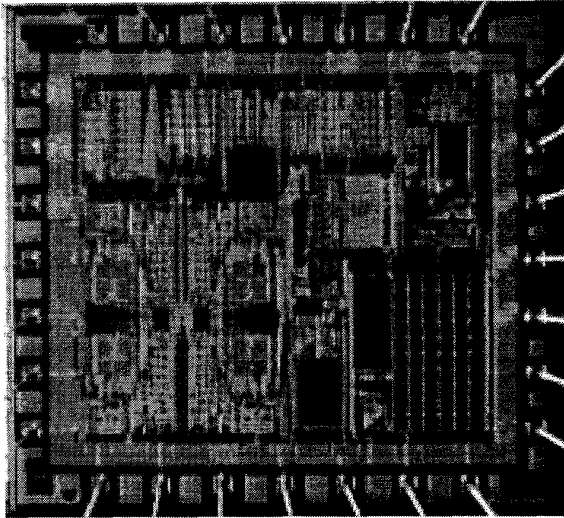
Figure 8. Chip photo of the stimulator chip

since the application would normally allow a simple retriggering of the stimulation pulses if a pulse was missing due to a transmission error.

5. EXPERIMENTAL RESULTS

Prototype chips have been fabricated in MIETEC's $2\mu m$ CMOS technology. The process has been selected primarily because of its capability to handle the rather large supply voltage. The total chip size is $3mm \times 4mm$. For evaluation purposes the chip has been encapsulated in a standard dual-in-line package. A chip photo is shown in fig. 8. For devices to be used for implantation an alternative encapsulation and mounting together with the discrete devices must be employed.

The chip has been tested with respect to some critical parameters and with respect to functionality. All the circuit blocks have been found to work satisfactorily. The carrier recovery and envelope detection work as predicted. The PLL is able to lock on the carrier and hold its frequency when the carrier is off with a decay of less than $0.1\%/s$. The digital supply voltage has been measured to be within a tolerance of 10%. The total supply current is about $600\mu A$ which is close to the simulated value. The charge balanc-
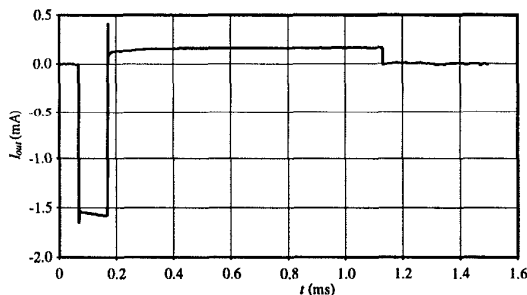

Figure 9. Measured output current pulse from the stimulator

ing circuit shows a mismatch of 5–10% of the stimulation charge, slightly more than expected, but still acceptable.

Functionally, the chip works as expected. Fig. 9 shows the waveform of the output current when the output has been programmed to a duration of $100\mu s$ and an amplitude of $1.5mA$. The output has been measured as the voltage across a $2k\Omega$ load resistor. The charge balancing pulse following the stimulation pulse is clearly seen.

6. CONCLUSION

A prototype chip for a neural stimulator has been designed and fabricated. The chip comprises all the signal processing functions required for the application. A novel method for charge balancing of the stimulation pulses has been developed. Initial measurements show full functionality of the chip and specifications well within the tolerances expected. The next step will be to employ the chip in experiments with functional electrical stimulation of rabbits in order validate that the performance specification of the chip are adequate for the planned applications.

Acknowledgement

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