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An Improved Harmonics Mitigation Scheme for a Modular Multilevel Converter

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ABSTRACT Modular Multilevel Converters (MMC) are gaining importance because of their flexible structure, re-configurable property, and simplicity of operation. The operation of MMC at a low-switching frequency (LSF) helps in enhancing the performance of the converter. This paper proposes an improved harmonics mitigation scheme for a Multilevel DC-Link Inverter (MLDCLI), which is a variant of MMC. The proposed scheme is a modified version of the conventional Nearest Level Modulation (NLM) scheme, termed as modified Nearest Level Modulation (mNLM) Scheme. The proposed scheme is effective compared to NLM because of the choice of the switching angles obtained by the use of the algorithm proposed. The MLDCLI topology is operated for twelve different configurations, and mNLM is implemented on all the configurations. Using MATLAB software, the simulation results are validated, and the same is extended to a hardware prototype. The simulation and experimental results of NLM and mNLM schemes are compared. The effectiveness of the proposed scheme is evident by the reduced voltage THD, increased rms voltage, increased rms current, and increased output power.

INDEX TERMS Modular multilevel converters, DC-AC power converters, pulse width modulation converters, power conversion harmonics, nearest level modulation, total harmonics distortion.

I. INTRODUCTION

A multilevel inverter (MLI) is a combination of power semiconductor switches and dc voltage sources to generate ac output voltage in a stepped waveform. The proper commutation of the power semiconductor switches helps in adding the dc voltage sources to produce the ac output. The presence of multiple switches also helps to reduce voltage sharing among the switches to generate high power output [1], [2]. These converters can synthesize the output waveform with reduced harmonics content. Hence, they are used to attain high voltage levels in high power conversion [3], [4]. The other applications of MLI involve integration with renewable sources, use in motor drives, and power systems [5]–[9].

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The most common and conventional multilevel inverter topologies are neutral point clamped inverter (NPC), flying capacitor clamped inverter (FC), and cascaded h-bridge inverter (CHB) [10]–[14]. In recent years many new topologies have evolved, which can generate a higher number of levels with a reduced number of switches than the conventional inverter topologies [15]–[18]. This has given rise to a new classification of MLI based on the symmetry of the input dc sources of the MLI [19]. An MLI with equal magnitude dc sources is classified as symmetrical MLI. On the other hand, an asymmetrical MLI has an unequal magnitude of dc sources. An asymmetrical MLI is preferred over the symmetrical MLI for numerous advantages such as reduced THD, improved ac waveshape, higher output power etc, [20], [21].

Modular Multilevel Converters (MMC) are a variant of MLIs which carry a modular and reconfigurable structure. Multilevel DC-Link inverters (MLDCLI) form a very

TABLE 1. Advantages of low-switching frequency over high-switching frequency modulation schemes.

Sl.	Performance Parameters	HSF Schemes ⊗	LSF Schemes ✓
1	Device switching stress	high	low
2	Device switching losses	high	low
3	Device cooling requirements	high	low
4	Device manufacturing cost	high	low
5	Device utilization	low	high
6	Converter efficiency	low	high

significant topology among the existing MMC topologies. The MLDCLI is a combination of cascaded half-bridge cells as well as a full-bridge inverter. The cascaded half-bridge cells operate to increase the levels at the output of the MMC, whereas the full-bridge plays the part of generating the negative polarity of the ac output. The striking feature of the MLDCLI is the reduced switch count as compared to the conventional MLI topologies [22]. The MLDCLI can also operate under symmetrical as well as asymmetrical configurations and applications includes renewable energy sources and battery electric vehicles [23], [24].

Even though numerous research is carried on the MLI topologies by academicians and industrialists, the efficient operation of MLI also depends on the way of operation of the switches. Hence, there are many modulation schemes used and developed to operate an MLI efficiently [25]–[30]. For the sake of simplicity, modulation schemes may be classified into high-switching frequency (HSF) and low-switching frequency (LSF) modulation schemes. In an HSF scheme, the switches are operated in several kHz to reduce the harmonics at the output [31]–[34]. The switches in LSF modulation schemes are operated at less than 1kHz [4], [35], [36].

Switching losses in a power semiconductor switch is a vital parameter in medium-voltage high-power applications. When switching loss is reduced, it leads to a reduction in the manufacturing and operating costs of a converter. It also helps in better device utilization, higher converter efficiency, and reduced cooling requirements [37]–[39]. Hence, LSF modulation schemes are often most preferred to HSF modulation schemes. The advantages of LSF schemes over HSF are tabulated in Table 1.

NLM falls under the category of LSF schemes. The switching frequency of the power semiconductor switches depends on the line frequency of the MLI. This paper proposes a modified version of the NLM to reduce the THD content at the ac output of the MLI. The NLM scheme has outstanding advantages over the other LSF modulation schemes. The drawbacks of all the LSF modulation schemes and the advantages of NLM scheme are discussed a follows:

1) Equal-Phase Method (EPM) and Half-Equal-Phase Method (HEPM):
   ⊗ The EPM and HEPM schemes carry equal duty cycles and, hence, they yield a very high voltage and current THD.
   ⊗ Since the THD is very high, it reduces the output rms voltage and rms current. This, in turn, offers a poor power conversion efficiency, and hence, they are not a recommended PWM scheme.
2) Selective Harmonics Elimination (SHE):
   ⊗ SHE is a useful scheme for the elimination of the lower order harmonics, but it comes at the cost of increased higher order harmonics [40].
   ⊗ Any improvement in the SHE scheme requires an increase in the switching frequency which is undesirable.
   ⊗ The SHE scheme is also highly dependent on the modulation index, and hence, for getting the maximum efficiency of the SHE scheme, it is important to calculate the exact modulation index.
3) Space Vector Control (SVC):
   ⊗ For a lower number of MLI levels, the working principles of SVC and NLM are almost the same. However, when the MLI levels increases, the SVC becomes increasingly complex [37].
   ⊗ The SVC scheme is ideal for use when a particular switching pattern is necessary with respect to varying input voltages.
4) Nearest Level Modulation (NLM):
   ✓ The striking feature of NLM is the simplicity in its execution. A simple equation is sufficient to calculate the switching angles enabling ease of execution [40].
   ✓ With the NLM equation, it is very easy to extend it to any number of MLI levels.
   ✓ There is enough scope for improving NLM without increasing the switching frequency.

Hence, it can be observed that the NLM scheme offers good advantages over its counterpart LSF schemes. This paper proposes an improved version of the NLM scheme by following an algorithm to obtain a new set of switching angles. The new set of switching angles helps in improving the performance parameters of the inverters such as THD, rms voltage, rms current, and output power.

II. MULTILEVEL DC-LINK INVERTER

Figure 1 shows the circuit diagram of a MLDCLI. It consists of four dc sources and twelve switches. Four of the switches act as an h-bridge, and the remaining eight switches are part of cascaded half-bridge cells. A single half-bridge cell consists of two switches. Thus, four such half-bridge cells are cascaded to generate various levels. The operation of the switches in the half-bridge cell determines whether the associated dc sources should be added in the circuit or not. The switches in the half-bridge operate in a toggle fashion.

When the pair of switches S_1-S_2 are considered, turning on switch S_2 and turning off switch S_1 provides a current path which add the voltage source V_{dc1} to the main circuit.

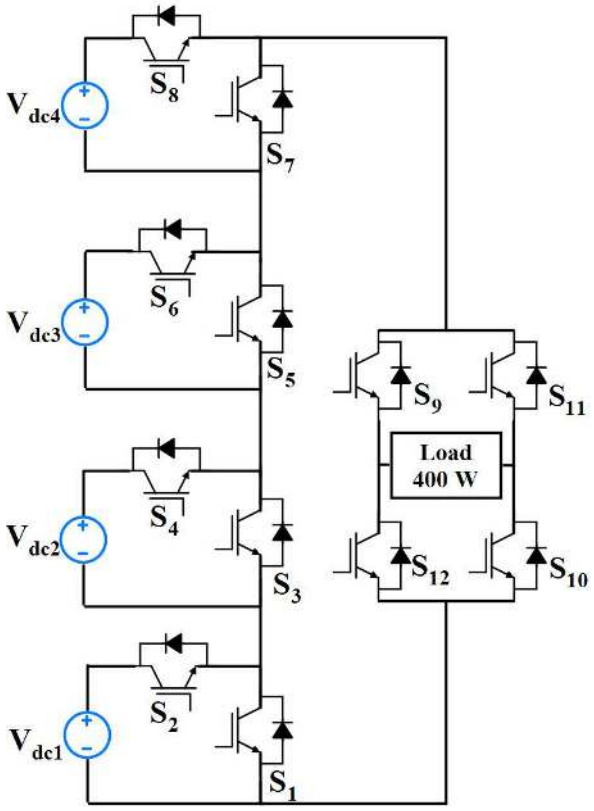

FIGURE 1. Circuit of multilevel DC-Link inverter.

However, turning on switch S_1 and turning off switch S_2 disassociates V_{dc1}. The other switch pairs S_3-S_4, S_5-S_6 and S_7-S_8 operate similarly to associate or disassociate with their respective dc voltage sources. The switch pair S_9-S_{10} on operation will provide the positive half cycle of the ac output. The negative half of the ac output is provided by the switch pair $S_{11}-S_{12}$. Hence, for a single cycle, the switching frequency of the half-bridge cells is twice the switching frequency of the h-bridge. The h-bridge is operated at a switching frequency of 50 Hz to generate a 50 Hz ac output.

A. SYMMETRIC CONFIGURATION

In the symmetric configuration, all the voltage sources carry equal voltage magnitude. This leads to four possible voltage levels i.e, V_{dc1}, $V_{dc1} + V_{dc2}$, $V_{dc1} + V_{dc2} + V_{dc3}$ and $V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4}$ [41]. Hence, a 9-level output is generated. This is the first configuration of the twelve possible configurations presented in this paper. This symmetrical configuration can be extended to any number of levels using the following equations.

By adding the number of voltage sources, the MLI levels will increase. The values of all the dc sources are the same, which is shown in equation (1).

$$V_{dc,j} = V_{dc} \quad for\ j = 1, 2, 3, 4 \ldots \tag{1}$$

The number of MLI levels at the output and the number of switches in MLDCLI circuit are related as equation (2).

$$N_{level} = n - 3 \quad for\ n = 6, 8, 10, 12 \ldots . \tag{2}$$

As the number of switches increase, the number of input sources also increases, which is shown in equation (3).

$$N_{source} = \frac{n-4}{2} \quad for\ n = 6, 8, 10, 12 \ldots . \tag{3}$$

B. ASYMMETRIC CONFIGURATION

In the asymmetric configurations, the magnitudes of input dc voltages are unequal. In general, an asymmetrical configuration generates a greater number of levels than symmetrical configurations. This helps in improving the ac output voltage waveform quality and the associated THD. However, with the increase in MLI levels, the number of modes of operation of the MLI increases for a single cycle, which results in an increase in the switching frequency. The switching pattern also increases in complexity with higher MLI levels. Nevertheless, a higher MLI level is always preferred. In this section, there are 11 asymmetrical configurations considered to generate levels starting from 11-level to 31-level.

In configuration 2, the 4^{th} dc voltage source is twice in voltage magnitude of the other three voltage sources generating an 11-level output. Configuration 3 carries input dc voltage sources of ratio 1:1:2:2 and generates 13-level. To generate a 15-level, the 2^{nd}, 3^{rd} and 4^{th} are chosen with a twice the magnitude of the 1^{st} input dc voltage source. The 17-level and 19-level MLI are generated with the input dc voltage sources of 1:2:2:3 and 1:2:2:4, respectively. A natural number sequence is followed by the dc voltage source to generate 21-level MLI output. To generate a 23-level MLI output, a dc voltage ratio of 1:2:3:5 is used, which resembles a Fibonacci series. With the input dc voltage sources of 1:2:3:6, 25-level MLI is generated. 27-level and 29-level MLI are generated using the dc voltage source ratios of 1:2:4:6 and 1:2:4:7, respectively. A binary sequence dc voltage source is employed to generate 31-level. Table 2 shows the consolidated modes of operations for all the configurations.

III. CONVENTIONAL AND PROPOSED MODULATION SCHEME

A. NEAREST LEVEL MODULATION SCHEME

Figure 2 presents the graphical diagram of the NLM scheme. A single cycle is shown where a 7-level MLI output is compared with a sinusoidal waveform. Besides it, a quarter cycle of the full cycle is shown, which provides deep insight into the working of the conventional scheme. For the ease of understanding, the sinusoidal waveform cutting the rising edge of the MLI level can be divided into two parts. The upper part is called Upper sub-level (USL), while the lower part is called the Lower sub-level (LSL). For NLM scheme the, the magnitude of USL and LSL are the same. This is applicable to all the rising edges of the MLI levels. With the

TABLE 2. Various configurations of operation of MLDCLI.

Configuration	No. of Levels	Ratio of DC Sources	Possible Voltage Combinations
1	9	1:1:1:1 (39 V, 39 V, 39 V, 39 V)	V_{dc1}, V_{dc1}+V_{dc2}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
2	11	1:1:1:2 (31 V, 31 V, 31 V, 62 V)	V_{dc1}, V_{dc1}+V_{dc2}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
3	13	1:1:2:2 (26 V, 26 V, 52 V, 52 V)	V_{dc1}, V_{dc1}+V_{dc2}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
4	15	1:2:2:2 (22 V, 44 V, 44 V, 44 V)	V_{dc1}, V_{dc2},V_{dc1}+V_{dc2}, V_{dc2}+V_{dc3},V_{dc1}+V_{dc2}+V_{dc3}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
5	17	1:2:2:3 (19 V, 38 V, 38 V, 58 V)	V_{dc1}, V_{dc2}, V_{dc1}+V_{dc2}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
6	19	1:2:2:4 (17 V, 34 V, 34 V, 68 V)	V_{dc1}, V_{dc2}, V_{dc1}+V_{dc2}, V_{dc2}+V_{dc3},V_{dc1}+V_{dc2}+V_{dc3}, V_{dc2}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
7	21	1:2:3:4 (15.5 V, 31 V, 46.5 V, 62 V)	V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc1}+V_{dc4}, V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
8	23	1:2:3:5 (14 V, 28 V, 42 V, 70 V)	V_{dc1}, V_{dc2}, V_{dc3}, V_{dc1}+V_{dc3}, V_{dc4},V_{dc1}+V_{dc4}, V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4},V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
9	25	1:2:3:6 (13 V, 26 V, 39 V, 78 V)	V_{dc1}, V_{dc2}, V_{dc3}, V_{dc1}+V_{dc3}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc1}+V_{dc4}, V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
10	27	1:2:4:6 (12 V, 24 V, 48 V, 72 V)	V_{dc1}, V_{dc2},V_{dc1}+V_{dc2}, V_{dc3}, V_{dc1}+V_{dc3}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc2}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
11	29	1:2:4:7 (11 V, 22 V, 44 V, 77 V)	V_{dc1}, V_{dc2},V_{dc1}+V_{dc2}, V_{dc3}, V_{dc1}+V_{dc3}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc1}+V_{dc4}, V_{dc2}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}
12	31	1:2:4:8 (10 V, 21 V, 41 V, 83 V)	V_{dc1}, V_{dc2},V_{dc1}+V_{dc2}, V_{dc3}, V_{dc1}+V_{dc3}, V_{dc2}+V_{dc3}, V_{dc1}+V_{dc2}+V_{dc3}, V_{dc4}, V_{dc1}+V_{dc4}, V_{dc2}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc4}, V_{dc3}+V_{dc4}, V_{dc1}+V_{dc3}+V_{dc4}, V_{dc2}+V_{dc3}+V_{dc4}, V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}

help of equation (4), the firing angles α_i are calculated [39].

$$\alpha_i = sin^{-1}(\frac{i-0.5}{n}); \quad for\ i = 0, 1, 2, 3, \ldots, n \tag{4}$$

B. MODIFIED NEAREST LEVEL MODULATION SCHEME

An improved low switching frequency modulation scheme needs the THD to be calculated properly. Then the switching angles are substituted in the THD equation to find whether the newer set is increasing or decreasing the THD. Hence, equation (5) is used to calculate the THD [42].

$$THD = \frac{\sqrt{\frac{\pi^2 n^2}{8} - \frac{\pi}{4}\sum_{i=0}^{n-1}(2i+1)\alpha_{i+1} - (\sum_{i=1}^{n} cos(\alpha_i))^2}}{\sum_{i=1}^{n} cos(\alpha_i)} \tag{5}$$

A nine-level configuration is taken up for the study of the algorithm of mNLM. The nine-level configuration has four switching angles. The algorithm begins by calculating the THD with the initial set of switching angles. The first switching angle (α_1) was reduced by 1 degree, keeping α_2, α_3 and α_4 unchanged. The revised THD was calculated with these updated switching angles. When the revised THD was found less than the previous one, the first switching angle (α_1) was further reduced by 1 degree. This led to the second iteration, and the revised THD was compared with the previous THD. This iteration process continued until there was no further reduction in the THD content when compared to the previous one. When the revised THD was greater than the previous one during the first iteration, (α_1) was kept the same, and the second switching angle (α_2) was proceeded with a decrease by 1 degree. With the least THD obtained by varying the first switching angle (α_1) alone, the second switching (α_2) was decreased by 1-degree till

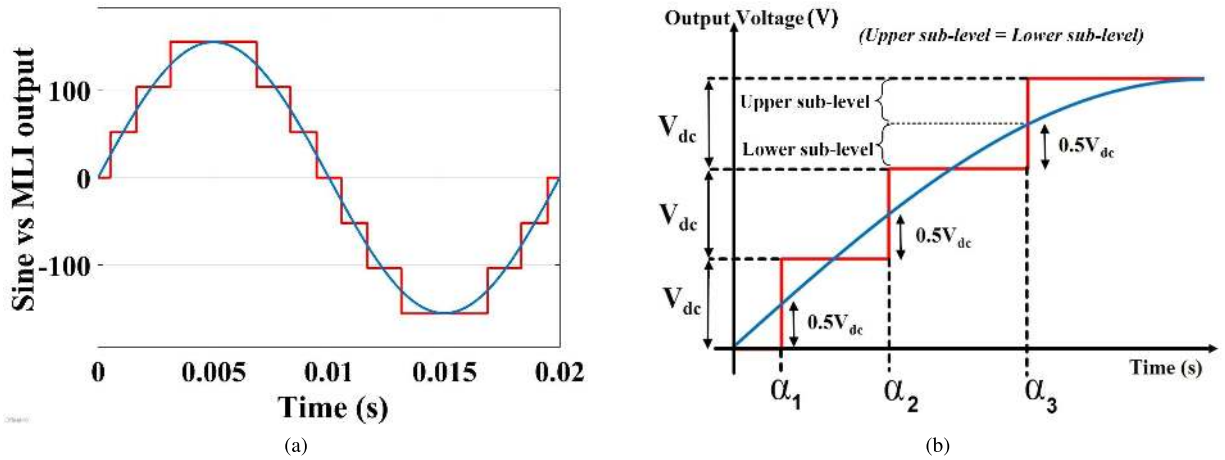

FIGURE 2. NLM scheme (a) Comparison of sine wave and MLI output for a one cycle (b) Quarter cycle of the waveform.

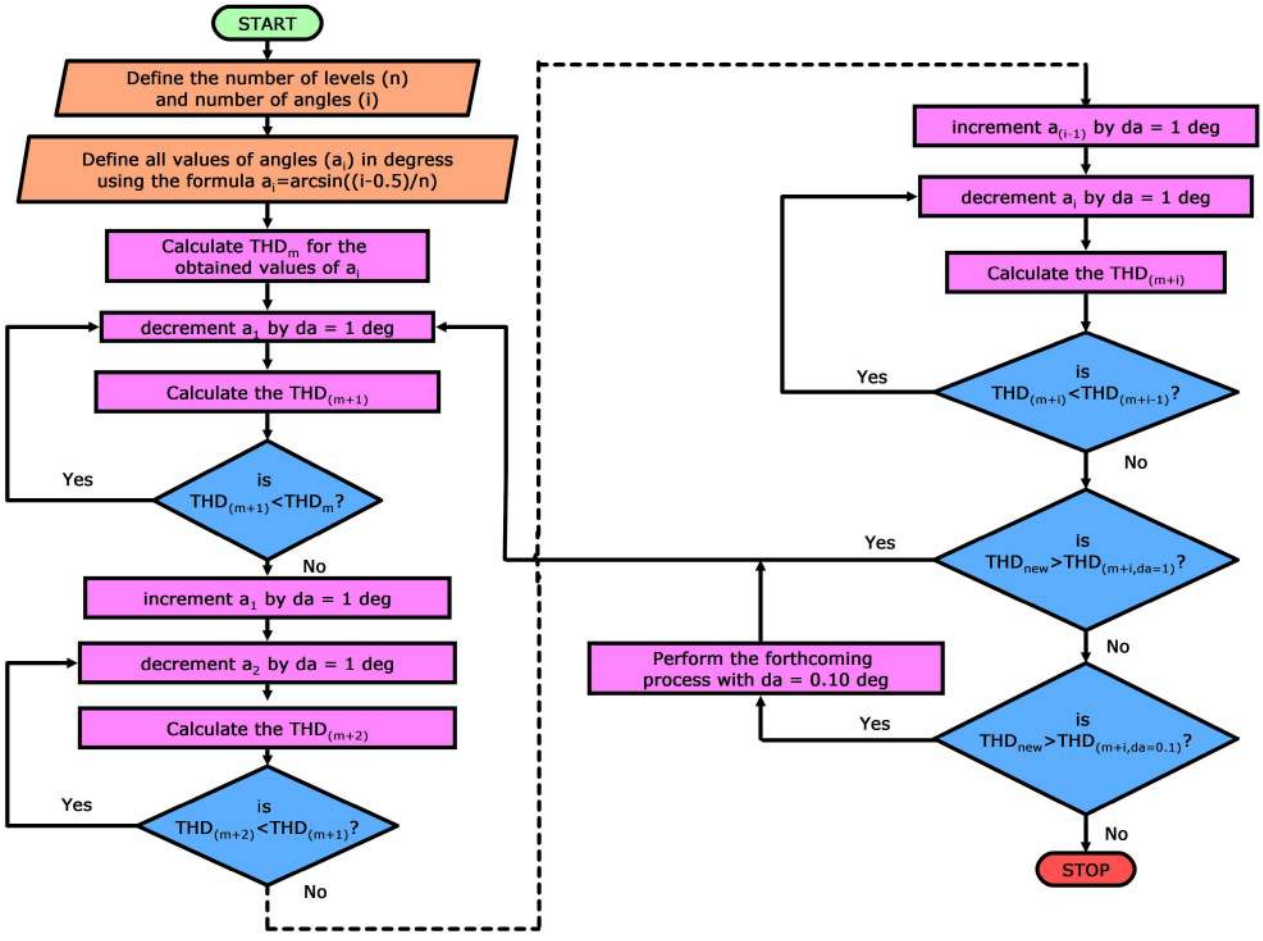

FIGURE 3. Algorithm of modified nearest level modulation scheme.

the least THD was obtained. This process continued for all the switching angles. This constitutes the first cycle. Once the last switching angle (α_4) was varied, and the least THD obtained, the entire process starting from (α_1) was again repeated for the same 1-degree variation. This formed the second cycle. The cycles are repeated until the least THD content was obtained. The process undergone so far was again repeated for a change in the switching angle α_1, α_2, α_3, and α_4 value of 0.10 degree. This helped to fine-tune the angles.

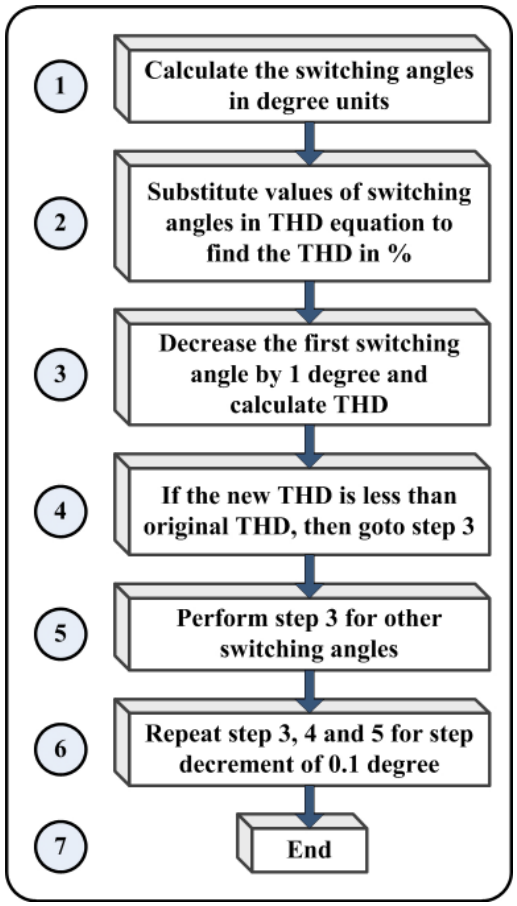

FIGURE 4. Simplified block diagram of mNLM scheme.

Based on the number of switching angles (α_i), the number of cycles required to complete the mNLM algorithm varies. The number of cycles required to complete the algorithm increases as the number of switching angles increases. Figure 3 is the flowchart of the mNLM algorithm. Table 3 shows the significant results for the nine-level configuration. The difference in THD among the various iterations are seen from the iteration number 1, 10, 16, 25, 37, and 42. The difference in THD for the nine-level configuration is due to the equation 5, which takes in to account the sinusoidal nature of MLI output. Table 3 leads to the observation of any absence of any decrease in the THD contents following a decrease in α_1, and thereby maintained at the same level, between iterations 1 and 10. However, there was a decrease in THD following a decrease of α_2. There was no further decrease in the THD following a continued decrease in the α_2 after the 10th iteration till the 25th iteration. Hence, the value of α_3 was decreased to enable observation of the change in THD content. The process continues by varying the angle of α_4.

An interesting observation to note from Table 3 is a significant impact on the THD content seen as a result of variations in angle α_4. A significant variation was therefore seen in α_4 among the switching angles. The switching angle α_1 was also seen as having the least impact among the switching angles on the THD content. Table 3 leads to the inference of 42 iterations being taken for arriving at the least THD content of 8.9025%, which provides the final switching angles. Iterations 1, 10, and 16 were done with an accuracy of 1 degree whereas, iterations 25, 37, and 42 were done with an accuracy of 0.10 degree. A similar attempt can be made by the above-explained process for the other asymmetric configurations. While implementing mNLM for all the symmetric and asymmetric configurations, it is necessary to redefine the number of levels (n) and the number of angles (i) for each configuration. This is because the number of levels is different for each configuration, and so is the number of angles. Hence, the number of iterations increases with a higher number of switching angles. The algorithm is then repeated from the start to the end. The entire process is an offline implementation where equation 4 and equation 5 are used in the form of a simple MATLAB code. The switching angles are revised to obtain the final mNLM switching angles and programmed into the microcontroller before operating the MLDCLI. The MLDCLI circuits run on the pre-programmed microcontroller program and do not require any further monitoring.

TABLE 3. Modified NLM (Results of significant iterations).

Iteration	1	10	16	25	37	42
α_1 (deg)	7.18	7.18	7.18	6.78	6.78	6.78
α_2 (deg)	22.02	21.02	21.02	21.02	20.82	20.82
α_3 (deg)	38.68	37.68	36.68	36.68	36.28	36.28
α_4 (deg)	61.04	57.04	56.04	56.04	55.74	55.84
THD(%)	9.3627	8.9813	8.9181	8.9109	8.9028	8.9025

IV. RESULTS AND ANALYSIS

The simulation output is shown from Figure 5 to Figure 8. The MLDCLI was operated to generate 110 V_{rms}, 50 Hz and 400 W output. The results of four critical configurations are shown i.e., 9-level, 17-level, 23-level and 31-level.

Figure 5 shows the V, and I output for 9-level configuration using NLM and mNLM scheme. It can be observed that the THD generated using NLM scheme was 8.35% while it was 7.67% using mNLM scheme. The V and I waveform for the 17-level configuration is shown in Figure 6 along with the voltage THD. The proposed scheme was found to generate a lesser THD of 3.47%. The 23-level configuration V and I output is shown in Figure 7. The NLM and mNLM schemes were found to generate a THD of 2.07% and 1.87%, respectively. The last configuration is a 31-level output, where the waveform is observed to be nearly sinusoidal shown in Figure 8. The THD associated with NLM and mNLM schemes is also less. Figure 9 represents the performance comparison of various inverter parameters such as V_{THD}, V_{RMS}, I_{RMS}, Output Power from 9-level to 31-level. The graph voltage THD of mNLM is found to be tracing a parallel path to that of NLM with a good margin of difference. Similarly,

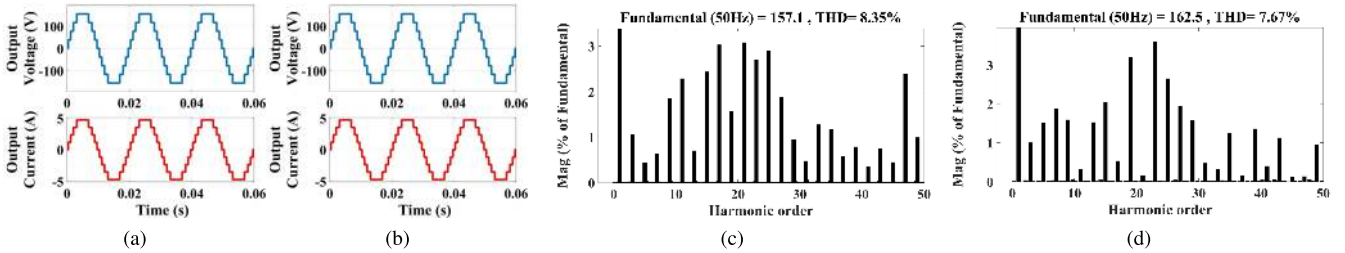

FIGURE 5. Simulation output using 9-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

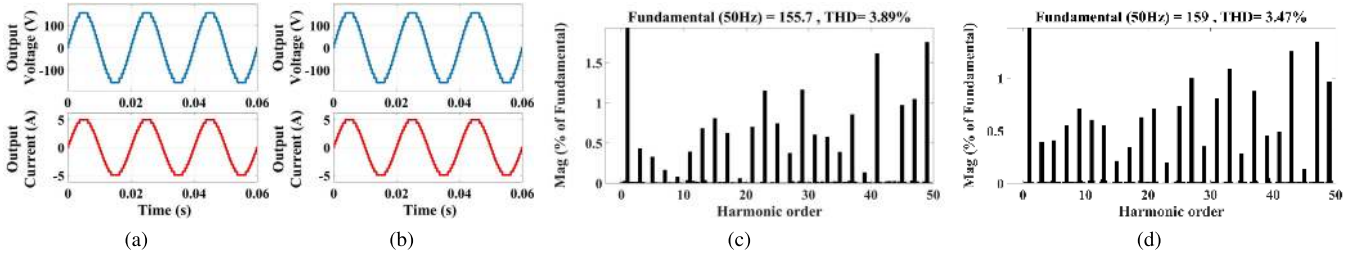

FIGURE 6. Simulation output using 17-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

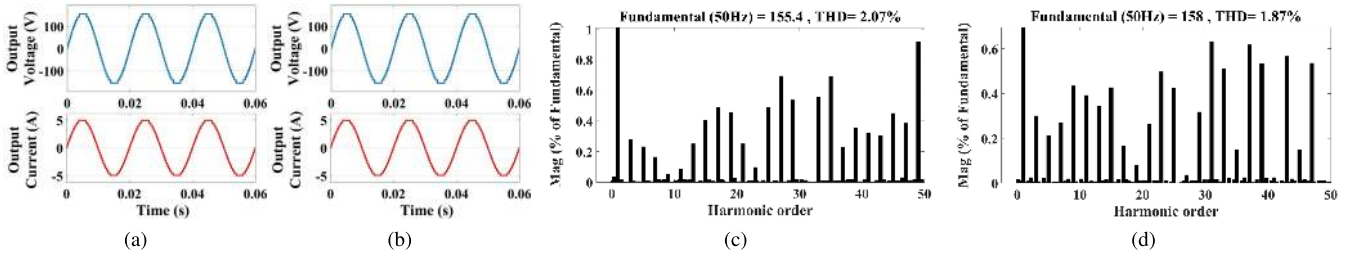

FIGURE 7. Simulation output using 23-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

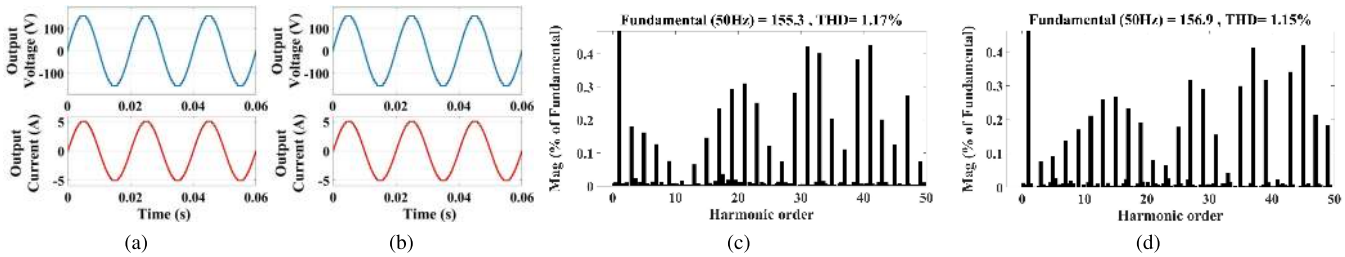

FIGURE 8. Simulation output using 31-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

the rms voltage and rms current had a difference of range between 1.5 V to 4 V and 0.10 A, respectively, between NLM and mNLM scheme. The output power is the product of voltage and current had shown very good improvement by the use of the proposed modulation scheme over the conventional modulation scheme. Thus, it was concluded from the comparison that the proposed scheme is performed better than the conventional scheme in all the important inverter parameters.

The experimental setup is shown in Figure 15, where the entire setup is demonstrated, which was carried out at the laboratory. The experimental results were carried out using four regulated power supplies; the main MLDCLI circuited fabricated on a PCB with twelve H15R1203 IGBTs,

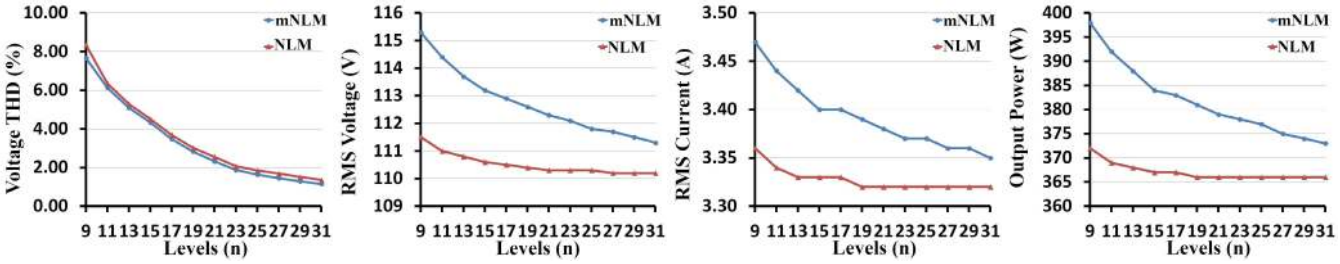

FIGURE 9. Comparison of simulated NLM and mNLM outputs (a) V_{THD} (b) V_{RMS} (c) I_{RMS} (d) Output power.

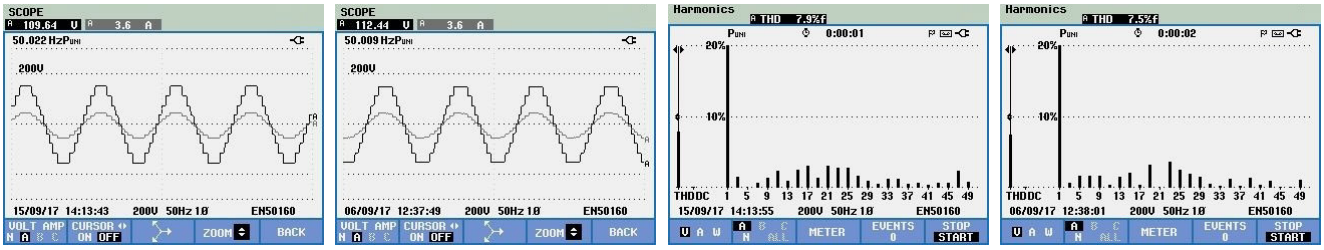

FIGURE 10. Experimental output using 9-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

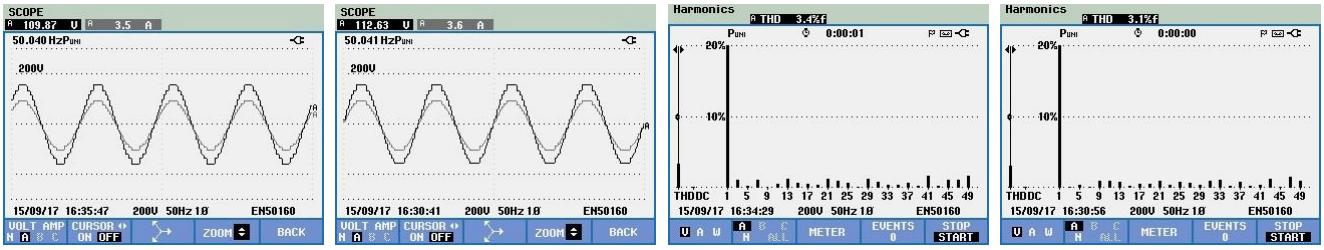

FIGURE 11. Experimental output using 17-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

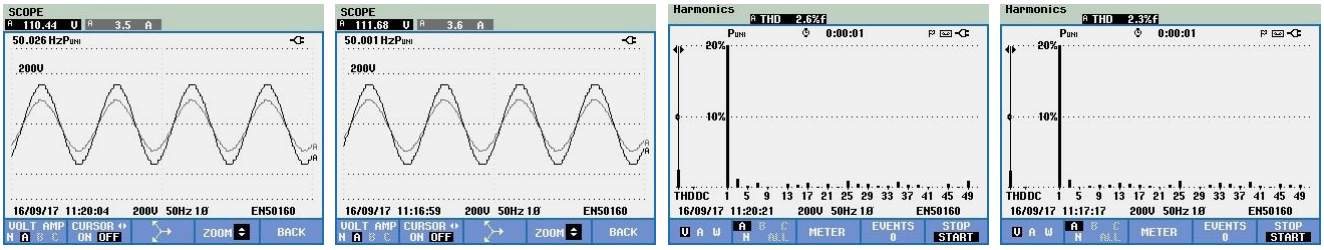

FIGURE 12. Experimental output using 23-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

AVR Atmega32 microcontroller to generate the gate pulses, TLP250 as driver IC, a rheostat as a resistive load and Fluke435b power quality analyzer to measure the THD. The microcontroller was programmed using a USBasp programmer, and Fluke 435 power quality analyzer provides a precise THD. Figure 10 to Figure 13 shows the experimental results of the four critical configurations. The experimental results were found to be similar to that of simulation results.

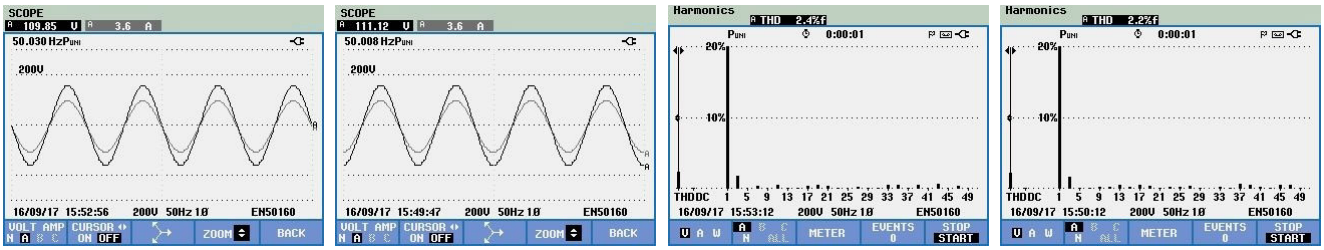

FIGURE 13. Experimental output using 31-level configuration (a) NLM V & I waveforms (b) mNLM V & I waveforms (c) THD of voltage output using NLM (d) THD of voltage output using mNLM.

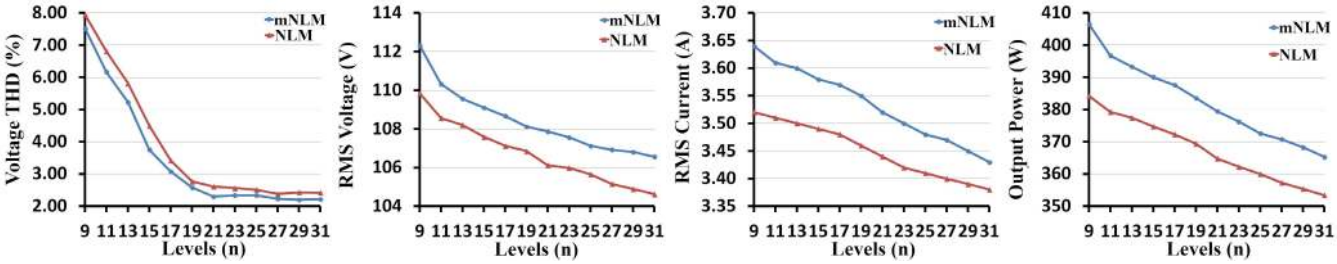

FIGURE 14. Comparison of experimental NLM and mNLM outputs (a) V_{THD} (b) V_{RMS} (c) I_{RMS} (d) Output power.

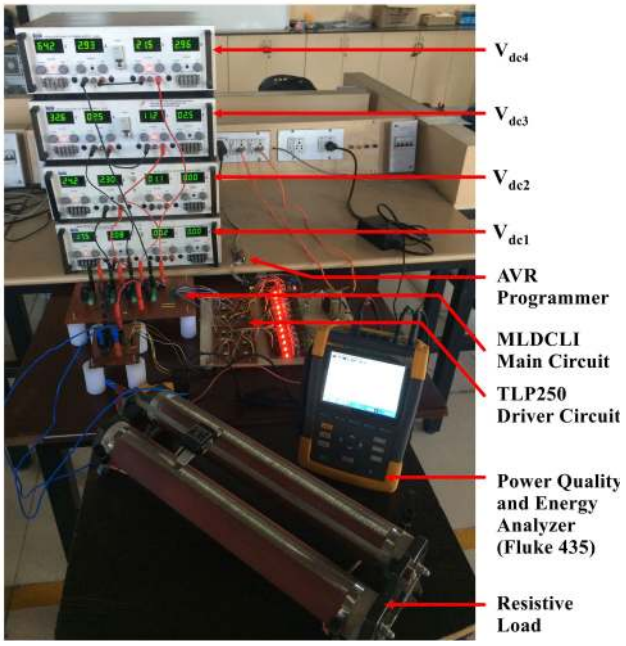

FIGURE 15. Complete hardware setup.

The experimental results confirm that the mNLM scheme is superior to the NLM scheme in all the inverter parameters. The comparison of experimental results for all the configurations is shown in Figure 14. The interesting observation from the experimental results is that the reduction in THD at higher MLI levels is large compared to that of the simulation results. It is also noted that with an increase in the number of levels, the output voltage and current reduced slightly on account of a slightly higher voltage drop across the switches [32]. The same can be observed for the special application of MLI, such as railway transportation electrification [34]. Hence, the mNLM is highly suitable to improve the experimental performance of MMCs.

Table 4 presents the THD generated by some of the recent works using NLM for a 9-level configuration. The proposed mNLM scheme generated 8.35% THD, whereas the NLM in

TABLE 4. Comparison of THD using mNLM for 9-level configuration (8.35%) with other recent references on NLM.

Sl.	Reference	THD as per the Reference
1	[43]	9.27%
2	[44]	9.12%
3	[45]	9.32%

TABLE 5. Simulation and experimental results of implementing mNLM for 9-level symmetric configuration on RL load.

Inverter Parameters	Simulation Results		Experimental Results	
	NLM	mNLM	NLM	mNLM
Voltage THD (%)	8.57	7.89	8.3	7.9
Current THD (%)	1.81	1.28	1.9	1.4
RMS Voltage (V)	111.5	115.3	107.44	111.28
RMS Current (A)	3.39	3.50	3.5	3.6
Output Power (W)	332	355	330	352

TABLE 6. Hardware parameters of MLDCLI topology.

1	Output Voltage	110 V_{rms}
2	Output Current	3.6 A_{rms}
3	Output Power	400 W
4	Output ac frequency	50 Hz
5	DC sources	Aplab (64 V / 5 A, 4 nos)
6	IGBT	H15R1203 (1200 V / 30 A, 12 nos)
7	Opto-isolator	TLP250 (12 nos)
8	Controller	AVR Atmega32 Microcontroller
9	Loading Rheostat	29 ohms / 5 A
10	Inductive Load	50 mH / 5 A
11	Power Quality Analyzer	Fluke 435b

other research work had generated a higher THD. The simulation and experimental results of the proposed modulation scheme on the RL load are presented in Table 5. Table 6 consolidated the hardware parameters for carrying out the experiment on MLDCLI topology.

V. CONCLUSION

This paper has proposed a modified Nearest Level Modulation scheme for a Multilevel DC-Link Inverter, which is a variant of MMC. The proposed scheme is implemented for twelve different configurations, from 9-level to 31-level in the MLDCLI. The simulation is carried out using the MATLAB Simulink 2015b version, and a hardware prototype of the same is presented. To assess the effectiveness of the proposed modulation scheme, four different inverter output parameters are taken. The analysis is carried out for all the MLDCLI configurations. From the analysis carried out for all the parameters, it is found that the voltage THD has decreased to a very good extent. On the other hand, the output rms voltage, output rms current, and output power are also found to have increased. A promising application of mNLM is to integrate with the renewable energy sources for fundamental switching frequency modulation.

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