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An Improved Measurement Matrix Generator for Compressed Sensing of ECG Signals

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Abstract: Compressed sensing (CS) is being widely used to compress and reconstruct data for processing electrocardiogram (ECG) signals obtained through Wireless Body Area Networks. However, the conventional measurement matrix generator and compression computations for CS are in parallel, resulting in significant power consumption and a large area. This paper proposes a serial measurement matrix generator, which reduces the clock frequencies by using linear feedback shift registers and latches. A CS circuit for ECG signals processing based on the proposed measurement matrix generator is proposed and implemented in a SMIC 55 nm CMOS process. The experimental results show that the power consumption is only 1.690 μW at 1.2 V, and the chip area is 0.608 mm^2, which has obvious advantages over the traditional parallel architecture. The reconstruction results show that the Percentage Root-mean-square Difference is 1.32%, which means that the design meets the basic clinical requirements.

Keywords: compressed sensing; wireless body area networks; electrocardiogram; measurement matrix generator

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1. Introduction

Cardiovascular disease is a common disease that seriously threatens human health, especially for the elderly. It has the characteristics of high morbidity, high disability and high mortality. According to statistics, cardiovascular disease currently accounts for about one-third of the global death toll [1–3]. Clinically, long-term and real-time monitoring of electrocardiogram (ECG) signals can effectively assist doctors in diagnosing and treating patients; thus, reducing the aggravation or death due to negligence or untimely treatment [4,5]. Therefore, the research and processing of biological signals are crucial to human health. Wireless Body Area Networks (WBANs) have been widely used in bioelectrical signal monitoring because of the advantages of portability, comfort, and security. Nevertheless, the implementation of WBANs still faces many challenges such as high power consumption and large area [6–8]. Data transmission occupies most of the total power consumption in WBANs, and the power consumption is positively correlated with the amount of data transmitted. Therefore, reducing the amount of data transferred can effectively reduce power consumption. Compressed sensing (CS), including signal compression and reconstruction, has been chosen to process ECG signals to fix the above problems. The signal compression process is relatively simple and consumes less power [9]. The reconstruction process is a little complicated, but it is generally implemented in the data processing center, where there is no limit on power consumption.

Many attempts have been made to apply CS to WBANs in recent years. Nasimi et al. [10] proposed a CS method to remove redundancy completely from frames by using the pseudo-periodic nature of ECG signals, and the technique could achieve superior reconstruction quality. Kumar et al. [11] showed a CS-based compression realized in

a pipelined architecture, and the CS design could achieve high data rates and enable a wake-up implementation to bypass computation for insignificant input samples. Li et al. [12] adopted a Compressed Learning algorithm combined with a one-dimensional Convolutional Neural Network that could directly learn ECG signals in the compression domain without expanded normalization. Liu et al. [13] presented a CS-based encryption scheme, and an ultrahigh efficiency was achieved by leveraging CS for simultaneous data compression and encryption.

Although a great deal of work has been carried out on CS circuit design, there is still some room for further improvement. The measurement matrix for CS is usually generated using a pseudo-random sequence generator, which contains two sets of linear feedback shift registers (LFSRs) [14]. However, the clock frequency of the sequence generator must be equal to that of the matrix sequence, leading to relatively high dynamic power consumption. Moreover, the conventional measurement matrix generator and its corresponding compression are in parallel [11]. A large number of matrix multiplication units make the circuit area quite large.

This paper proposes a serial measurement matrix generator that can produce a matrix at low clock frequencies using LFSRs and latches. A CS circuit for ECG signals is implemented with serial compression calculations based on the proposed measurement matrix generator. This work converts matrix multiplication into matrix addition and reduces the circuit area significantly by reusing an adder unit. The rest of this paper is organized as follows. Section 2 introduces the background of the CS algorithm and a typical digital processing system for ECG signals based on CS. Section 3 proposes an improved measurement matrix generator. Section 4 presents the implementations of the CS circuit based on the proposed measurement matrix generator. Section 5 presents the simulation and reconstruction results, as well as the circuit implementation in a SMIC 55 nm CMOS process. Section 6 discusses the power consumption and area results. Finally, the conclusion is drawn in Section 7.

2. Background

2.1. CS Algorithm

Conventional Nyquist processing requires sampling faster than twice the highest frequency of the signal, resulting in a large number of samples. CS benefits from two fundamental concepts, those being sparsity of the signal and incoherence, so that it can compress the original signal at a sampling rate far lower than the Nyquist rate and reconstruct data accurately [15]. It is critical to CS that the signal is sparse in at least one domain. The incoherence principle states that the measurement matrix used to acquire the signal must be incoherent with the dictionary that represents the signal sparsely. In general, the sparser the signal being measured, the more CS exploits the signal characteristics and the better the reconstruction quality.

CS is mainly divided into two processes, compression and reconstruction [16]. The compression process compresses an N-dimensional input signal, $\mathbf{X} = [x_1, x_2, \ldots, x_N]^{\mathrm{T}}$, into an M-dimensional signal, $\mathbf{Y} = [y_1, y_2, \ldots, y_M]^{\mathrm{T}}$, via an $M \times N$ measurement matrix $\mathbf{\Phi}_{M\times N}$, where $N > M$. The signal $\mathbf{Y}$ can be expressed by [16]:

$$\mathbf{Y} = \mathbf{\Phi X} = \begin{bmatrix} \Phi_{1,1} & \cdots & \Phi_{1,N} \\ \vdots & \ddots & \vdots \\ \Phi_{M,1} & \cdots & \Phi_{M,N} \end{bmatrix} \times \begin{bmatrix} x_1 \\ \vdots \\ x_N \end{bmatrix} = \begin{bmatrix} \Phi_{1,1} \\ \vdots \\ \Phi_{M,1} \end{bmatrix} \times [x_1] + \cdots + \begin{bmatrix} \Phi_{1,N} \\ \vdots \\ \Phi_{M,N} \end{bmatrix} \times [x_N] \quad (1)$$

The reconstruction solves the original data $\mathbf{X}$ based on $\mathbf{Y}$ and $\mathbf{\Phi}$. Since $N > M$, the solution of Equation (1) is under-determined and is usually obtained by solving the convex optimization problem. Typical recovery algorithms used in CS include orthogonal matching pursuit (OMP), compressed sampling matching pursuit (CoSaMP) and Block-Sparse Bayesian Learning (BSBL) algorithm [17]. BSBL algorithm is more stable and efficient for CS-based ECG compressing and performs better than others [18].

The performance of CS algorithms is usually measured by the CF and the Percentage Root-mean-square Difference (PRD) [19] to measure compression efficiency and reconstruction quality, respectively. The PRD of less than 9% is considered acceptable for physician-based diagnosis. In addition, the reconstructed signal quality can be considered "very good" when the PRD is less than 2% [20].

2.2. CS Processing System

Figure 1 shows a typical digital processing system for ECG signals based on CS. ECG signals are sampled, amplified and filtered by the sensor. An analog-to-digital converter (ADC) converts analog signals into digital signals. The compression process is performed in the dashed box, where an N-dimensional input signal $\mathbf{X}$ is compressed into an M-dimensional signal $\mathbf{Y}$. The amount of data transmitted after compression can be reduced remarkably. The reconstruction process is mainly performed on the remote server.

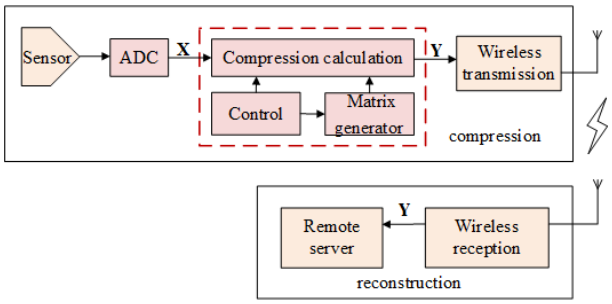


Figure 1. The processing system architecture based on CS.

3. Proposed Measurement Matrix Generator

In order to simplify the compression calculations, the sparse binary matrix [21] is selected as the measurement matrix. Since the matrix elements are either 0 or 1, the compression process only requires addition calculations.

Two sets of LFSRs usually generate the conventional measurement matrix, and the matrix sequence is parallel. This paper proposes a serial measurement matrix generator and uses only one set of LFSRs. First, four sets of pseudo-random binary sequences are generated by the LFSRs. Next, the four sets of sequences are processed to obtain matrix sequences.

The feedback function of the LFSRs can be expressed as a primitive polynomial:

$$h_0 \times 1 + \cdots + h_{n-2} \times x^{n-2} + h_{n-1} \times x^{n-1} + h_n \times x^n,\ M \times N \leq m = 2^n - 1 \tag{2}$$

where h_0 and h_n are always 1, and $h_1, h_2, \ldots$, and h_{n-1} are 0 or 1. The maximum sequence length is m. The primitive polynomial can be written as a transition matrix:

$$\mathbf{T} = \begin{bmatrix} h_1 & h_2 & \cdots & \cdots & \cdots & h_{n-1} & h_n \\ 1 & 0 & \cdots & \cdots & \cdots & 0 & 0 \\ 0 & 1 & 0 & \cdots & \cdots & \cdots & 0 \\ 0 & 0 & 1 & \cdots & \cdots & \cdots & 0 \\ \vdots & & & \ddots & & & \vdots \\ \vdots & & & & \ddots & & \vdots \\ 0 & \cdots & \cdots & \cdots & 0 & 1 & 0 \end{bmatrix}_{n \times n} \tag{3}$$

The connections between the flip-flops in the LFSRs with four outputs are expressed as:

$$\mathbf{W} = \mathrm{mod}(\mathbf{T}\cdot\mathbf{T}\cdot\mathbf{T}\cdot\mathbf{T}, 2) = \begin{bmatrix} w_{1,1} & w_{1,2} & \cdots & \cdots & \cdots & w_{1,n-1} & w_{1,n} \\ \vdots & & & & & & \vdots \\ w_{4,1} & w_{4,1} & \cdots & \cdots & \cdots & w_{4,n-1} & w_{4,n} \\ 1 & 0 & \cdots & \cdots & \cdots & \cdots & 0 \\ 0 & 1 & 0 & & & & \vdots \\ \vdots & & \ddots & & & & \vdots \\ 0 & \cdots & 0 & 1 & 0 & 0 & 0 \end{bmatrix}_{n\times n} \tag{4}$$

where $\cdot$ is matrix multiplication, and mod (**A**, 2) is modulo 2 for each element in matrix **A**.

The proposed measurement matrix generator is shown in Figure 2, where the two vertical dashed lines divide the three clock domains of $f/4$, $f/2$ and f, respectively. The clock frequency f is equal to the rate of data compression. Some of the flip-flops' outputs are fed back to the inputs of the first flip-flop in each group (each row is a group).

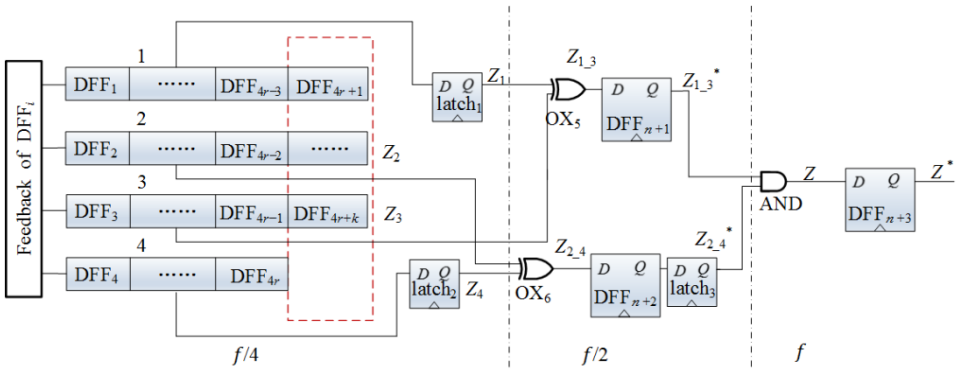


Figure 2. Proposed measurement matrix generator.

The connections of flip-flops in the LFSRs are as follows:

$$\mathrm{DFF}_i/D = (w_{i,1} \times \mathrm{DFF}_1/Q) \oplus (w_{i,2} \times \mathrm{DFF}_2/Q) \oplus \cdots \oplus (w_{i,n} \times \mathrm{DFF}_n/Q) \tag{5}$$

where $(w_{i,n} \times \mathrm{DFF}_n/Q)$ is DFF_n/Q when $w_{i,n}$ is 1, $\oplus$ represents the XOR operation, and $1 \le i \le n$, n is determined by the value of $M \times N$, $r = n/4$, and $k = n\%\,4$ ($r \ge 1$, $1 \le k \le 3$).

The part enclosed in the dashed box in Figure 2 is determined by the value of k. When $k = 1$, the structure contains the flip-flop DFF_{4r+1} only; when $k = 2$, there are two flip-flops, DFF_{4r+1} and DFF_{4r+2}. The values of Z_2 and Z_3, and the inputs of latch_1 and latch_2 are also determined by k:

$$\mathrm{latch}_1/D = \left\{ \begin{array}{c} \mathrm{DFF}_{4r-3}/Q, 1 \le k \le 2 \\ \mathrm{DFF}_{4r+1}/Q, 3 \le k \le 4 \end{array} \right\} \tag{6}$$

$$Z_2 = \left\{ \begin{array}{c} \mathrm{DFF}_{4r-2}/Q, 1 \le k \le 2 \\ \mathrm{DFF}_{4r+2}/Q, 3 \le k \le 4 \end{array} \right\} \tag{7}$$

$$Z_3 = \left\{ \begin{array}{c} \mathrm{DFF}_{4r-1}/Q, 1 \le k \le 2 \\ \mathrm{DFF}_{4r+3}/Q, 3 \le k \le 4 \end{array} \right\} \tag{8}$$

$$\mathrm{latch}_2/D = \left\{ \begin{array}{c} \mathrm{DFF}_{4r-4}/Q, 1 \le k \le 2 \\ \mathrm{DFF}_{4r}/Q, 3 \le k \le 4 \end{array} \right\} \tag{9}$$

Latch_1 delays the output of the first sequence group to produce Z_1, which serves as the input of OX_5 gate together with Z_3. The outputs of the XOR gates OX_5 and OX_6 have double the frequency of their input sequences, as shown in Figure 3. Similarly, the AND

gate increases the frequency of Z. The probability that the sequence Z is 1 is about 1/4 as it is generated by an AND gate.

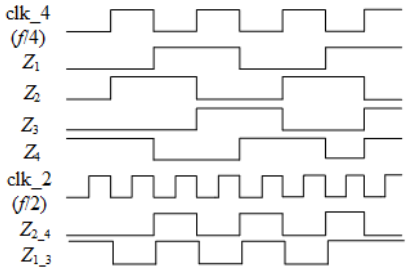


Figure 3. The timing diagram of Z_1, Z_3, Z_{1_3}, Z_2, Z_4, and Z_{2_4}.

4. Compressed Sensing Circuit

4.1. Structure of the CS Circuit

A CS circuit for ECG signals is presented based on the proposed measurement matrix generator. The circuit architecture of the CS circuit is shown in Figure 4, which includes the following six modules:

1. ADC: The ADC converts the ECG signals into digital signals, while the other five modules compress the signals.
2. Clock module: The dominant clock f is divided into two clocks with frequencies $f/4$ and $f/2$, respectively.
3. Matrix generation module: The measurement matrix generator produces a serial sparse binary matrix $\mathbf{\Phi}$.
4. Control module: It generates the enable signals to control the matrix generation, compression calculation, and storage modules on or off, which can significantly reduce dynamic power consumption.
5. Compression calculation module: The module uses a serial calculation method to compress the N-dimension signal into an M-dimension signal by the measurement matrix $\mathbf{\Phi}$.
6. Storage module: It contains M memories that update data in the compression process and store the final results.

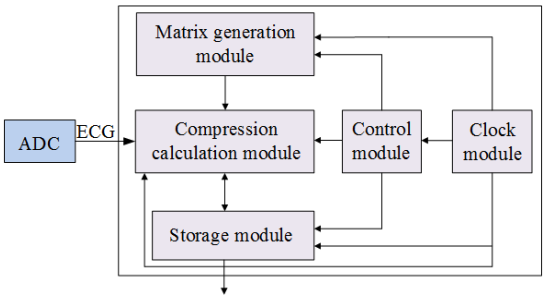


Figure 4. ECG signals processing circuit architecture.

4.2. Compression Calculations

Since the sequence of the measurement matrix is serial, the corresponding compression calculations are also serial. Only one adder unit is needed, so the compression calculation area is small. This paper adopts a serial architecture to realize the compression of ECG signals, as shown in Figure 5. One input of the adder depends on the measurement matrix's element. If the element is 1 (0), the input is ECG data (0). The other input comes from the data of the storage module. The storage module buffers the results of each addition operation.

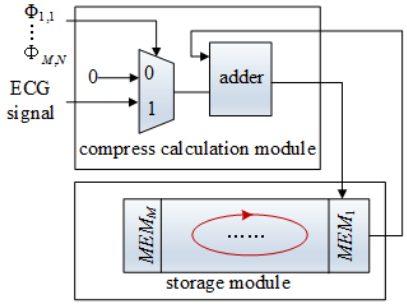


Figure 5. The compression process.

Specifically, after the compression calculation module receives the first ECG signal value, the values of $\Phi_{1,1} \times x_1$, $\Phi_{2,1} \times x_1$, . . . , and $\Phi_{M,1} \times x_1$ will be obtained at the frequency of f, and stored in MEM_1, MEM_2, . . . , and MEM_M, respectively. After receiving the second ECG signal value, the compression calculation module performs $\Phi_{2,1} \times x_2 + MEM_1$, $\Phi_{2,2} \times x_2 + MEM_2$, . . . , and $\Phi_{M,2} \times x_2 + MEM_M$, then stores the calculated results into the corresponding memories. Only the addition operation is required for the compression, as the measurement matrix elements are either 0 or 1. Since the element's probability of taking the value of 1 is about 1/4, the number of addition calculations required is significantly reduced, minimizing the dynamic power consumption.

5. Simulation and Implementation

5.1. Parameter Determination

The CS algorithm is simulated using MATLAB to determine the relevant parameters of the circuit. The experimental data are ECG signals from the MIT-BIH database, and Records 101 and 102 are selected for testing. The MIT-BIH database is chosen among the Internet—available ones as it is the most widely used in the scientific literature [22]. The sampling frequency for the ECG signals (f_{sample}) is 360 Hz. As can be found in Figure 6, when the value of CF is no more than 4, the PRD is less than 2%, which ensures the reconstruction quality. The reconstruction quality is worse than others when M is 32. However, when M arrives at 128, the reconstruction quality reaches a level close to M = 64, but it consumes more power and occupies a larger area.

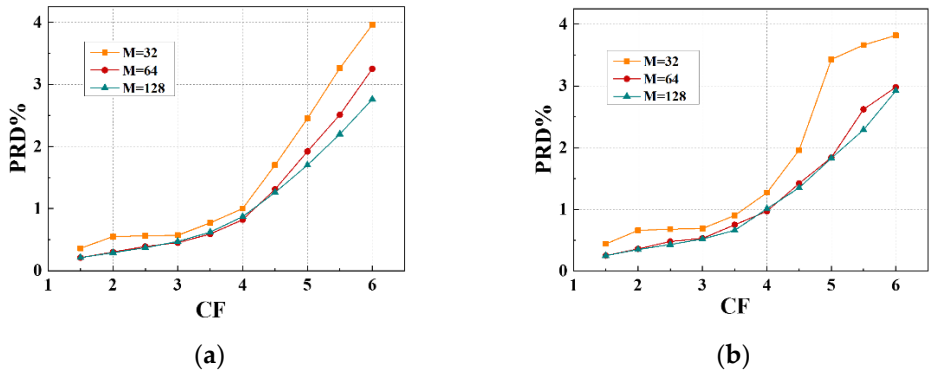


Figure 6. Reconstruction quality with various M and CF, (**a**) Records 101; (**b**) Records 102.

Therefore, the values of M and CF are set to 64 and 4, respectively. Therefore, N = CF $\times$ M = 256. The maximum sequence length m is determined from Equation (2). The value of n is determined by the result of $M \times N$, which is 16,384. Since 32,767 ($2^{15} - 1$) is larger than 16,384, the value of n is set to 15.

5.2. Implementation

Since n is 15, the primitive polynomial is chosen to be $1 + x^{14} + x^{15}$. Equation (4) can be calculated by:

$$\mathbf{W} = \begin{bmatrix} 0 & 0 & \cdots & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & \cdots & \cdots & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & \cdots & \cdots & \cdots & 0 & 1 & 1 & 0 \\ 0 & 0 & \cdots & \cdots & \cdots & \cdots & 0 & 1 & 1 \\ 1 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ 0 & 1 & 0 & & & & & & 0 \\ \vdots & & \ddots & & & & & & \vdots \\ \vdots & & & \ddots & & & & & \vdots \\ 0 & \cdots & \cdots & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix}_{15\times 15} \tag{10}$$

Therefore, the connections of flip-flops in the measurement matrix generator are determined as follows:

$$\begin{cases} \mathrm{DFF}_1/D = \mathrm{DFF}_{11}/Q \oplus \mathrm{DFF}_{12}/Q \\ \mathrm{DFF}_2/D = \mathrm{DFF}_{12}/Q \oplus \mathrm{DFF}_{13}/Q \\ \mathrm{DFF}_3/D = \mathrm{DFF}_{13}/Q \oplus \mathrm{DFF}_{14}/Q \\ \mathrm{DFF}_4/D = \mathrm{DFF}_{14}/Q \oplus \mathrm{DFF}_{15}/Q \\ \mathrm{DFF}_5/D = \mathrm{DFF}_1/Q \\ \cdots \\ \mathrm{DFF}_{15}/D = \mathrm{DFF}_{11}/Q \end{cases} \tag{11}$$

The implementation of the matrix generation module is shown in Figure 7. The first group of flip-flops includes DFF_1, DFF_5, DFF_9, and DFF_{13}, and the second group of flip-flops includes DFF_2, DFF_6, DFF_{10}, and DFF_{14}, and so on. The four sets of pseudo-random sequences Z_1, Z_2, Z_3 and Z_4 are generated at the clock frequency of $f/4$. The frequencies of sequences Z_{1_3} and Z_{2_4} are raised to $f/2$ by the XOR gates. In addition, the values of Z_{1_3} and Z_{2_4} are equal to $Z_1 \oplus Z_3$ and $Z_2 \oplus Z_4$, respectively. The frequency of sequence Z is raised to f by the AND gate. The value of Z is equal to Z_{1_3} * & Z_{2_4} *, and & represents the AND operation. In the sequence Z *, the elements $a_1, \ldots,$ and a_M are used as the first column of the measurement matrix, $a_{M+1}, \ldots,$ and a_{2M} as the second column, and so on. Therefore, the measurement matrix $\mathbf{\Phi}$ is generated, and $[\Phi_{1,1}, \Phi_{2,1}, \ldots, \Phi_{M,1}]^{\mathrm{T}}$ corresponds to $[a_1, a_2, \ldots, a_M]^{\mathrm{T}}$, $[\Phi_{1,2}, \Phi_{2,2}, \ldots, \Phi_{M,2}]^{\mathrm{T}}$ corresponds to $[a_{M+1}, a_{M+2}, \ldots, a_{2M}]^{\mathrm{T}}$, and so on.

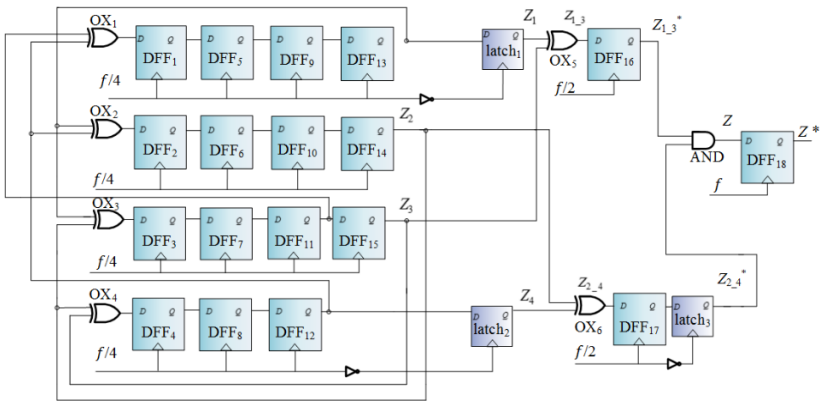


Figure 7. Matrix generation module.

The sampling frequency for the ECG signals (f_{sample}) is set to 360 Hz in the compression calculation and storage modules. The clock frequency f is at least M times of the sampling frequency. Since 40,000 >> 23,040 (64 × 360), the frequency f is chosen to be 40 kHz.

The CS circuit is implemented using Verilog. This paper uses a 12-bit asynchronous low-power SAR ADC. The simulation waveform is shown in Figure 8. The inputs include two clock signals, *clk_pad* and *sample_pad*, and two control signals, with one enabling the ECG signals named *ecg_valid_pad* and the other named *rst_n_pad* for reset control. The 12-bit ECG data *xin* comes from the SAR ADC.

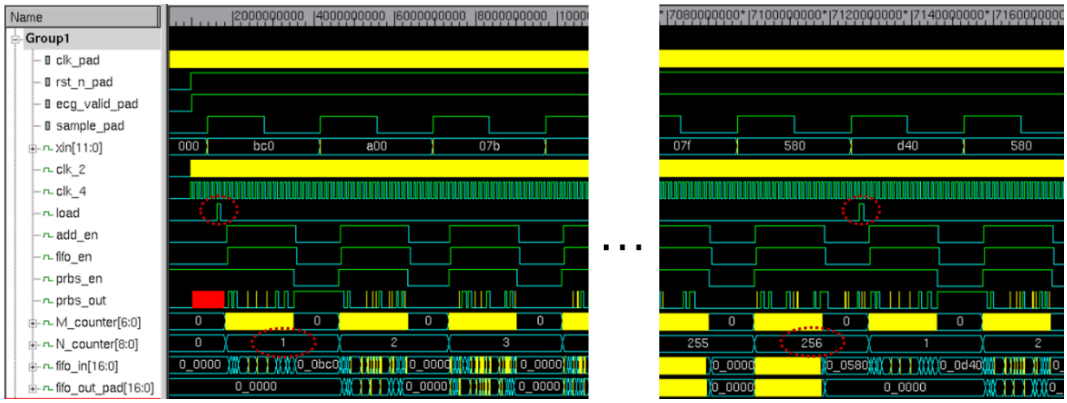
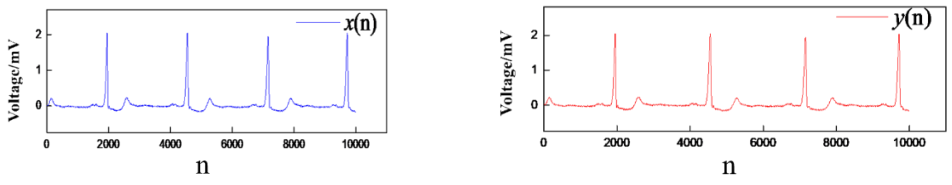


Figure 8. Waveforms of CS circuit.

Specifically, the signal *prbs_en* is set to 0 to disable the matrix generation module after M calculations of ECG data. The simulation results show that out of the 16,384 elements of the measurement matrix, 4099 elements are 1 (accounting for about 1/4), and the rest 12,285 are all elements 0. The compression calculation and storage modules are enabled by *add_en* and *fifo_en*, respectively. After the signal *load* is set to 1, the matrix generation module loads the seed. Seed is the initial value of flip-flops in the LFSRs. The seed selected in this paper is 15′b1010_1100_1110_011.

The compression calculation process is determined by the counters *M_counter* and *N_counter*. If *M_counter* = c and *N_counter* = d, it indicates that the calculation is currently $\Phi_{c,d} \times x_d$ ($1 \leq c \leq M$, $1 \leq d \leq N$). As shown in Figure 8, when *N_counter* is 9′d256, the 256th data is compressed, and one compression cycle is completed. The output signal *fifo_out_pad* is the compressed data. ECG signals are periodic. The simulation results show that the compressed data are all less than 131,072, so the signal *fifo_out_pad* is set to 17 bits, reducing the circuit's redundancy design and power consumption.

After the simulation, the compressed ECG data are imported into MATLAB and reconstructed by the BSBL algorithm. The original and reconstructed signals are shown in Figure 9, where $x(n)$ represents the original signal from the database and $y(n)$ represents the reconstructed signal. The PRD is 1.32%, so the quality of the reconstructed signal can be considered "very good".



(**a**) (**b**)

Figure 9. (**a**) Original signal; (**b**) Reconstructed signal.

The proposed architecture is implemented in a SMIC 55 nm CMOS process. A standard-cell RTL to GDSII flow is used to implement the chip. The supply voltage

selected in this work is 1.2 V. Figure 10 depicts the chip layout after place and route, and the area is 0.608 mm^2 (780 µm × 780 µm), which IO limits. Without taking IO into account, the core area is only 0.059 mm^2 (244 µm × 243 µm), including the ADC area of 0.011 mm^2 (85 µm × 134 µm).

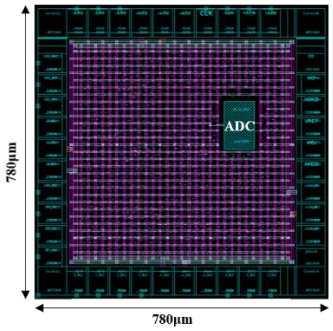


Figure 10. The layout of this work.

Power consumption is simulated after physical implementation. Table 1 lists the power consumption results. The total power is 1.690 µW, of which the IO power is 1.003 µW and the core power is 0.687 µW, including the ADC power of 0.049 µW. The dynamic power is 0.484 µW and the static power is 1.206 µW. The dynamic power ratio is as low as 28.6%, which is effectively reduced.

Table 1. Power consumption results.

Process	Supply	Frequency	Static Power	Dynamic Power	Total Power
SMIC 55 nm	1.2 V	40 kHz	1.206 µW	0.484 µW	1.690 µW

6. Discussion

Compared with other parallel architectures, the proposed architecture has less hardware consumption. The comparison with other work and related performance parameters are shown in Table 2, where area and power consumption are for core excluding IO. Our work requires a lower clock frequency and provides significant power advantages while consuming a smaller area. In addition, the compression and reconstruction performance measured by CF and PRD is better than other work.

Table 2. CS circuit comparisons with other work.

Source	Tech (nm)	Supply (V)	ADC (bit)	Frequency (MHz)	CF	PRD	Area (mm^2)	Power (µW)
Nasimi [10]	/	0.6	/	100	2	5%	/	84.5
Kumar [11]	65	0.65	/	15	3	/	0.128	238
Li [12]	40	1.1	/	5	1.25	/	0.049	117
Liu [13]	180	1.8	16	4	4	/	1.5	155
Our work	55	1.2	12	0.04	4	1.32%	0.059	0.687

7. Conclusions

This paper proposes a serial measurement matrix generator and implements a CS circuit for ECG signals in a SMIC 55 nm CMOS process. The work shows significant advantages over traditional parallel architecture. In addition, the compressed results are imported into MATLAB and reconstructed by the BSBL algorithm. The PRD is 1.32%, indicating that the reconstructed quality is "very good", so this design could be used in health monitoring and clinical medicine.

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