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An Improved Partially Interleaved Transformer Structure for High-voltage High-frequency Multiple-output Applications

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***Abstract*— This paper proposes an improved partially interleaved structure for high-voltage (several kV) high-frequency (several hundred kHz) multiple-output applications. The proposed transformer structure is compared with other typical structures with the leakage inductance, AC capacitance, AC resistance and the ratio of AC/DC resistance taken into consideration. The proposed structure features lower leakage inductance, smaller AC capacitance, lower AC resistance and lower ratio of AC-DC resistance, which is suitable for high-frequency high-efficiency applications. A planar transformer with the proposed structure was built and tested in an LCLC resonant converter, where the input voltage is 40 V, output is 4800 V, switching frequency is 500 kHz, the output power is 288 W and the efficiency is 96.8%, which validates the analysis.**

***Index Terms*— high-voltage, high-frequency, improved partially interleaved structure, multiple-output, planar transformer**

I. Introduction

High-voltage power supplies with multiple outputs are widely used in Travelling-Wave Tube Amplifiers [1] (TWTAs), lasers [2], Magnetic Resonance Imaging (MRI) [3], where several high-voltage outputs are required by the system. Nowadays, the power supplies are moving towards high power density and high efficiency, which is mainly restricted by the magnetic components and semiconductors in high-voltage multiple-output application. The emergence of novel power switches, such as GaN and SiC devices [4, 5, 6] helps to increase the power density and efficiency from the semiconductor aspect. However, the magnetic design, especially the high-voltage transformer design is still a big challenge. The reason can be given as follows. In order to achieve high efficiency, resonant topologies are applied to reduce the switching loss. The structure of a high-voltage planar transformer has a crucial role on the performance of a resonant converter since its parasitic impedances are utilized to form a resonant tank [7, 8, 9]. As for the leakage inductance, the general way to reduce the leakage is using the interleaving structure. However, the parasitic capacitance will increase as the interleaving will lead to more overlapped area. From the aspect of the parasitic capacitance, the common way is to shift the winding to reduce the overlapped area. However, the shifting will result in the increase of the leakage. As a result, the leakage inductance and parasitic capacitance are interrelated and need careful consideration. Taking the LCLC resonant converter as an example (Fig. 1a), the leakage inductance (L_r), magnetizing inductance (L_m) and parasitic capacitance (C_p) of the transformer are utilized in the resonant tank. The 3D structure of a high-voltage planar transformer is shown in Fig. 1b. As for the switching frequency of the LCLC resonant converter, it is lower than 100 kHz, which is mainly limited by the parasitic parameters of the high-voltage transformer [1].

The planar transformer has been investigated and used comprehensively since it was proposed. Previous research investigated different winding configurations [10, 11], the analysis of impedances [12] and the design of the planar transformers [13, 14]. However, these researches mainly focused on low-voltage high-current applications, which is due to the difficulty in designing the adequate electrical insulation. However, with the development of the Polyimide PCB, the capability for providing electrical insulation has improved greatly, with the electric field intensity increasing from 3 kV/mm to 80 kV/mm or higher [15], which contributes to the application of the planar transformer in the high-voltage field.

In high-voltage applications, apart from the AC/DC resistance and L_r, the electrical insulation and C_p need further investigation [14]. However, C_p is always ignored in the previous researches, such as LLC resonant converters. This is due to the larger impedance of C_p compared with that of L_m. However, in high-voltage applications, in order to boost the output voltage, there are few turns in the primary side with a large number of turns in the secondary side. As a result, a large C_p exists, the impedance of which is comparable with that of L_m. Therefore, C_p cannot be ignored.

In resonant converters, C_p is utilized as the resonant component, which will affect the efficiency and switching

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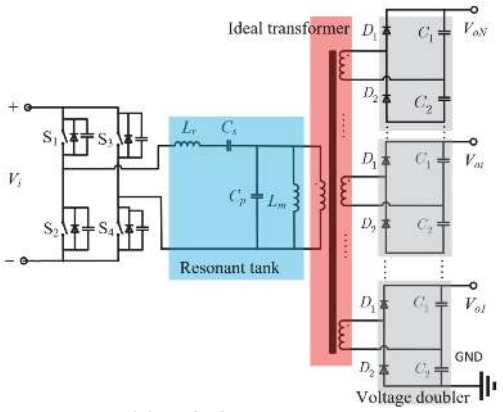
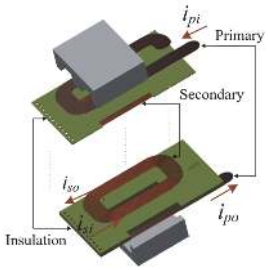


(a) LCLC resonant converters



(b) 3D structure of a high-voltage planar transformer

Fig. 1 High voltage transformer with voltage doublers

frequency of the converter. Take the LCLC resonant converter as an example [16], the energy to charge or discharge C_p is mainly provided by L_m. With higher C_p, the energy required for the charging or discharging will increase, which will increase the conduction loss. In this way, C_p needs careful design.

This paper focuses on the applications of the planar transform in high-voltage field and manages to do the trade-off design among all the parasitics. An improved partially interleaved transformer structure for high-voltage high-frequency multiple-output applications is proposed. The proposed structure and other typical structures are shown in Section II. In Section III, IV and V, the comparison between the proposed structure and other typical structures is made, with L_r, AC resistance (R_{ac}), the ratio of AC/DC resistance and AC capacitance (C_p) taken into consideration. In Section VI, the partial discharge of the high-voltage transformer caused by the partial interleaving is discussed. In Section VII, a planar transformer with the proposed structure is built and tested in LCLC resonant converters. Section VIII provides a summary of the whole paper.

II. Winding Configurations for High-voltage Planar Transformers

In high-voltage multiple-output DC-DC converters, as illustrated in Fig. 1, there are always several secondary windings and to further boost the voltage, each secondary winding is often connected to a voltage doubler. Each output of a voltage doubler can be used as an independent output. As a result, there are several outputs.

Interleaving is a general method to reduce the leakage inductance; however, it may cause an increase of the parasitic capacitance. In this paper, the overall effect of interleaving is investigated. As for the secondary winding, each secondary winding needs at least two layers, with one layer for the incoming line and the other for the outgoing line. The configurations of secondary windings considered in this work are illustrated in Fig. 2. The parasitic capacitance between two adjacent turns (C_{inter}) and between two layers (C_{intra}) are labeled.

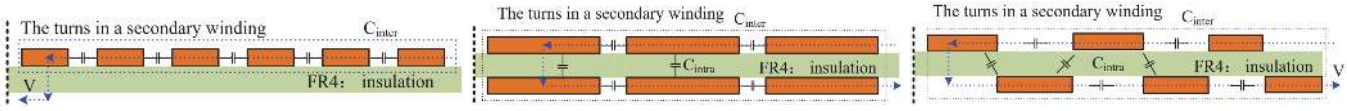
The single-layer structure is shown in Fig. 2(a), where all the turns in a secondary winding are in a single layer, while the other layer is only used for the outgoing line. As a result, C_{intra} is low. However, it is obvious that the layer for the outgoing line is not fully utilized, which results in higher DC resistance.

The two-layer structure is shown in Fig. 2(b). In this structure, half of the turns in a secondary winding are on one layer while other turns are on the other layer. The two layers are fully utilized and the conductors have the largest width compared with the single-layer structure and the non-interleaved structure, which means that the lowest DC resistance can be achieved. However, because of the large overlapped area, the parasitic capacitance may be high.

The non-overlapped structure is shown in Fig. 2(c). In this structure, half of the turns are on one layer while other turns are on the other layer, which is similar to the two-layer structure. Compared with the two-layer structure, the overlapped area of the turns is minimized to reduce the intra-winding parasitic capacitance.

Combing the primary windings with the secondary windings, a range of winding configurations of the planar transformer is derived, as shown in Fig. 3. There is one primary winding with *m* turns and *n* secondary windings. Fig. 3(a), (c) and (e) show the non-interleaved structures, while Fig. 3(b), (d) and (f) show the partially interleaved structures. In order to ensure the effectiveness of the electrical insulation, a thick insulation is used between the high voltage sides of the primary and secondary windings in the partially interleaved structures. The thickness of this insulation is determined by the insulation material and the voltage between the primary and secondary windings. In addition, the distribution of the parasitic capacitance is also shown in Fig. 3, which will be discussed in Section V.

The derivation of the equations, such as the leakage inductance and AC capacitance, are based on the general structure shown in Fig. 3 and can be easily adopted to other cases easily. In addition, an example is also given to validate the analysis. In order to make a fair comparison, in this example, all the six winding structures use the same magnetic core, which is FEE 38/16/25 and the magnetic material is N87 from



(a) Single-layer structure (b) Two-layer structure (c) Non-overlapped structure

Fig. 2 Configurations of the secondary winding

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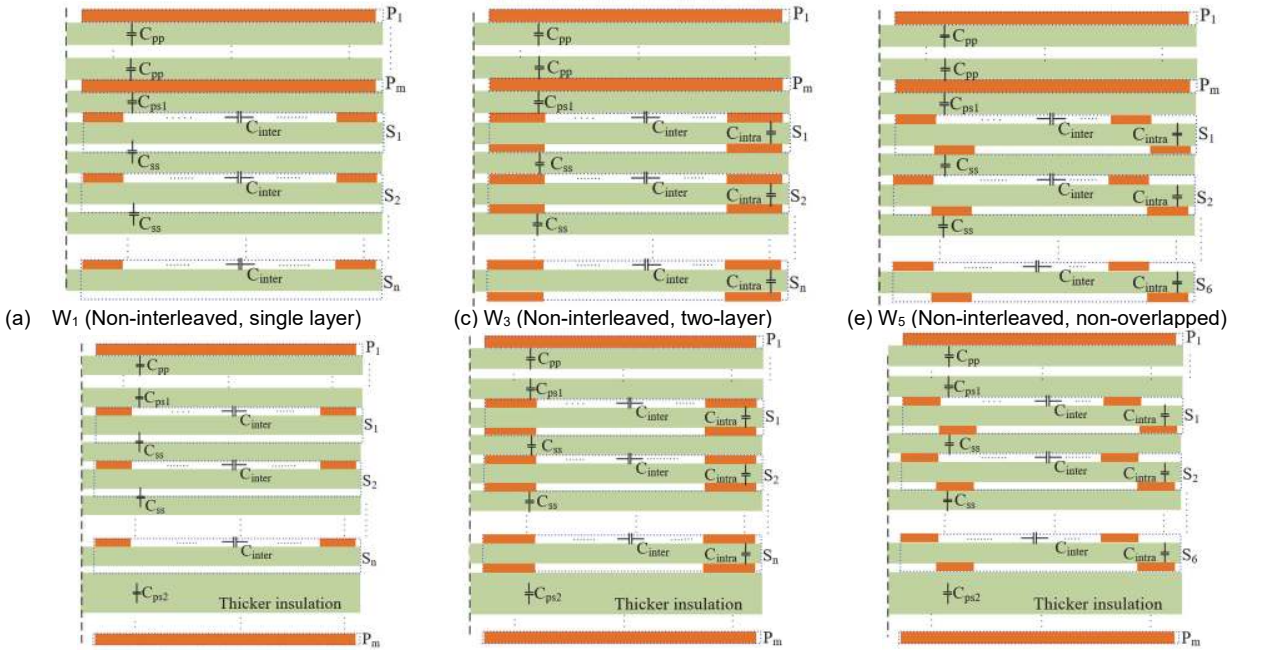

(a) W_1 (Non-interleaved, single layer) (c) W_3 (Non-interleaved, two-layer) (e) W_5 (Non-interleaved, non-overlapped)

(b) W_2 (Partially interleaved, single layer) (d) W_4 (Partially-interleaved, two-layer) (f) W_6 (Partially-interleaved, non-overlapped)

Fig. 3 Overview of the winding configurations for high-voltage planar transformers

TDK. In addition, each structure has one primary winding and six secondary windings, with two turns in the primary winding and twenty turns in each secondary winding. The parameters of the windings are given in Table I.

In the following parts, the parasitic parameters of the winding configurations (L_r, the ratio of AC/DC resistance, R_{ac} and C_p) will be compared.

III. Leakage Inductance

In a resonant converter, L_r is always used as a resonant component in the resonant tank and will affect the resonant condition. As a result, it is important to predict L_r. In Part A, the L_r of each winding configuration is calculated based on the Magneto-motive Force (MMF). In Part B, the L_r is simulated in Ansys Maxwell. Finally, the calculated results are compared with the simulated results to validate the correctness of the calculations.

TABLE I
PARAMETERS OF HIGH VOLTAGE PLANAR TRANSFORMERS

Symbol	Quantity	Value
w_p	Width of the primary winding	7.27 mm
d_p	Thickness of the primary winding	0.2 mm
d_s	Thickness of the secondary winding	70 μm
d_{ni}	Thickness of the normal insulation	0.3 mm
d_{ti}	Thickness of the thicker insulation	1.6 mm
d_{cw}	The safe distance between the windings and the core	1.7 mm
d_{s1}	The width of the turns in single-layer structure	0.27 mm
d_{s2}	The width of the turns in two-layer structure	0.64 mm
d_{s3}	The width of the turns in non-overlapped structure	0.36 mm
P_T	Nominal power of the transformer	288 W

A. Calculations of leakage inductance

The calculation of L_r is based on the MMF distribution. The magnetizing current is ignored and the ampere-turn of the primary windings is equal to that of the secondary windings. Assuming i_p is applied to the primary winding, the MMF distribution is shown in Fig. 4. It can be seen from Fig. 4 that compared with the corresponding non-interleaved structure, the highest magnetic field intensity is reduced with partially interleaved structures, which means the even distribution of the magnetic field.

Assuming the magnetic field intensity is constant in the horizontal direction, based on the distributions of MMF, H can be calculated by

$$\sum_{i=1}^{N} I_i = HW_w \tag{1}$$

where W_w is the width of the core widow. $\sum_{i=1}^{N} I_i$ is the total current that contributes to MMF. Calculations are carried out by assuming the direction out of the paper is positive while the direction into the paper is negative.

As a result, the magnetic energy, E_m can be derived by the integration of the magnetic energy density over the core window volume

$$E_m = \frac{1}{2}\iiint \mu_0\mu_r H^2 dV \tag{2}$$

According to the relation of the transformer leakage inductance, L_r and the magnetic energy

$$E_m = \frac{1}{2}L_r i_p^2 \tag{3}$$

Combing (2) and (3), the L_r referred to the primary side can be calculated by

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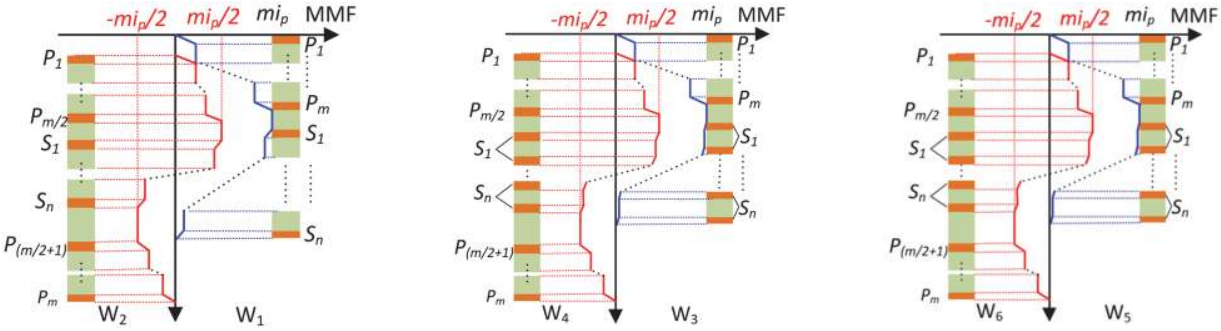


(a) Distribution of MMF of W_1 and W_2 (b) Distribution of MMF of W_3 and W_4 (c) Distribution of MMF of W_5 and W_6

Fig. 4 Distribution of MMF in different configurations

$$L_r = \frac{1}{i_p^2}\iiint \mu_0\mu_r H^2 dV \quad (4)$$

where i_p is the current excitation applied to the primary winding. It should be pointed out that (4) is only valid considering a linear operation point, far from magnetic saturation.

The winding configurations with the parameters in Table I are used as an example to compared the leakage inductance. The calculation results of L_r are listed in Table II. It may be concluded that with the partially interleaved structures (W_2, W_4 and W_6), compared with the corresponding non-interleaved structures (W_1, W_3 and W_5), the L_r is reduced by half.

TABLE II
CALCULATION RESULTS OF THE LEAKAGE INDUCTANCES

Winding configurations	Value (nH)
W_1	125.02
W_2	54.54
W_3, W_5	137.78
W_4, W_6	60.37

It should be pointed out that the analytical calculations are based on the assumption that the current is distributed evenly through the conductors. However, in the range of several hundred kHz, the relative errors are acceptable [17].

B. Simulation of leakage inductance

In order to validate the accuracy of the calculation results, Finite Element Analysis (FEA) simulations were carried out in Ansys Maxwell with the same current levels applied to the primary and secondary windings as in calculations. The distributions of the magnetic field intensity, H, in W_1, W_2 and W_4 at 500 kHz are shown in Fig. 5.

It can be seen from Fig. 5 that the compared with the non-interleaved structure (Fig. 5a), in the partially interleaved structures (Fig. 5b), the highest magnetic field intensity is reduced, which is accordance with the analytical analysis.

Based on the distributions of the magnetic field intensity, the L_r of each winding configuration can be calculated. The L_r in each winding configuration versus frequency is shown in Fig. 6.

It may be concluded that compared with non-interleaved structures (W_1, W_3 and W_5), the L_r of the partially interleaved structures (W_2, W_4 and W_6) are greatly reduced. Among the partially interleaved structures, the single-layer structure (W_2) and two-layer structure (W_4) share almost the same L_r, which is slightly lower than that of W_6. W_4 and W_6 have the same MMF distribution and therefore the analytic formulas predict that they have the same L_r. However, because the turns in the two layers of W_6 are shifted from one another, coupling between them is lower than in W_4 where the turns on all winding layers are in the same radial location, and this results in higher L_r for W_6.

C. Comparison of the calculation results and the simulation results

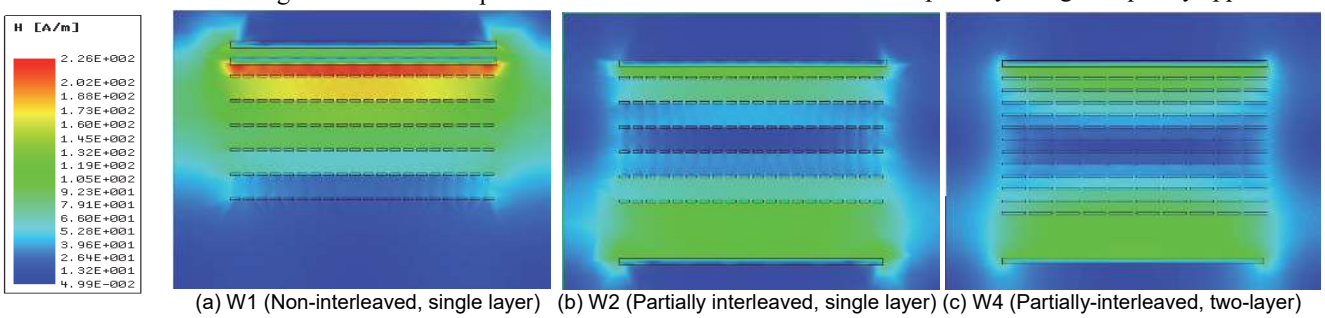
The comparison of the simulation and the calculated results is shown in Fig. 7.

It can be seen that the calculated results show good agreement with the simulation results, which validates the effectiveness of the calculations. In order to operate at high switching frequency, a lower L_r is required.

In this way, W_2 and W_4 are suitable for high switching frequency, high power density applications.

IV. AC RESISTANCE

The R_{ac} is a significant parameter to determine the copper loss of a transformer, especially in high frequency applications,



(a) W1 (Non-interleaved, single layer) (b) W2 (Partially interleaved, single layer) (c) W4 (Partially-interleaved, two-layer)

Fig. 5 Distributions of the magnetic field @ 500 kHz

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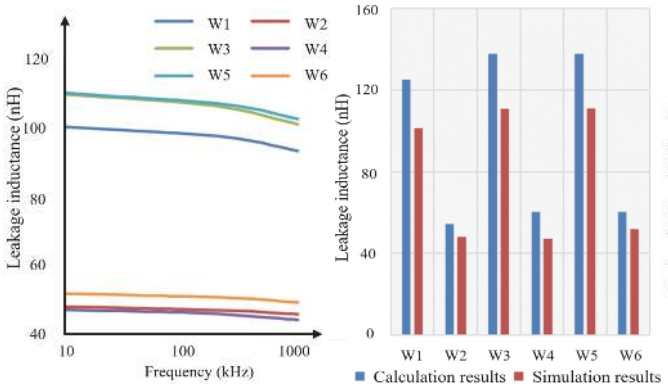

Fig. 6 Simulated leakage inductance Fig. 7 Comparison of leakage inductance

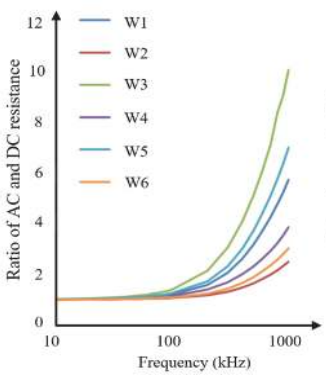

Fig. 8 AC/DC resistance

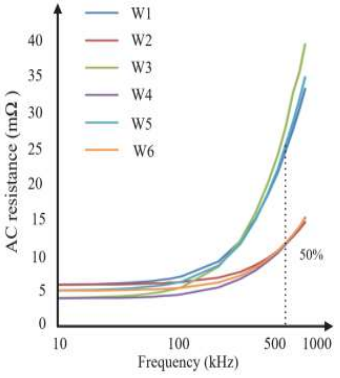

Fig. 9 AC resistance

where the proximity effect and eddy skin effect will lead to the huge increase of the R_{ac}. In this section, the total AC/DC resistance referred to the primary side is analyzed. At first, the ratio of AC/DC resistance referred to the primary side is simulated in FEA software to show the high-frequency characteristics. After that, in order to assess the copper loss, the R_{ac} of each winding configuration referred to the primary side is simulated.

A. The ratio of AC/DC resistance

The ratio of AC/DC resistance can be used to reflect the high-frequency characteristics. The simulation results of the ratio of AC/DC resistance are shown in Fig. 8.

It can be seen from Fig. 8 that the AC/DC resistance of the partially interleaved structures (W_2, W_4 and W_6) is lower than that of the non-interleaved structures (W_1, W_3 and W_5). It can be explained as follows. In the non-interleaved structure, higher leakage energy in the window leads to higher proximity effect, which means the conductors in the non-interleaved structures suffer more severe proximity effect.

As for the AC/DC resistance of W_2 and W_4, it can be seen from Fig. 5 that the distance between two adjacent layers in W_2 is doubled compared with that of W_4. In this way, the proximity effect is reduced further.

B. AC resistance

Although it is proved that W_2 has the lowest ratio of AC and DC resistance, it should be noted that the DC resistance of W_4 is lower than that of W_2, which means that in the low-frequency range, the AC resistance of W_4 is still lower than that of W_2. Therefore, it is significant to investigate the absolute value of the R_{ac}.

The R_{ac} is simulated in FEA software and the R_{ac} versus frequency is shown in Fig. 9.

It can be seen from Fig. 9 that partially interleaved structures (W_2, W_4 and W_6) have better high-frequency characteristics than the corresponding non-interleaved structures (W_1, W_3 and W_5), which is in accordance with the previous analysis. In addition, the R_{ac} of W_4 is the lowest at low frequency (less than 500 kHz), mainly profiting from lower DC resistance. However, when the frequency increases to 500 kHz, the R_{ac} of W_4 increases to the same value as W_2. When the switching frequency is higher, the R_{ac} of W_4 will be higher than that of W_2, which means less copper loss in W_2 at high frequency (larger than 500 kHz).

Based on the above analysis, it can be concluded that under high frequency conditions, the partially interleaved, single layer structure, W_2 has better high-frequency characteristics and lower copper loss. In addition, compared with the non-interleaved structure, the corresponding partially interleaved structure has 50% reduction in the R_{ac}. However, the critical frequency may vary from case to case and need further investigation according to the specific application.

V. AC Capacitance

In the LCC and LCLC resonant converters, the AC capacitance (C_p) of a transformer is used as a resonant component in the resonant tank. In the LCLC resonant converters, higher C_p means more circulating energy, which will lead to higher conduction loss. Therefore, it is significant to investigate the winding configurations to find one with lower C_p.

The distributions of the C_p in each structure are shown in Fig. 3. C_{ps1} and C_{ps2} are the parasitic capacitances between the primary winding and the secondary windings. C_{ss} is the parasitic capacitance between two secondary windings. C_{intra} is the parasitic capacitance between two layers in a secondary winding. C_{inter} is the parasitic capacitance between two adjacent turns in the same layer.

In this section, taking the voltage doublers into consideration, the C_p of each winding configuration is calculated and the calculated results are validated by the simulation results.

A. Calculation of AC capacitance

The calculation of the C_p referred to the primary side is based on the following method. Assuming V_p is applied to the primary winding, the voltage per turn is V_p/n_p. Then the voltage of each turn both in the primary and secondary windings can be calculated. The C_p referred to the primary side can be calculated by [14]

$$C_p = \frac{2E_{tot}}{V_p^2} \tag{5}$$

Where E_{tot} is the total electric energy stored in the window of the magnetic core.

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TABLE III
THE VOLTAGE (AC+DC) OF EACH TURN IN THE SECONDARY WINDINGS

T	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
W_1	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_2	20.5	21	21.5	22	22.5	23	23.5	24	24.5	25	25.5	26	26.5	27	27.5	28	28.5	29	29.5	30
W_3	40.5	41	41.5	42	42.5	43	43.5	44	44.5	45	45.5	46	46.5	47	47.5	48	48.5	49	49.5	50
W_4	60.5	61	61.5	62	62.5	63	63.5	64	64.5	65	65.5	66	66.5	67	67.5	68	68.5	69	69.5	70
W_5	80.5	81	81.5	82	82.5	83	83.5	84	84.5	85	85.5	86	86.5	87	87.5	88	88.5	89	89.5	90
W_6	100.5	101	101.5	102	102.5	103	103.5	104	104.5	105	105.5	106	106.5	107	107.5	108	108.5	109	109.5	110

TABLE IV
THE VOLTAGE (AC) OF EACH TURN IN THE SECONDARY WINDINGS

T	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
W_1	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_2	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_3	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_4	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_5	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
W_6	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10

In this case, the electric energy contains four parts: the electric energy stored between the primary winding (E_{pp}), between the primary winding and the secondary windings (E_{ps}), the electric energy stored in the secondary windings, the electric energy stored between two secondary windings (E_{ss}).

The electric energy in the primary winding is

$$E_{pp} = \frac{1}{2}\sum_{i=1}^{m-1} C_{pp\_i} V_{pp\_i}^2 \tag{6}$$

Where C_{pp_i} is the parasitic capacitance between two turns in the primary winding. V_{pp_i} is the voltage of the capacitance.

The electric energy stored between the primary windings and the secondary windings can be calculated by

$$E_{ps} = \frac{1}{2}\sum_{i=1}^{2} C_{ps\_i} V_{ps\_i}^2 \tag{7}$$

Where C_{pp_i} is the parasitic capacitance between two turns in the primary winding. V_{pp_i} is the voltage of the capacitance.

The energy stored in a secondary winding contains two parts. The first part is the electric energy stored between two adjacent turns in the same layer, which can be calculated by

$$E_{inter} = \frac{1}{2}\sum_{i=1}^{Ns-1} C_{inter\_i} V_{inter\_i}^2 \tag{8}$$

Where N_s is the number of the turns in a secondary winding. C_{inter_i} is the capacitance between two adjacent turns in the same layer, which can be calculated by the equation for the plane-parallel capacitor. V_{intra_i} is the voltage between two adjacent turns, which is V_p/n_p.

The second part is the electric energy stored between two layers in a secondary winding, which can be calculated by

$$E_{intra} = \frac{1}{2}\sum_{i=1}^{Ns/2} C_{intra\_i} V_{intra\_i}^2 \tag{9}$$

Where C_{intra_i} is the capacitance between two layers in a secondary winding, which can be calculated by the equation for the plane-parallel capacitor.

The electric energy stored between two adjacent secondary windings can be calculated by

$$E_{ss} = \frac{1}{2}\sum_{i=1}^{Ns/2} C_{ss\_i} V_{ss\_i}^2 \tag{10}$$

Where C_{ss_i} is the capacitance between two adjacent secondary windings.

As a result, the total electric energy of a system is the sum of the electric energy stored in all the capacitors in the system, which can be calculated by

$$E_{tot} = \sum_{j=1}^{m-1} E_{pp\_j} + \sum_{j=1}^{t} E_{ps\_j} + \sum_{j=1}^{n-1} E_{inter\_j} + \sum_{j=1}^{n-1} E_{inter\_j} + \sum_{j=1}^{n-1} E_{ss\_j} \tag{11}$$

Where t is one in the non-interleaved structure and two in the partially interleaved structure.

Substituting (10) into (5), the C_p referred to the primary side can be calculated by

$$C_p = \frac{2(\sum_{j=1}^{m-1} E_{pp\_j} + \sum_{j=1}^{t} E_{ps\_j} + \sum_{j=1}^{n-1} E_{inter\_j} + \sum_{j=1}^{n-1} E_{inter\_j} + \sum_{j=1}^{n-1} E_{ss\_j})}{V_p^2} \tag{12}$$

However, in the high-voltage multiple-output applications, as shown in Fig. 1, since the output of each secondary winding is connected to a voltage doubler and in series with the other secondary winding, there is an increasing DC component across the winding capacitance, which is caused by the capacitors (C_1, C_2 …, and C_n) in the voltage doubler. Assuming 1V is applied to the primary winding, the voltage of each turn with the DC component in the secondary windings is listed in Table III.

Using the equations (6), (7), (8), (9), (10) and (11), and the AC voltage excitations in Table IV, the C_p referred to the primary winding in each winding configuration is calculated and calculated results are shown in Table V.

The following simulation results will validate the calculated results.

B. Simulation results of C_p

In order to validate the calculated results, the C_p is simulated in the electrostatic solver of Ansys Maxwell with the same voltage boundary conditions applied as in calculations. The distributions of the electric field intensity in W_1, W_2 and W_5 are shown in Fig. 10. For ease of comparison, all the color maps in Fig. 10 are produced to the same scale.

The C_p is calculated by the electric field energy. The simulated results are shown in Fig. 11. In order to facilitate comparison, the calculated results are included in Fig. 11 as well.

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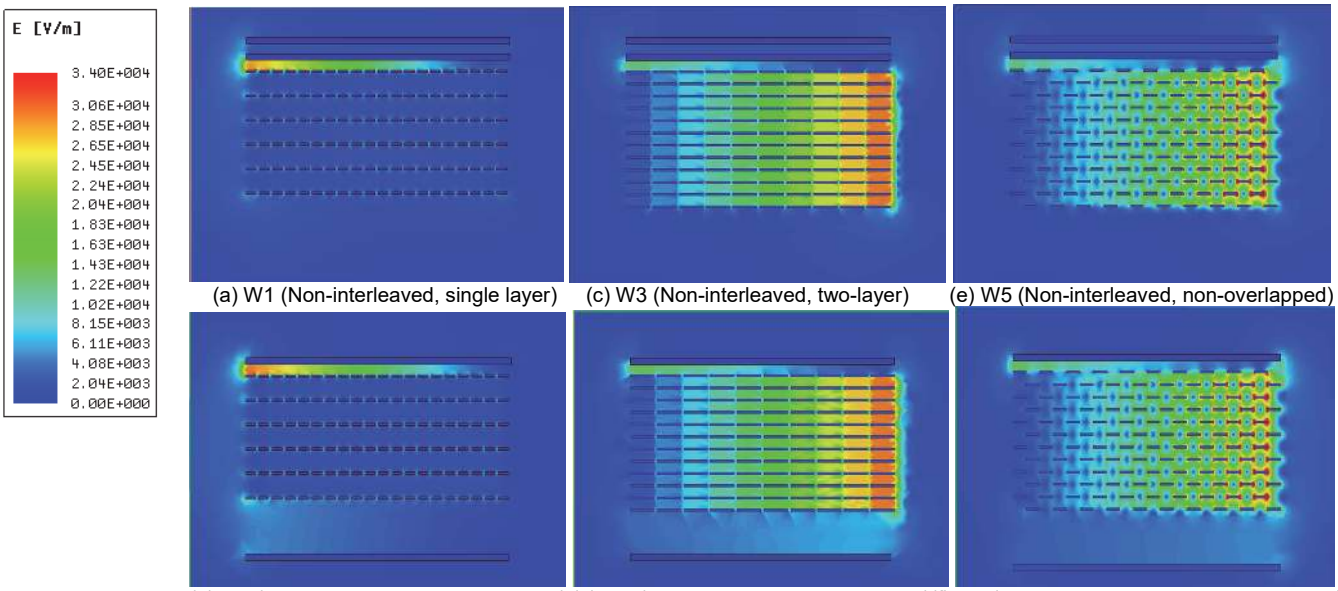

(a) W1 (Non-interleaved, single layer) (c) W3 (Non-interleaved, two-layer) (e) W5 (Non-interleaved, non-overlapped)

(b) W2 (Partially interleaved, single layer) (d) W4 (Partially-interleaved, two-layer)(f) W6 (Partially-interleaved, non-overlapped)

Fig. 10 Distributions of the electric field intensity

It can be seen from Fig. 11 that the calculation results are in accordance with the simulation results, which validates the accuracy of the calculations. The C_p of the partially interleaved structure is slightly higher than that of the corresponding non-interleaved structure because the partially interleaved structure causes extra capacitance between the primary winding and the secondary winding.

Among the three partially interleaved structures (W_2, W_4 and W_6), W_4 has the highest C_p, which can be explained by the following two reasons. Firstly, in the two-layer structure, half of the turns are on one layer while the other half are on another neighboring layer. As a result, there is high intra-winding capacitance (C_{intra}), which is shown in Fig. 2. In addition, the overlapped winding area in W_4 is the largest. Compared with W_4, the C_p of W_6 is much lower, mainly because the overlapped area is reduced. However, the large intra-winding capacitance (C_{intra}) still exists, which mainly contributes to the AC capacitance of W_6. W_2 has the lowest capacitance among all the partially interleaved structures. All the turns are in one layer while the other layer is used for the outgoing line only. In this way, C_{intra} is reduced greatly. As a result, the C_p of the single-layer structure is reduced.

VI. Comparison of The Transformer Design

A. Effect of the transformer design on resonant converter operation

The analysis about the parastics is summarized in Table VII. In the resonant converters, the parasitic parameters of the transformer will be utilized in the resonant tank and have crucial effect on the performance of the converter:

Effect of L_r. With higher leakage inductance (L_r), the switching frequency will be reduced, which will lead to the increase in the volume of the passive components, such as the inductors, transformers and the filter capacitors. For high-voltage applications, it is desirable that the transformer has low L_r. As a result, it can be seen from Table VII that the partially interleaved structures (W_2, W_4 and W_6) are suitable for high-frequency applications.

Effect of R_{ac}. The copper loss is main part of the power loss in a transformer. In order to reduce the copper loss, a winding configuration with low AC resistance (R_{ac}) is better than others. It can be seen from Table VII that taking the high-frequency application (higher than 500 kHz) into consideration, W_2, W_4 and W_6 have relative lower R_{ac}.

Effect of the C_p. As for the parasitic capacitance (C_p) of a transformer, a larger C_p will lead to high current to charge and discharge the capacitance and the conduction loss will increase. For low power loss considerations, a winding structure with low C_p is desirable. As a result, it can be seen from Table VII that W_1 and W_2, featured with low C_p, are desirable.

As a result, it can be concluded that from different points of

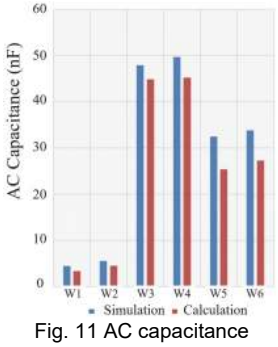

Fig. 11 AC capacitance

TABLE V
CALCULATION OF AC CAPACITANCE

Winding	C_p
W_1	6.72
W_2	9.0
W_3	44.83
W_4	45.2
W_5	25.4
W_6	27.3

TABLE VI
VOLTAGE EXCITATIONS

Winding	Voltage (kV)
P and S_1	1.2
S_1 and S_2	1.2
S_2 and S_3	1.2
S_3 and S_4	1.2
S_4 and S_5	1.2
S_5 and S_6	7.5

TABLE VII
SUMMARY OF THE PARASITICS VOLTAGE EXCITATIONS IN ELECTRIC INSULATION TEST

Winding	L_r (nH) (500kHz)	R_{ac}(mΩ) (500kHz)	Cp (nF)
W_1	95.5	18.38	8.72
W_2	46.4	9.6	11.1
W_3	103.6	20	44.83
W_4	44.9	9.14	45.2
W_5	105.0	18.54	25.4
W_6	50.16	9.43	27.3

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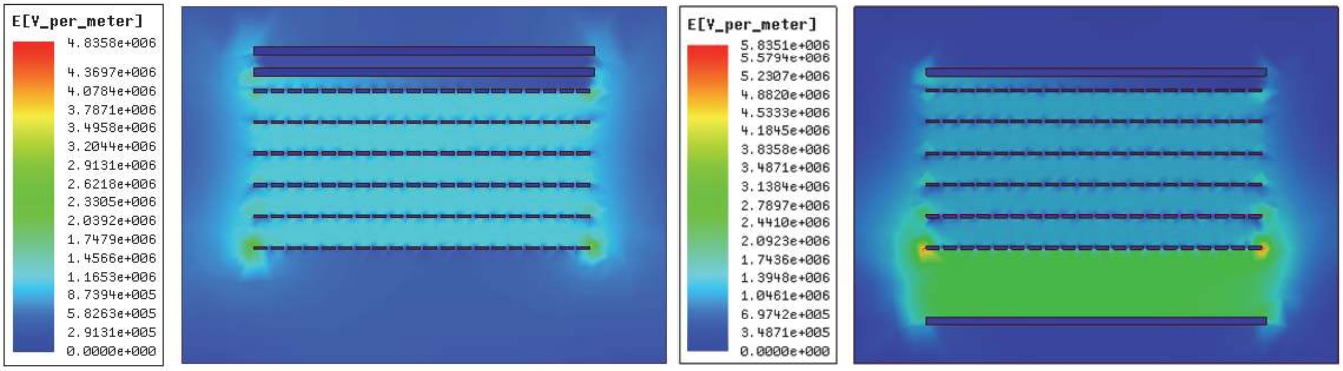


(a) Electric field intensity field distributions of W1 (b) Electric field intensity distributions of W2

Fig. 12 Simulations of the electric field intensity under real working conditions

view, the optimal design result will be different, which means the design of the planar transformer needs tradeoff. In this case, taking all the parasitics into consideration, W_2, which is featured with low L_r, low C_p and low R_{ac} is suitable for high-voltage high-frequency multiple-output applications.

B. Analysis of the partial discharge

Partial discharge is a big issue in high-voltage transformers. In this paper, as the partially interleaved structure is applied, it is necessary to analyze the effect of the partially interleaving on the partial discharge.

Comparison of the partially interleaving and non-interleaving is carried out between W_1 and its corresponding partial interleaved structure W_2. The voltage of each turn under the real working conditions is applied to the corresponding turn, where the input voltage is 40 V, the highest output voltage is 4800 V. The distributions of the electric field intensity are shown in Fig. 12. It should be noted that Fig. 10 shows the AC electric field distribution only while Fig. 12 shows the magnitude of the combined DC and AC electric fields.

It can be seen from Fig. 12 that the highest electric field intensity of W_2 (5.84×10^6 *V/m*) is slightly higher than that of W_1 (4.84×10^6 *V/m*), which is caused by the partially interleaving. However, the highest electric field can be reduced by the increase of the insulation.

As a result, it can be concluded that the partially interleaving will increase the partial discharge. However, the increase in partial discharge can be optimized by increasing the thickness of the insulation.

VII. Experimental Validation

A. Planar transformer for high-voltage high-frequency applications

Based on the above discussion about the comparison of the transformer design, a planar transformer with the partially-interleaved single-layer structure for a 40 V input, 4800 V output LCLC resonant converter was built. The planar transformer uses the same parameters as listed in Table I.

The shape of the core for the planar transformer is FEE 38/16/25 and the material is N87. The planar transformer has one primary winding and six secondary windings. The primary winding has two turns. In order to achieve a partially interleaved structure, one turn is placed at the top of the PCB (P_1) while the other is at the bottom (P_2). The six secondary windings (S_1, S_2, S_3, S_4, S_5 and S_6) are located between the primary winding and each secondary winding has twenty turns with the single-layer structure. As the output voltage increases from S_1 at the top to S_6 at the bottom, which means the voltage of S_1 is the lowest while that of S_6 is the highest, in order to satisfy the requirement of the high-voltage insulation, a thicker insulation is added between secondary winding (S_6) and the bottom primary winding (P_2).

B. Testing of the planar transformer

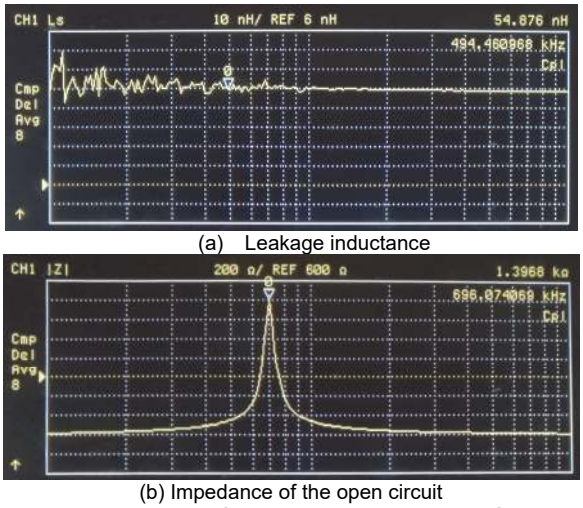
The planar transformer was tested with a HP 4940 impedance analyzer. The test results are shown in Fig. 13.

The L_r is measured from the primary winding with the secondary windings short circuit. It can be seen from Fig. 13(a) that L_r is 54.9 nH, which shows small relative error compared with the calculation result (54.54 nH) and the simulation result (48.04 nH). L_m is 3.9 μH.

When the secondary side is open circuit, as L_r is much lower than that L_m, the resonant frequency between L_m and C_p is measured by the impedance analyzer as shown in Fig. 13(b):

$$f_r = \frac{1}{2\pi\sqrt{L_m C_p}} \tag{13}$$

Where f_r is the resonant frequency, which can be read from the measured result impedance versus frequency results under open-circuit conditions.



(a) Leakage inductance

(b) Impedance of the open circuit

Fig. 13 Test results of the high voltage planar transformer

Therefore, C_p of the planar transformer is found to be

$$C_p = 13.2 \text{ nF} \tag{14}$$

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Fig. 14 Electrical insulation test

The measured C_p shows acceptable relative error compared with the simulation result (11.1 nF) and the calculation result (9.0 nF).

For high-voltage applications, the effectiveness of the high voltage insulation must be tested. The test is carried out between each of the adjacent windings (P and S_1, S_1 and S_2, S_2 and S_3, S_3 and S_4, S_4 and S_5, S_5 and S_6, P and S_6). The voltage excitations applied to the windings are listed in Table VI. The test of the electrical insulation between P and S_6 (highest voltage, 7.5 kV) is shown in Fig. 14.

It can be seen from the current meter that the leakage current is zero, which proves the effectiveness of the electrical insulation.

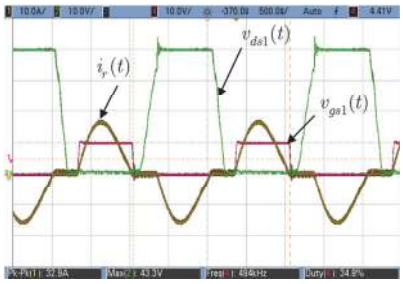
C. Testing of the planar transformer in an LCLC resonant converter

The LCLC resonant converter with fixed-frequency fixed-duty cycle as a DC transformer is widely used in the second stage of a two-stage converter [16]. There are four resonant elements in the resonant tank: L_r, C_s, L_m and C_p. All the transformer parasitics are incorporated into the resonant tank and only C_s is needed.

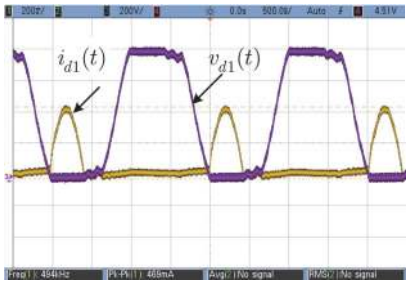
The LCLC resonant converter with the planar transformer is shown in Fig. 15. The input voltage is 40 V, the output of each secondary winding is connected to a voltage doubler to produce 800 V. The outputs of the six voltage doublers are connected in series. As a result, each output of a voltage doubler can be used for a separate load and the maximum output voltage is 4800 V.

The measured waveforms of the resonant current $i_r(t)$, the voltage and the driving signal of S_1 in the LCLC resonant converter with the planar transformer are shown in Fig. 16, where it can be seen that the switching frequency of the converter is 500 kHz.

It can be seen from Fig. 16(a) that when S_1 is turned on, the voltage of S_1 is zero and the resonant current is also zero, therefore, S_1 operations with Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS). The switching loss is minimized. The voltage and current of the rectifier diode D_1 is shown in Fig. 16(b). ZCS and ZVS are also achieved, which will reduce the switching loss.



(a) Measured waveforms of S_1



(b) Measured waveforms of the rectifier D_1

Fig. 16 Measured results

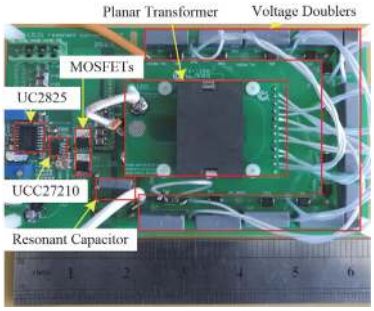


Fig. 15 LCLC resonant converter with a high voltage planar transformer

The efficiency of the converter under different input voltages is tested and is shown in Fig. 17. When the input voltage is 40 V, the input current is 7.35 A, the output is 4800 V, the output current is 59.88 mA, and the load is 80 kΩ, the efficiency is 96.8%.

D. Loss breakdown of the LCLC resonant converter

In this part, the power loss of the LCLC resonant converter is derived based on circuit simulation, including the driving loss (P_{s_dr}), conduction loss of the switches (P_{s_on}), copper loss (P_{T_Cu}), core loss (P_{T_Fe}) and dielectric loss (P_{T_Die}) of the planar transformer and the rectifier loss (P_D).

As for the power loss of the high voltage planar transformer, in addition to the conventional copper loss and core loss, the dielectric loss is also considered in this case. The dielectric loss is caused by the charging and discharging process of the parasitic capacitance. In this case, the power loss factor ($\tan\delta$) of FR4 is 0.01, according to the definition of the power loss factor

$$\tan\delta = 2\pi f_s C_p R_s \tag{15}$$

Where R_s is the equivalent series resistance, f_s is the switching frequency of the capacitance, C_p is the value of the capacitance.

The dielectric loss (P_{T_Die}) can be calculated by

$$P_{T\_Die} = I_{c\_rms}^2 R_s \tag{16}$$

Where I_{c_rms} is the RMS current across the parasitic capacitance, which can be derived from the circuit simulation.

The rectifier loss is calculated by the forward voltage (V_R) times the average current (I_{av}):

$$P_D = V_R I_{av} \tag{17}$$

The total loss (P_{tot}) can be calculated by

$$P_{tot} = P_{S\_dr} + P_{S\_on} + P_{T\_Cu} + P_{T\_Fe} + P_{T\_Die} + P_D \tag{18}$$

The power loss of each part is derived from circuit

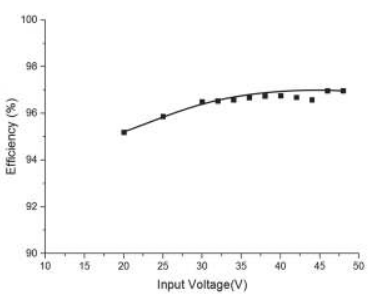


Fig. 17 The efficiency under different input voltage

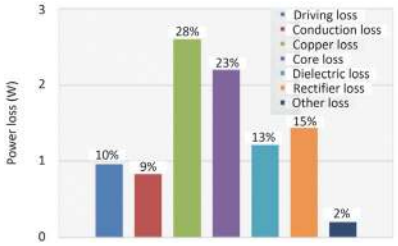


Fig. 18 Loss breakdown of the LCLC resonant converter

simulation and the loss breakdown is shown in Fig. 18. The simulated P_{tot} is 9.24 W while the measured P_{tot} is 9.44 W. It can be concluded that the simulated P_{tot} is in accordance with the measured result.

The power loss of the switches (driving loss and conduction loss) account for 19%, which is relatively high in the total power loss. However, this can be improved by replacing the Silicon MOSFETs by GaN MOSFETs. The power loss of the transformer accounts for 64%, which is the highest in the total loss. As for the dielectric loss, the Polyimide PCB with lower power loss factor, which will contribute to the reduction of the equivalent series resistance, can be used.

According to Table VII, when other winding configurations are compared with W_2, the non-interleaved structures (W_1, W_3 and W_5) will limit the high switching frequency due to higher leakage inductance compared with the partially interleaved structures (W_2, W_4 and W_6). In addition, compared with W_2, W_4 and W_6 will suffer from higher conduction loss and copper loss due to high AC capacitance.

VIII. Conclusions

A partially-interleaved single-layer structure for high-voltage high-frequency multiple-output applications is proposed in this paper. The parasitic capacitance is considered and this transformer structure manages to do the trade-off design among all the parasitic parameters. Based on leakage inductance, AC/DC resistance and AC capacitance, this structure is compared with other five typical structures. Simulations and calculations show that both the leakage inductance and the AC/DC resistance are reduced. In addition, this structure shares almost the same AC capacitance with the non-interleaved single-layer structure.

Besides, a planar transformer with the partially-interleaved single-layer structure is built and tested with the LCLC resonant topology. Compared with the state of the art in TWTA application, by careful design of a planar transformer, leakage inductance is reduced while maintaining inter-winding capacitance within values that ensure ZVS and ZCS, with the result that the switching frequency is increased from less than 100 kHz to 500 kHz without any decrease in efficiency.

Therefore, based on the above analysis, it may be concluded that the partially-interleaved single-layer structure proposed in this paper is suitable for high-voltage high-frequency multiple output applications.

It should be noted that the analysis in this paper considered a particular application, however, due to the improvement in leakage inductance, AC capacitance and AC resistance, the case of partial interleaving would provide similar benefits in other high voltage applications having high step-up and isolation requirements.

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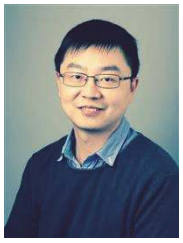

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