An Improved Single-Electron-Transistor Model for SPICE Application

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ABSTRACT

An improved SPICE macro-model based on parameter- and line-fitting method for single electron transistors is proposed in this paper. The proposed model can describe correctly the exponential dependence of I_{ds} on V_{ds} in the Coulomb blockade region as well as Coulomb oscillation in I_{ds}-V_{gs} characteristics of the single electron transistor. The proposed model was applied to a single-electron inverter circuit, and the resulting voltage transfer characteristics agreed closely with the results obtained from the well-accepted Monte-Carlo simulator SIMON 2.0.

1. INTRODUCTION

Single electron transistor (SET) has recently drawn much attention of researchers and scientists due to its potential being one of the elements for future low power, high-density memories and logic circuits [1]. The operation of SET involves only a few electrons and its device characteristics are quite different from those of the conventional metal-oxide-semiconductor (MOS) transistors. Many models based on tunneling and quantum mechanics such as SENECA[2] and MOSES [3] have been developed for SETs in order to gain more insights into the SETs characteristics. The rapid advances in nano-scale fabrication technology expedite the realization of single electron integrated circuits, and there are increasing demands on a compact and accurate SET model for single electron integrated circuits analysis and design. Several compact models [4-6] have been reported in this aspect. In particular, Yu *et al.* proposed a compact SPICE macro-model for SETs [4] according to parameter-based modeling and line-fitting method. In Yu's model, they assumed that the interconnection among SETs is large enough such that each SET can be treated independently and the results they obtained are in good agreement with that from the simulator KOSEC (Korea Single Electron Circuit Simulator) [4]. However, there are large discrepancies between the results obtained from Yu's mode and that from the well-accepted Monte-Carlo SET simulator SIMON [7]. In particular, the drain-source current I_{ds} in Yu's model increases linearly with the drain-source voltage V_{ds} in the Coulomb blockade region. For practical SETs, the I_{ds} should change exponentially with V_{ds} in the Coulomb blockade region. In addition, in Yu's model the base line of I_{ds} increases as gate-source voltage V_{gs} increases in the Coulomb oscillation characteristic of SETs due to leakage current between the gate and the source of SETs. To avoid the above-mentioned disadvantages of Yu's model, we proposed a modified and more accurate SPICE macro-model of SETs. By comparing with the results obtained from SETs simulator SIMON 2.0, our proposed model can described the I_{ds}-V_{ds} characteristics of SETs correctly in both the Coulomb blockade and non-Coulomb blockade regions. Our proposed model predicts more accurate Ids-Vgs Coulomb oscillation characteristic. We also applied our proposed SET model to a single-electron inverter circuit, and the resulting voltage transfer characteristics was in good agreement with the results obtained from SIMON 2.0.

2. SET MACRO-MODELS

The circuit diagram for a SET is shown in Fig. 1, in which a Coulomb island and two tunnel junctions located respectively near the drain and the source of the SET are obvious. The gate of the SET is capacitively coupled to the Coulomb Island. The macro-model proposed by Yu *et al.* consists of a resistor R_G with a large resistance of 100G connected between gate and source, and two branches consisting of the combinations of resistors, diodes and voltages are included between drain and source for the symmetric features of the I_{ds}-V_{ds} characteristics. R_1 is the primary resistor in Coulomb blockade region. R_2 and R_3 are resistors of SET in non-Coulomb blockade region when its drain-source voltage V_{ds} is larger than a certain value in positive and negative direction, respectively. In the real situation, the gate of the SET should be capacitively coupled to and isolated from the Coulomb Island through an isolation junction. Therefore, in our proposed SET macro-model, which is given in Fig. 2, two face-to-face ideal diodes D_4 and D_5, rather than a large resistor R_G, to block all the possible current flows from the gate to the source in the SET. It is noted that I_{ds} should be exponentially dependent on V_{ds} due to tunneling of electron through the tunneling junction [1]. To account for the exponential increase of I_{ds} as a function of V_{ds} inside the Coulomb blockade region, R_1, R_2 and R_3 have to be a function of V_{ds} as well and are modified in our model as follows:

$$R_1(V_G, V_{ds}) = CR1 + CR2[\cos(CF \times \pi \times V_G) + 1] \times 2^{(CV_P - V_{ds}) \cdot x}$$

$$R_2(V_G, V_{ds}) = R_3(V_G, V_{ds}) = \frac{CV_P}{CI_2 - 2CV_P / R_1(V_G, V_{ds})}$$

where the parameter x is a function of temperature. The expressions for CR1, CR2, CF and CV_p are:

$$CR1 = 4R_j$$

$$CR2 = 1.33R_j$$

$$CF = \frac{2C_g}{e}$$

$$CV_P = 0.02$$

Here R_j is the junction tunneling resistance and C_g gate normal capacitance.

3. SIMULATION RESULTS OF TERMINAL CHARACTERISTICS

Figure 3 reveals the simulation results of the shows the simulation results of I_{ds}-V_{gs} characteristics of SETs according to our proposed model for T = 0 °K. The Coulomb oscillation [8] can be clearly seen from this figure. Figure 4 (a) is the comparison of I_{ds}-V_{ds} characteristics obtained from SIMON 2.0, our proposed model and Yu's model for both the Coulomb blockade and non-Coulomb blockade regions. Clearly, our model gives a more accurate result than that of Yu's model when compared with SIMON 2.0. In order to clarify the discrepancy in Yu's model, we re-plotted in Fig. 4 (b) the I_{ds}-V_{ds} characteristics of SETs in Coulomb blockade region for R_j = 100 MΩ, C_j = 1.6aF, C_g = 3.2aF and T = 30°K. We observed that the simulation results obtained from our model matched more closely with that of SIMON 2.0, particularly within the Coulomb blockade region. Since the current flowing from source to drain in a SET depends on the tunneling probability through both the drain tunneling junction and source drain tunneling junction, the drain-source current I_{ds} should be an exponential function of drain-source voltage V_{ds}. However, in Yu's model we see that the I_{ds} varies linearly with V_{ds}. For SIMON 2.0 and our proposed model, the exponential increase in I_{ds} as a function of V_{ds} in the Coulomb blockade region is obvious.

Figure 5 shows the I_{ds} versus gate-source voltage V_{gs} (I_{ds}-V_{gs}) characteristics obtained from SIMON 2.0, Yu's model and our proposed model for T = 30°k, C_g = 3.2aF, C_j = 1.6aF, and R_j = 100M. Coulomb oscillations of I_{ds} as a function of V_{gs} are observed for all the three simulation results. It is clear that the I_{ds}-V_{gs} characteristics obtained from our improved model is much closer to that obtained from SIMON 2.0 when compared with Yu's model. We also noted that in Yu's model the base line of I_{ds} increased as V_{gs} increased because a large resistor R_G was connected between the gate and the source of the SET, and the current flowing between gate and source was added to I_{ds}. In an ideal SET, the isolation junction between the gate and Coulomb Island makes the current flowing from gate to source negligibly small. As was explained previously, in our model two face-to-face diodes rather than a large resistor were used between gate and source of the SET so that no current would flow between them.

4. SIMULATION OF SINGLE-ELECTRON INVERTER

The transfer characteristic of a single electron inverter was simulated. The circuit diagram of the single-electron inverter used for simulation in this work is given in Fig. 6. Figure 7 shows the simulated voltage transfer characteristics obtained from SIMON 2.0, Yu's model and our proposed SPICE model. Large discrepancy exists among the above three simulation results because that for SPICE macro modeling the interconnection is assumed to be large enough so that the neighboring SETs in the circuit are treated independently [4]. On the other hand, for SIMON 2.0 simulation, the charge states of all the Coulomb islands are calculated altogether to take into account of the interaction between neighboring Coulomb islands. Although, the simulation results shown in [4] were in good agreement with that from KOSEC, we found that large discrepancies existed between the simulation results of Yu's model and SIMON 2.0. Using the proposed SPICE model, however, the simulation results matched closely to that from SIMON 2.0. The discrepancy of the voltage transfer characteristics between Yu's model and ours/SIMON 2.0 mainly caused by the large resistor R_G connected between the gate and source in Yu's model and leakage current flows as a result of applying V_{gs} at the gate of the SET.

5. CONCLUSION

In this paper we proposed an improved SPICE macro-model for single electron transistors. By comparing with the well-accepted Mote-Carlo simulator SIMON 2.0, our proposed macro-model can describe correctly the I_{ds}-V_{ds} and I_{ds}-V_{gs} characteristics of SETs as well as the voltage transfer characteristic of the single electron inverter. Under the condition that the interconnections between single-electron transistors are large enough, SPICE macro modeling simulation provides an efficient way for single electron circuits analysis with reasonable accuracy, and those time-consuming calculations needed in Monte-Carlo simulation be avoided.

Acknowledgement

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References:

[1] K.K.Likharev, "Single-electron devices and their

applications," *Proceedings of the IEEE*, Volume: 87 Issue: 4, pp.606 –632, April 1999 ,

[2] L.R.C. Fonseca, A.N. Korotkov, K.K. Likharev, and A.A. Odintsov, " A numerical study of the dynamics and statistics of single electron systems," *J. Appl. Phys.*, vol. 78, pp. 3238-3251, 1995.

[3] R.H. Chen, A.N. Korotkov, and K.K. Likharev, "Single-electron transistor logic," *Appl. Phys. Lett.*, vol. 68, pp. 1954-1956, 1996.

[4] Y.S. Yu, S.W. Hwang, and D. Ahn, "Macromodeling of single-electron transistors for efficient circuit simulation," *IEEE Trans. Eelctron Devices*, 46(8), pp. 1667-1671, 1999.

[5] A. Amakawa, H. Majima, M. Fujisima, and K. Hoh, "single-electron circuit simulation," *IEICE Trans. Electronic*, vol. E81-C , pp.21-29, Jan. 1998.

[6] M. Kirihara, K. Nakazato, and M. Wagner, "Hybrid circuit simulator including a model for single electron tunneling devices," *Jpn. J. Appl. Phys.*, vol. 38, pp. 2028-2032, 1999.

[7] C. Wasshuber, H. Kosina, S. Selberherr, "SIMON-A simulator for single-electron tunnel devices and circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Volume: 16 Issue 9, pp.937-944, Sept. 1997.

[8] Y. Takahashi; A. Fujiwara, Y. Ono, and K. Murase, "Silicon single electron devices and their applications," *Proceedings of the 30th IEEE International Symposium on Multiple-Valued Logic* (ISMVL 2000), pp.411 –420, 2000.

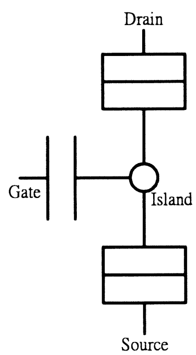


Fig. 1 Circuit diagram for a SET.

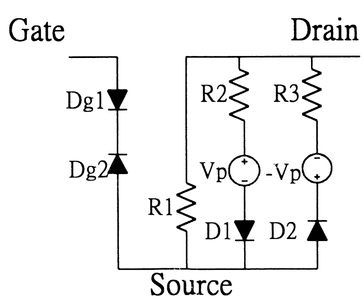


Fig. 2 The proposed SET SPICE macro-model.

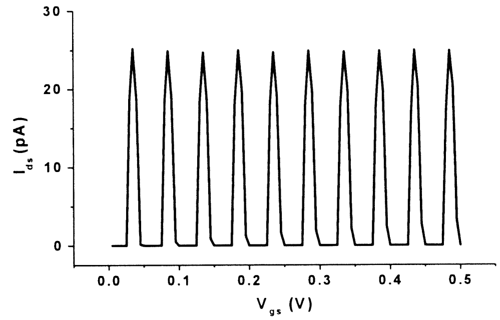
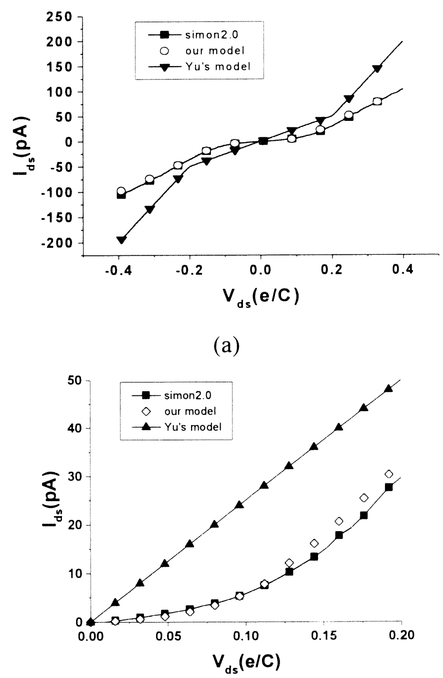


Fig. 3 Simulation results of Coulomb oscillation of I_{ds} as a function of V_{gs} for Cj=1.6af , Cg=3.2af , Rj=100M , Vds=0.01 , T=0k



(b)

Fig. 4. Comparison of I_{ds}-V_{ds} characteristics (a) for both of the Coulomb blockade and non-Coulomb blockade regions, and (b) in Coulomb blockade region obtained from SIMON 2.0, Yu's model and the proposed model under the condition of R_j=100 MΩ, C_j=1.6af, C_g=3.2af and T=30°K.

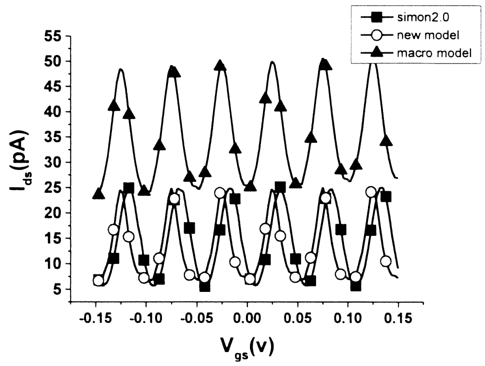


Fig. 5. Simulation results of Coulomb oscillation in I_{ds}-V_{gs} characteristics obtained from SIMON 2.0, Yu's model and the proposed model.

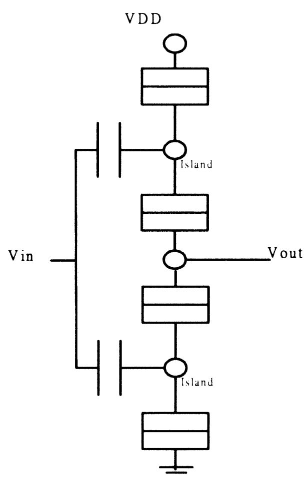


Fig. 6. Circuit diagram for a single-electron inverter.

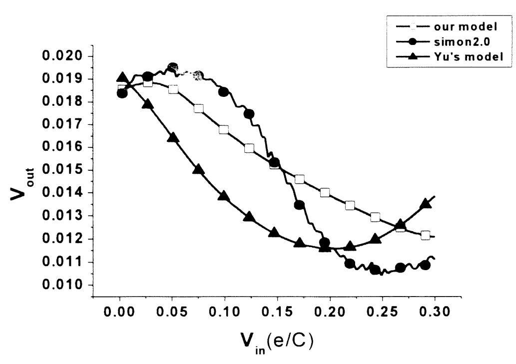


Fig. 7. Simulation Results of the voltage transfer characteristics for a single-electron inverter under the condition of VB = 0.03, Cj = 1.6af, Cg = 3.2af, Rt = 100M, CL = 32af and T = 30 °K.