An Improved Small-Signal Parameter-Extraction Algorithm for GaN HEMT Devices

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***Abstract*—A highly efficient and accurate extraction algorithm for the small-signal equivalent-circuit parameters of a GaN high electron-mobility transistor device is presented. Elements of the extrinsic equivalent-circuit topology are evaluated using a modified "cold field-effect transistor" approach whereby the undesirable need to forward bias the device's gate terminal is avoided. Intrinsic elements are determined based on a circuit topology, which identifies, for the first time, a time delay in the output conductance of GaN-based devices. The validity of the proposed algorithm has been thoroughly verified with excellent correlation between the measured and modeled S-parameters up to 50 GHz.**

***Index Terms*—Gallium nitride (GaN), heterojunction field-effect transistor (HFET), high electron-mobility transistor (HEMT), parameter extraction, small-signal modeling.**

I. Introduction

RECENT publications on GaN-based high electron-mobility transistor (HEMT) technology have demonstrated superior performance capabilities over more traditional GaAs/InP/SiGe-based counterparts [1]–[3]. The large bandgap energy (E_g), typically of the order of 3.4 eV, results in higher breakdown fields ($E_{\rm br} = 4$ MV/cm) permitting much larger voltage swing across the output of the device [4]. Fabrication of the device on a high thermal conductivity (k) substrate [5], e.g., SiC ($k = 4.5$ W/cm $\cdot$ K) will enable improved power-handling capabilities and increased thermal stability under adverse temperature operating conditions [6]. Furthermore, enhanced carrier-confinement processes, whereby both piezoelectric and spontaneous polarizations contribute to the 2-DEG layer formation, induce improved sheet carrier densities in excess of 2×10^{13} e/cm^2 [7] when compared with GaAs, typically 2×10^{12} e/cm^2. Monte Carlo simulations have also predicted saturation velocities of the order of $v_{\rm sat} = 2.5 \times 10^7$ cm/s [8]. Taking all these factors into consideration, GaN-based transistor technologies have undoubtedly become an ideal candidate for high-power and high-frequency microwave circuitries for applications in many areas including aerospace, military, and wireless communications.

Over the last few decades, the development of an accurate device model has proven to be a vital step in the "first-pass" design approach when designing monolithic microwave integrated circuits (MMICs). Models provide a valuable tool for predicting the large-signal performance of a device when simulated with complex modulation schemes like wideband code division multiple access (W-CDMA). An electrical equivalent circuit is one such device model. It provides a means of describing the electrical properties of the device-under-test (DUT) by linking elements of the equivalent circuit directly to the physical structure of the device. Complete characterization of a device's large-signal performance warrants an accurate evaluation of this underlying equivalent circuit under small-signal conditions.

During the last decade, a number of papers have presented different approaches for extracting the small-signal model (SSM) parameters of GaN-based transistors. An LDMOS modeling technique [9] has been proposed for the GaN heterostructure field-effect transistor (HFET) [10], whereby all eight parasitic elements are evaluated solely from the DUT in an off state. However, the present authors are of the view that, for some devices, extraction of the elements of the parasitic network using a single bias state can be problematic. In particular, the data required for series element extraction can be quite noisy and certain network parameters may exhibit an undesirable dependence with frequency. A 22-element distributed model proposed in [11] requires the estimation of initial element values for a bi-directional optimization technique. However, the process of acquiring these initial estimates involves the use of several empirical and algebraic assumptions, which may not suit all device structures. A low gate bias model extraction technique [12] has demonstrated an efficient SSM evaluation. All elements are determined without forward biasing the gate of the device. Nonetheless, the procedure can only be applied to devices where the equivalent drain–source capacitance $C_{\rm ds}$ is negligible. As will be highlighted in this paper, $C_{\rm ds}$ is, in general, not negligible and can be particularly high under certain cold field-effect transistor ("cold-FET") bias conditions. The existence of a significant $C_{\rm ds}$ effect has been addressed in a recent GaN "cold-FET" extraction approach [13]. In spite of this, an iterative procedure is required to determine a suitable forward biasing condition that is high enough to suppress the channel resistance, but low enough not to cause significant current flow through the gate terminal that could otherwise permanently degrade the future performance of the device. Furthermore, a certain level of modeling experience is required to identify the appropriate frequency ranges over which the Z-parameters can be used to evaluate the parasitic resistances.

Several publications [14], [15] have identified the existence of time delays in the output conductance element $(g_{\rm ds})$ of

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the standard small-signal equivalent circuit of FET devices. Without modifications to the conventional intrinsic circuit topology [16], this feature can be misinterpreted as bias-dependant drain and source access resistances. In extreme cases, these resistances may even appear negative [14], the plausibility of which is questionable from a physical point-of-view, while they can also create problems with implementation in simulators. The increased phase delay in $g_{\rm ds}$ at higher frequencies has been attributed to this phenomenon [17]. Based on this observation, an additional time dependence has been introduced into the $g_{\rm ds}$ element of a conventional equivalent circuit [18], [19]. In this study, similar phase delays in $g_{\rm ds}$ are identified for the first time in GaN-based HEMTs. Utilizing the circuit topology proposed in [18] issues regarding the physical consistency of the extracted access resistances are resolved.

A complete extraction procedure of all equivalent-circuit elements in a GaN HEMT device is presented in this paper. All extrinsic parasitic elements are evaluated under "cold-FET" conditions without forward biasing the gate terminal, as there is no requirement for the channel resistance to be small. Using a straightforward optimization procedure and utilizing a selection of well-established analytical expressions, values for the intrinsic equivalent-circuit elements can be accurately determined. The robustness and efficiency of this novel approach clearly distinguishes this study from previous extraction methodologies. This is demonstrated by the fact that elements are determined in a step-by-step noniterative procedure, which requires minimal intervention or experience on the part of the model developer. The validity of the proposed small-signal modeling methodology is discussed and the reliability of the evaluated SSM parameters is rigorously demonstrated.

II. Device Structure

The SSM has been determined for an AlGaN/GaN HEMT transistor fabricated at QinetiQ Ltd., Hampshire, U.K. It consists of a double cell "pi" structure with a 0.29-μm gate length, as measured by focused ion beam cross sectioning. The gate metallization is a "T profile" in order to minimize the parasitic gate resistance. The total gatewidth is 100 μm, consisting of two unit gatewidths of 50 μm, and the gate-to-drain spacing is approximately 1.8 μm. The layer structure consists of 28-nm AlGaN (26%), $\approx$1 nm of aluminum nitride (AlN), and 1.2-μm insulating GaN on a 4-H vanadium-doped silicon carbide (SiC) substrate. The AlN layer has the effect of increasing the mobility and is expected to reduce real space transfer into the AlGaN layer at high electric fields [20].

III. Extraction Procedure

The complete small-signal circuit proposed for this device is shown in Fig. 1. Lumped components of the intrinsic topology represent the first-order linearization of nonlinear elements in the equivalent-circuit model including a pair of parallel current sources. Both of these are derived from a single nonlinear current source, the first representing a standard transconductance, whereas the second represents a generalized conductance with possible delay. Time delays, indicative of the observed frequency dependence in each of these conductances, are specified with reference to the intrinsic terminal voltages, as depicted in Fig. 1. The extrinsic parasitics include bias-independent elements R_g, R_d, R_s, $C_{\rm pg}$, $C_{\rm pd}$, L_g, L_d, and L_s. Assuming that the parasitics are evaluated and deembedded correctly, the remaining bias-dependant intrinsic elements can be evaluated using both the analytical expressions presented in [16] plus the straightforward fitting routine described in this paper. The following outlines the novel procedure for the correct extraction of the entire set of circuit elements.

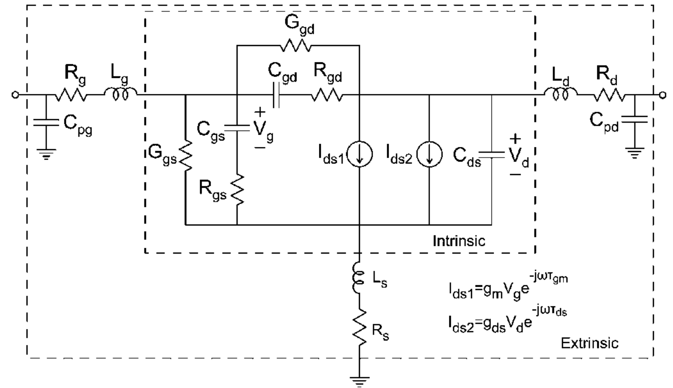


Fig. 1. Complete small-signal equivalent circuit for a GaN HEMT including intrinsic and extrinsic circuit topologies.

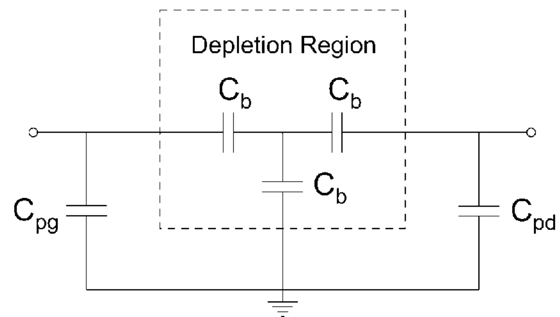


Fig. 2. Reduced equivalent-circuit topology for a "pinched-off" GaN HEMT.

A. Parasitic Pad Capacitance Extraction

Parasitic gate and drain pad capacitances of GaN HEMT are generally extracted from conventional "cold-FET" techniques, $V_{\rm DS} = 0.0$ V, using S-parameter measurements below pinched-off bias conditions, namely, $V_{\rm GS} < V_p$. Under these conditions, channel conductivity is negligible and the now passive device exhibits a purely capacitive behavior under low to medium frequencies [21]. For our GaN HEMT, under the pinchoff bias of $V_{\rm GS} = -8.0$ V, the equivalent-circuit topology of Fig. 2 was deemed to be an adequate electrical representation of the device in this bias state [9]. The star-connected network of gate capacitance elements C_b exploits the symmetrical behavior of the depletion capacitance under the gate [22]. Linear regression fits to the various algebraic Y-parameter quantities,

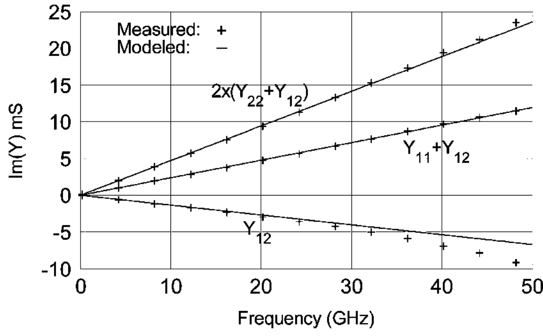


Fig. 3. Measured and modeled Y-parameters (0.2–50 GHz) for a 2 × 50 μm GaN HEMT under a "cold-FET" bias condition of $V_{\rm GS} = -8.0$ V and $V_{\rm DS} = 0.0$ V.

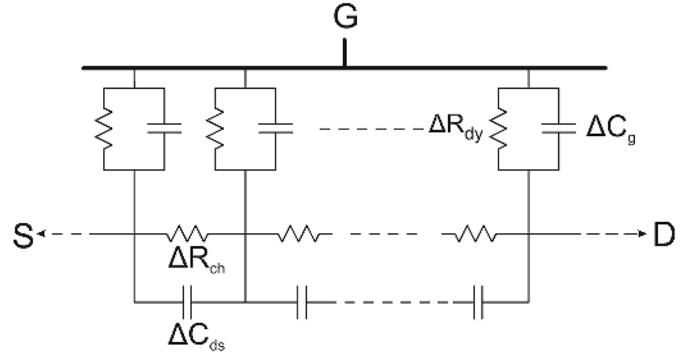


Fig. 4. Distributed gate network for a 2 × 50 μm GaN HEMT under open channel bias condition of $V_{\rm GS} = 0.0$ V and $V_{\rm DS} = 0.0$ V.

TABLE I
EXTRACTED "COLD-FET" PINCHED-OFF ELEMENTS

C_{pg} (fF)	C_{pd} (fF)	C_b (fF)
16.63	16.18	64.03

as illustrated in Fig. 3, provide values for the individual elements according to the following mathematical expressions:

$$\mathrm{Im}(Y_{12}) = -\omega \frac{C_b}{3} \tag{1}$$

$$\mathrm{Im}(Y_{11} + Y_{12}) = \omega \left(C_{\rm pg} + \frac{C_b}{3} \right) \tag{2}$$

$$\mathrm{Im}(Y_{22} + Y_{12}) = \omega \left(C_{\rm pd} + \frac{C_b}{3} \right). \tag{3}$$

As one can see, the highly linear behavior of the measured admittances justifies the reduced circuit topology of Fig. 2 over the lower frequency band. The extracted capacitances are presented in Table I.

It may be noted that a possible parasitic feedback capacitance between the gate and drain terminals has been omitted in the circuit of Fig. 2. In fact, based on geometrical data, estimates of this capacitance indicate values that are a factor of ten down on the pad capacitances, thereby permitting its omission from the equivalent circuit of Fig. 1, and subsequently, Fig. 2. This assumption will be further justified by the observed frequency independence of the extracted intrinsic parameters presented later in this paper. Furthermore, the authors acknowledge that the assumption of intrinsic symmetries, as inferred by Fig. 2, does not necessarily hold for all devices [23]. Certain device structures may also exhibit nonnegligible feedback capacitances [24]. A more generalized extraction approach would be to utilize open dummy structures, as demonstrated on the GaN HEMT in [12] and [13]. However, such structures were not available to the present authors, but techniques of this type should be used whenever these structures are available.

B. Parasitic Inductance and Resistance Extraction

Having evaluated the parasitic pad capacitances, an accurate means of characterizing the series access regions of the device was sought. Under open channel conditions, a distributed *RC* network has been proposed to characterize the electrical behavior of an FET device [25]. However, this model fails to account for any drain–source capacitance associated with the channel, arising from the separation of high electron concentration access regions at the drain and source [17]. Under low $V_{\rm DS}$ bias conditions, this separation becomes small and, thus, a significant increase in $C_{\rm ds}$ at $V_{\rm DS} = 0.0$ V can be expected. Therefore, a more suitable distributed circuit topology is proposed, as illustrated in Fig. 4. Here, $\Delta R_{\rm ch}$ and $\Delta C_{\rm ds}$ represent the distributed elements of the drain–source channel resistance and capacitance, respectively, while ΔC_g and ΔR_{dy} account for the equivalent impedance under the Schottky barrier, as described by Dambrine *et al.* in [25]. From transmission line theory, the impedance matrix of this two-port network is given by

$$Z = \begin{bmatrix} \dfrac{Z_0}{\tanh(\gamma L)} & \dfrac{Z_0(\cosh(\gamma L) - 1)}{\sinh(\gamma L)} \\ \dfrac{Z_0(\cosh(\gamma L) - 1)}{\sinh(\gamma L)} & \dfrac{2Z_0(\cosh(\gamma L) - 1)}{\sinh(\gamma L)} \end{bmatrix}. \tag{4}$$

Z_o represents the characteristic impedance and γL is the product of the transmission line coefficient and gate length of the gate's equivalent transmission line network. These quantities can be determined from an analysis of the distributed equivalent circuit of Fig. 4, and are given by the following:

$$Z_0 = \sqrt{\frac{R_{\rm ch}//C_{\rm ds}}{G_{dy} + j\omega C_g}} \tag{5}$$

$$\gamma L = \sqrt{(R_{\rm ch}//C_{\rm ds})(G_{dy} + j\omega C_g)} \tag{6}$$

where $G_{dy} = (R_{dy})^{-1}$. Under microwave frequencies $|(\gamma L)^2| \ll 1$ and, thus, the equivalent intrinsic impedance matrix simplifies to the following:

$$Z = \begin{bmatrix} \dfrac{\frac{1}{3}R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} + \dfrac{R_{dy}}{1 + j\omega C_g R_{dy}} & \dfrac{\frac{1}{2}R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} \\ \dfrac{\frac{1}{2}R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} & \dfrac{R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} \end{bmatrix}. \tag{7}$$

Deembedding the extracted pad capacitances from the equivalent circuit of Fig. 1, the complete Z-parameter representation

of the measured device, under unbiased "cold-FET" conditions, becomes

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s) + \frac{\frac{1}{3}R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} + \frac{R_{dy}}{1 + j\omega C_g R_{dy}} \tag{8}$$

$$Z_{12} = R_s + \frac{\frac{1}{2}R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} + j\omega L_s \tag{9}$$

$$Z_{22} = R_d + R_s + \frac{R_{\rm ch}}{1 + j\omega C_{\rm ds} R_{\rm ch}} + j\omega(L_d + L_s). \tag{10}$$

Previous extraction methodologies [26], [27] that avoid the forward gate biasing techniques describe a similar set of equations for the DUT, though without the apparent complication of the drain–source capacitance $C_{\rm ds}$, as shown in (8)–(10). Therefore, with reference to (8)–(10), the direct extraction approach for the remaining parasitic elements can no longer be applied here. However, the interaction of $C_{\rm ds}$ in parallel with the channel resistance introduces a favorable dispersive behavior into the measured series resistances. Therefore, despite increasing the complexity of the analysis, $C_{\rm ds}$ effectively permits the distinction of the channel resistance from the parasitic resistances, as can be mathematically inferred from (8)–(10). Hence, by incorporating this system of equations into a least squares (LS) fitting routine, one can evaluate unique and consistent values for the remaining parasitic elements. The general error function of such an LS fitting routine is given by

$$E_{xy}\big|_{\substack{x=1,2\\ y=1,2}} = \sum_i^N \left\{ \left[\mathrm{Re}\left(Z_{xy}^{\rm sim}(\omega_i) - Z_{xy}^{\rm meas}(\omega_i)\right)\right]^2 + \left[\mathrm{Im}\left(Z_{xy}^{\rm sim}(\omega_i) - Z_{xy}^{\rm meas}(\omega_i)\right)\right]^2 \right\}. \tag{11}$$

The following algorithm now details each step of the proposed novel extraction procedure.

Step 1) To improve the efficiency of the LS fitting process, individual impedance elements of the Z_{22}-parameter can be estimated as follows:

$$R_{\rm ch} \approx \mathrm{Re}(Z_{22}|_{f_L} - Z_{22}|_{f_H}) \tag{12}$$

$$R_d + R_s \approx \mathrm{Re}(Z_{22}|_{f_H}) \tag{13}$$

$$C_{\rm ds} \approx \frac{1}{\omega_M R_{\rm ch}} \left(\frac{R_{\rm ch}}{\mathrm{Re}(Z_{22}|_{f_M} - Z_{22}|_{f_H})} - 1 \right)^{\frac{1}{2}} \tag{14}$$

$$L_d + L_s \approx \frac{1}{\omega_H} \mathrm{Im}\left(Z_{22}|_{f_H} - \frac{R_{\rm ch}}{1 + j\omega_H C_{\rm ds} R_{\rm ch}} \right) \tag{15}$$

where $\omega = 2\pi f$ and quantities subscripted with L, M, and H denote parameters measured at the lowest, intermediate, and highest frequencies of 0.2, 25.0 and 50.0 GHz, respectively. The estimates given by (12)–(14) are based on an analysis of the real parts of Z_{22}, which are dominated by the interaction of $C_{\rm ds}$ with the channel resistances $R_{\rm ch}$ over the entire measured frequency range. At the highest frequencies, both the drain inductance L_d and source inductances L_s begin to dominate the imaginary part of the measured series impedance and are appropriately estimated by (15). An LS fit of (10) to the measured complex Z_{22}-parameter over the measured frequency range reveals the optimum values of these estimated quantities. Table II outlines values for both the estimated and fitted quantities for this step. A comparison of the measured and modeled results of both the real and imaginary components of Z_{22} is given in Fig. 5. This graph also highlights the significant reduction in the measured series output resistance over frequency due to $C_{\rm ds}$, as described earlier. The fitted $R_{\rm ch}$ and $C_{\rm ds}$ values can now be fixed for the remainder of the extraction process.

TABLE II
EXTRACTED Z_{22}-PARAMETERS

Parameter	R_{ch} (Ω)	R_d+ R_s (Ω)	L_d+L_s (pH)	C_{ds} (pF)
Estimated	6.02	20.52	40.55	1.42
Fitted	9.34	17.16	49.53	0.45

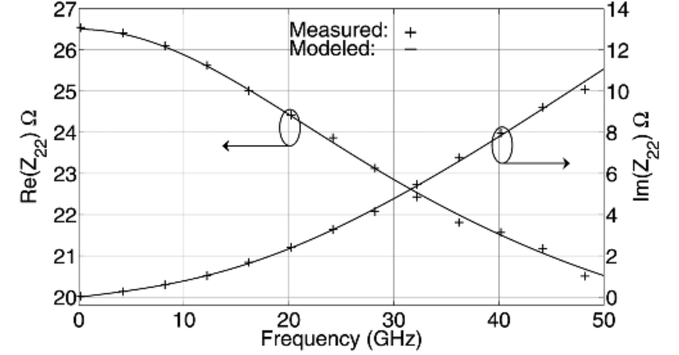


Fig. 5. Measured and modeled real and imaginary parts of the Z_{22}-parameter (0.2–50 GHz) for an unbiased "cold-FET" 2 × 50 μm GaN HEMT.

Step 2) The source resistance R_s and source inductance dominate the real and imaginary parts of Z_{12} at the highest frequencies and can be estimated as follows:

$$R_s \approx \mathrm{Re}(Z_{12}|_{f_H}) \tag{16}$$

$$L_s \approx \frac{1}{\omega_H} \mathrm{Im}\left(Z_{12}|_{f_H} - \frac{\frac{1}{2}R_{\rm ch}}{1 + j\omega_H C_{\rm ds} R_{\rm ch}} \right). \tag{17}$$

A similar LS fit of (9) to the measured complex Z_{12}-parameter reveals the final values of these quantities. The estimated and fitted values are given in Table III. Furthermore, a comparison of the measured and modeled Z_{12}-parameter for this step is shown in Fig. 6.

TABLE III
EXTRACTED Z_{12}-PARAMETERS

Parameter	R_s (Ω)	L_s (pH)
Estimated	8.01	2.01
Fitted	6.17	4.23

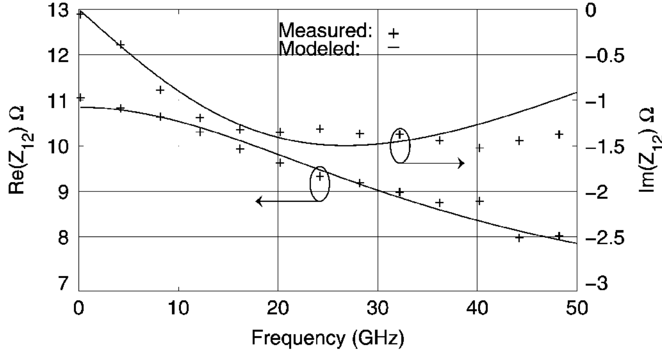


Fig. 6. Measured and modeled real and imaginary parts of the Z_{12}-parameter (0.2–50 GHz) for an unbiased "cold-FET" 2 × 50 μm GaN HEMT.

TABLE IV
EXTRACTED Z_{11}-PARAMETERS

Parameter	R_g+R_s (Ω)	R_{dy} (kΩ)	L_g+L_s (pH)	C_g (fF)
Estimated	10.0	9.16	44.76	144.0
Fitted	7.78	10.62	48.07	139.2

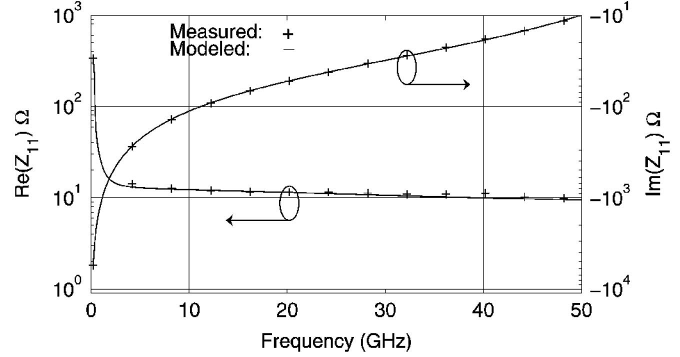


Fig. 7. Measured and modeled real and imaginary parts of the Z_{11}-parameter (0.2–50 GHz) for an unbiased "cold-FET" 2 × 50 μm GaN HEMT.

Step 3) Finally, estimates of the equivalent impedance parameters of the Z_{11}-parameter are made as follows:

$$C_g \approx -\frac{1}{\omega_L}\text{Im}\left(Z_{11}|_{f_L} - \frac{\frac{1}{3}R_{\text{ch}}}{1+j\omega_L C_{\text{ds}}R_{\text{ch}}}\right)^{-1} \tag{18}$$

$$R_{dy} \approx \frac{1}{(\omega_L C_g)^2}\text{Re}\left(Z_{11}|_{f_L} - \frac{\frac{1}{3}R_{\text{ch}}}{1+j\omega_L C_{\text{ds}}R_{\text{ch}}}\right)^{-1} \tag{19}$$

$$R_g + R_s \approx \text{Re}(Z_{11}|_{f_H}) \tag{20}$$

$$L_g + L_s \approx \frac{1}{\omega_H}\text{Im}\left(\begin{array}{c} Z_{11}|_{f_H} - \dfrac{\frac{1}{3}R_{\text{ch}}}{1+j\omega_H C_{\text{ds}}R_{\text{ch}}} \\ -\dfrac{R_{dy}}{1+j\omega_H C_g R_{dy}} \end{array}\right). \tag{21}$$

Under the lower frequencies, the complex impedances presented by the gate leakage resistance R_{dy} and gate capacitance C_g are prevalent. Using the fitted R_{ch} and C_{ds} values from Step 1) and rearranging (8), reasonable estimates of these intrinsic parameters are made according to (18) and (19). Series gate parasitics begin to dominate the measured impedances at the highest frequencies and are estimated according to (20) and (21). A final LS fit of the complex Z_{11}-parameter to (8) provide the optimum values for these quantities, the results of which are shown in Table IV. A graph of this fit is presented on a log scale in Fig. 7 to clearly highlight the outstanding correlation between the measured and modeled results over the measured frequency range.

TABLE V
EXTRACTED SERIES PARASITIC ELEMENTS

L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
43.85	45.30	4.23	1.60	10.98	6.17

At this stage, all the data required for the complete characterization of the device's parasitic network has been obtained. Where necessary, values for each individual parasitic element can be determined by performing algebraic operations on the fitted data from Tables II–IV. Table V now outlines the final values for each individual parasitic element, which will be used to determine the measured intrinsic parameters of the device.

C. "Hot-FET" Intrinsic Element Extraction

Values determined for the extrinsic elements can be deembedded from the measured data by a series of straightforward mathematical operations to reveal the measured intrinsic Y-parameters of the device [25]. Traditionally, equations described in [16] can be used to determine the remaining elements of the intrinsic circuit [26]–[28]. However, the introduction of the drain conductance delay parameter gives an overdetermined system of equations. This problem is depicted in the general equivalent circuit of Fig. 8, which is a simplified form of the intrinsic topology described in Fig. 1. Mathematically unique values can be extracted for a maximum of two intrinsic elements or parameters from each admittance quantity at each measured frequency. This is not so in the case of Y_{ds}, which is now described in terms of three parameters as follows:

$$Y_{\text{ds}} = g_{\text{ds}}\exp(-j\omega\tau_{\text{ds}}) + j\omega C_{\text{ds}}. \tag{22}$$

Therefore, a final fitting routine to (22) is required to evaluate the equivalent values of these parameters at each bias point.

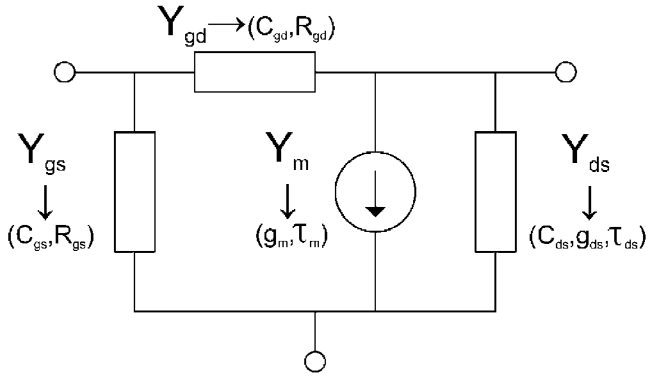


Fig. 8. Generalized equivalent intrinsic topology of a GaN HEMT device showing the lumped complex admittance quantities in each limb and their associated equivalent-circuit parameters.

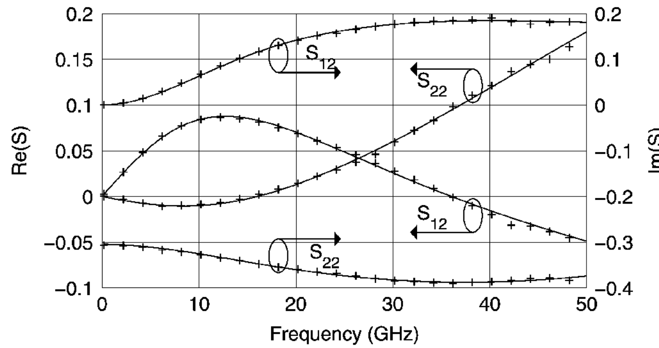


Fig. 9. Real and imaginary parts of the measured (+) and modeled (−) S-parameters (0.2–50 GHz) for 2×50 μm GaN HEMT at $V_{\rm GS} = 0.0$ V and $V_{\rm DS} = 0.0$ V.

Having outlined a detailed algorithm for extracting the SSM of a GaN HEMT, Section IV will now provide a thorough validation of this proposed approach.

IV. Results and Discussion

In Section III, the extraction algorithm for the extrinsic parasitics under "cold-FET" conditions was presented. To evaluate the accuracy of the extracted parasitic elements, Figs. 9 and 10 now compare a selection of the measured and modeled S-parameters of the device under both of these "cold-FET" bias conditions. Real and imaginary components of these quantities are plotted separately to highlight the excellent correlation between the measured and modeled results over the measured frequency range. These results provide a good indication of the accuracy of the extracted parasitic values thus far.

Deembedding all bias independent parasitic components from the measured data, the intrinsic elements were then determined under active multibias conditions. In the case where elements could be evaluated by direct analytical expressions, their unique values were determined over the entire measured frequency range. A selection of these elements extracted over frequency for two different bias points is shown in Figs. 11 and 12. Ignoring measurement errors, it is quite apparent that the extracted elements exhibit clear frequency independence over the measured frequency range. Similar results were observed for the majority of bias points across the bias plane. This result further validates both the chosen topology and the accuracy

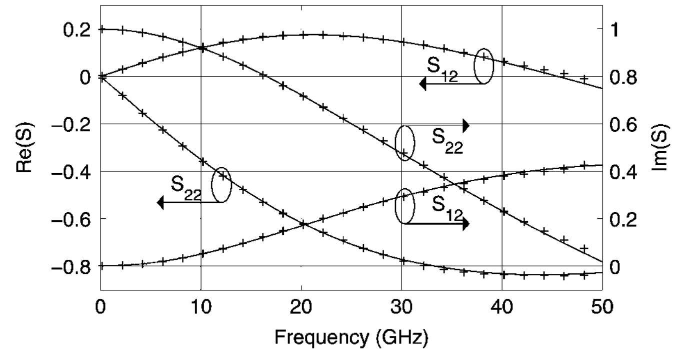


Fig. 10. Real and imaginary parts of the measured (+) and modeled (−) S-parameters (0.2–50 GHz) for 2×50 μm GaN HEMT at $V_{\rm GS} = -8.0$ V and $V_{\rm DS} = 0.0$ V.

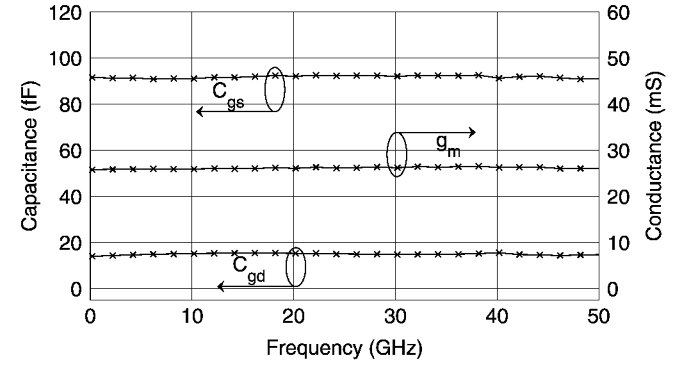


Fig. 11. Extracted intrinsic elements of $C_{\rm gs}$, $C_{\rm gd}$, and g_m versus frequency (0.2–50 GHz) for a 2×50 μm GaN HEMT at $V_{\rm GS} = -0.6$ V and $V_{\rm DS} = 12.5$ V.

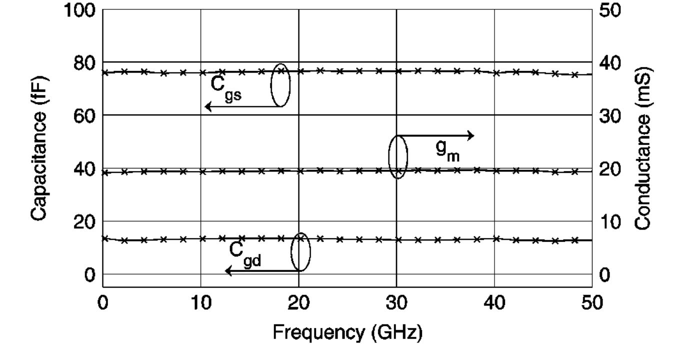


Fig. 12. Extracted intrinsic elements of $C_{\rm gs}$, $C_{\rm gd}$, and g_m versus frequency (0.2–50 GHz) for a 2×50 μm GaN HEMT at $V_{\rm GS} = -7.0$ V and $V_{\rm DS} = 20.0$ V.

of the proposed extraction technique. The real and imaginary parts of $Y_{\rm ds}$ for these bias points are also shown in Figs. 13 and 14, highlighting the appropriateness of the output conductance time delay approach.

To verify the small-signal behavior of the model, the proposed circuit topology of Fig. 1 was simulated with the extracted values determined using this novel procedure for our GaN HEMT. Table VI outlines a selection of the extracted values for three different bias points over the range of $V_{\rm GS}$ (−5–0 V). The ability of the model to accurately reproduce the measured data at these varying bias extremes is demonstrated in Fig. 15. Calculation of the error between the measured and

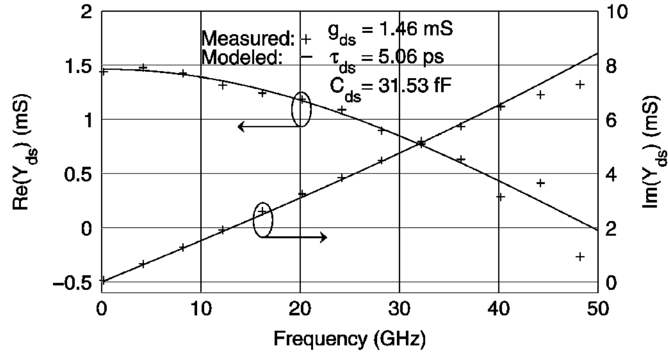


Fig. 13. Measured (+) and modeled (−) intrinsic output conductance $Y_{\rm ds}$ (0.2–50 GHz) and associated fitting parameters of $g_{\rm ds}$, $\tau_{\rm ds}$, and $C_{\rm ds}$ for a 2×50 μm GaN HEMT at $V_{\rm GS} = -6.0$ V and $V_{\rm DS} = 12.5$ V.

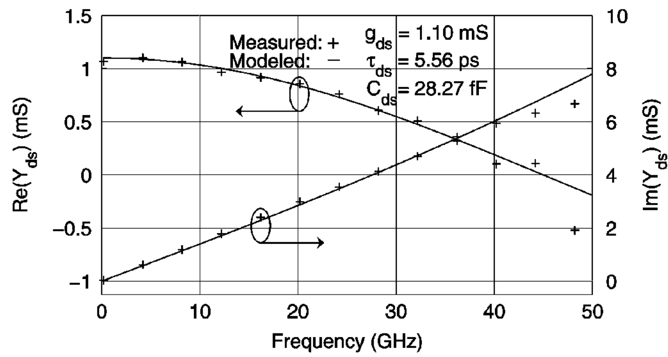


Fig. 14. Measured (+) and modeled (−) intrinsic output conductance $Y_{\rm ds}$ (0.2–50 GHz) and associated fitting parameters of $g_{\rm ds}$, $\tau_{\rm ds}$, and $C_{\rm ds}$ for a 2×50 μm GaN HEMT at $V_{\rm GS} = -7.0$ V and $V_{\rm DS} = 20.0$ V.

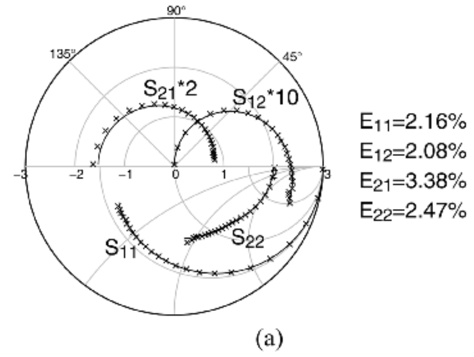
TABLE VI
EXTRACTED INTRINSIC ELEMENTS FOR 2×50 μm GaN HEMT

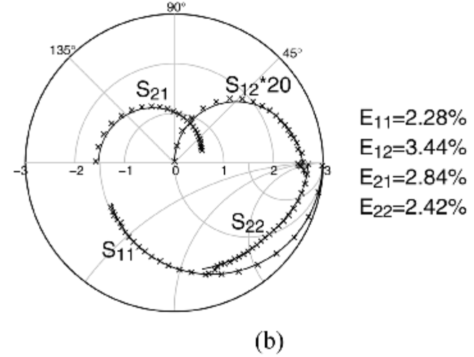
	V_{GS} = 0.0 V V_{DS} = 8.0 V	V_{GS} = -3.0V V_{DS} = 20.0 V	V_{GS} = -5.0 V V_{DS} = 6.0 V
C_{gs} (fF)	101.0	120.0	103.0
R_{gs} (Ω)	16.4	12.2	3.4
C_{gd} (fF)	32.0	13.0	19.0
R_{gd} (Ω)	53.8	145.0	54.0
g_m (mS)	11.0	18.8	26.3
τ_{gm} (ps)	1.01	1.53	0.82
g_{ds} (mS)	4.69	1.25	2.23
τ_{ds} (ps)	3.59	5.71	4.9
C_{ds} (fF)	36.0	31.0	38.6
G_{gs} (μS)	4.25	40.57	7.86
G_{gd} (μS)	1.62	3.80	5.11

modeled results is determined from the following generalized error expression [29]:

$$\%E_{xy}\Big|_{\substack{x=1,2\\ y=1,2}} = 100 \times \sqrt{\frac{\sum_M \sum_N \left|S_{xy}^{\rm sim} - S_{xy}^{\rm meas}\right|^2}{\sum_M \sum_N \left|S_{xy}^{\rm meas}\right|^2}}. \tag{23}$$

where M and N denote the number of bias and frequency points, respectively.





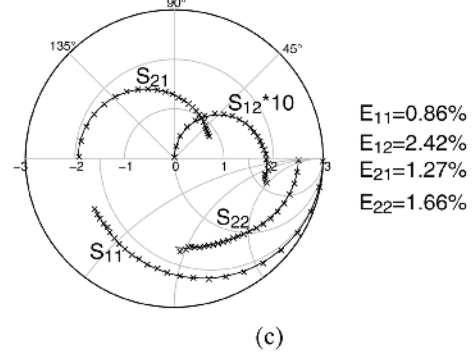


Fig. 15. Measured (×) and modeled (−) S-parameters (0.2–50 GHz) for 2×50 μm GaN HEMT for bias points (a) $V_{\rm GS} = 0.0$ V and $V_{\rm DS} = 8.0$ V, (b) $V_{\rm GS} = -3.0$ V and $V_{\rm DS} = 20.0$ V and (c) $V_{\rm GS} = -5.0$ V and $V_{\rm DS} = 6.0$ V.

In Fig. 16, the variation of all intrinsic parameters over the bias plane is presented, in particular, the drain–source capacitance $C_{\rm ds}$ in Fig. 16(c). In saturation the high-field channel region extends towards the drain, separating the highly doped source and drain access regions in an electrostatic sense, and a resulting $C_{\rm ds}$ develops [30]. Under decreasing $V_{\rm DS}$ bias and increasing $V_{\rm GS}$ bias, this separation becomes smaller, thus reducing this separation and giving rise to a sudden spike in the extracted $C_{\rm ds}$, particularly around $V_{\rm GS} = 0.0$, as shown. In retrospect, the behavior of the extracted $C_{\rm ds}$ around the "cold-FET" bias point of $V_{\rm GS} = 0.0$ V and $V_{\rm DS} = 0.0$ V highlights the requirement of the improved extraction methodology presented in this paper. The extracted capacitance at this bias is of the order of 15 times the magnitude of that extracted in the saturation region and, thus, its inclusion in the presented distributed topology of Fig. 4 is well justified. Overall, the behavior of the all-extracted elements is generally smooth over the bias plane, which

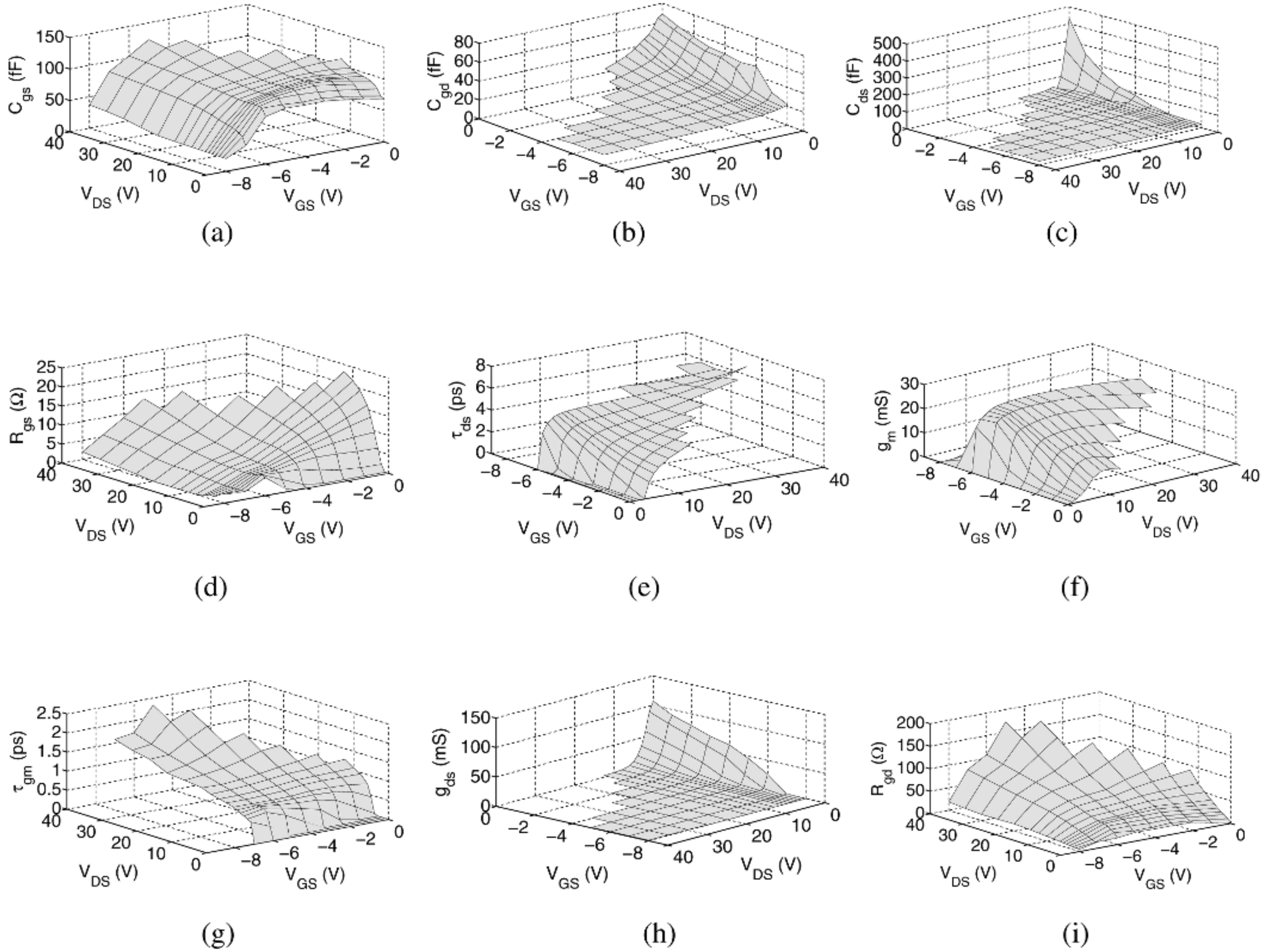


Fig. 16. Extracted intrinsic elements for 2×50 μm GaN HEMT over the measured bias plane.

is a favorable feature tending to verify the reliability of values determined by optimization-based extractions. These results are also consistent with those presented in previous publications on similar devices [11], [13].

A physical explanation of the drain time delay can be inferred from an analysis of its behavior over the bias plane. At biases exceeding the saturation voltage, the edges of the depletion layer are no longer largely confined to the region beneath the gate contact. In particular, the drain side of the depletion region extends steadily toward the drain terminal under increasing drain voltage. Correspondingly, a similar monotonic increase in the extracted drain delay can be observed in Fig. 16(e). Hence, one can postulate that it represents a delay in the drain current's response to the drain voltage arising from delays associated with the partially depleted high-field region. This essentially constitutes a transmission line effect, which, from a compact equivalent-circuit point-of-view, justifies the form of (22). Nonetheless, a more detailed explanation, particularly from researchers within the physical modeling community, may be warranted. The effectiveness of $\tau_{\rm ds}$, in terms of modeling accuracy, can be demonstrated by a comparison of the error in S_{22} with and without its inclusion in the circuit of Fig. 1. Applying (23) to all the measured and modeled S_{22}-parameters across the entire bias plane, the authors have found that the error is reduced from 11.2% down to 3.5%.

Several accounts have detailed bias dependencies in the access resistances R_d and R_s of GaN-based transistors [31], [32]. Their importance and subsequent impact on the linearity performance in terms of the measured transconductance and cutoff frequency has been demonstrated [33], [34]. It should be noted that the access resistances extracted for this device were bias independent. The values determined under "cold-FET" conditions were found to be highly sufficient in reproducing the measured S-parameters of our device. Furthermore it is quite clear from Figs. 11 and 12 that the extracted intrinsic elements remained independent of frequency over the active bias plane. This is a clear indication of the accuracy of the model parasitics and, therefore, the use of bias-independent access resistances appears to be well founded. Although it can be argued that the inclusion of a time delay in the output conductance could be "masking" nonlinearities in the access resistances, the authors found that its omission resulted in negative resistances, which is both incon-

sistent with device physics and unsuitable for implementation in large-signal simulation environments.

The efficiency of the proposed extraction algorithm is demonstrated by the fact the entire small-signal performance of the device across the *I–V* plane (125 bias points) was determined in under 30 s. The accuracy and closeness of the parameter estimates, as highlighted in Tables II–IV, and the overall systematic approach of the extraction procedure contributes to its efficiency. Simulations were performed in a MATLAB simulation environment on a 1.65-GHz computer.

Our technique has recently been applied to another $2 \times 50\ \mu$m GaN HEMT from a separate development process. Modeling accuracy, comparable to that presented in this paper, has been observed for this device including identification of almost identical delay phenomena in the output conductance. Straightforward scaling rules, similar to those proposed in [35], have permitted the extension of the proposed extraction methodology to wider device structures. Preliminary fitting results from a $2 \times 125\ \mu$m GaN HEMT have been very promising, indicating the robustness of the proposed extraction methodology.

V. Conclusion

A highly accurate and robust small-signal parameter extraction algorithm has been presented for a $2 \times 50\ \mu$m GaN HEMT device. All parasitics have been evaluated using traditional "cold-FET" techniques that utilize a modified distributed channel model, which accounts for the significant drain–source capacitance observed under these bias conditions. Furthermore, the requirement to suppress the channel resistance by forward biasing the gate terminal is avoided. Straightforward expressions are introduced to estimate these parasitic quantities and subsequently improve the efficiency of the systematic optimization procedure. A time dependency in the output conductance has been introduced into the equivalent-circuit topology. It effectively represents a time delay at the output and accounts for the observed increase in phase delay at higher frequencies. A simple optimization procedure has been described to evaluate its behavior across the bias plane. The extracted intrinsic elements have also shown appropriate frequency independence over the entire measured frequency range. The validity of all extracted values has been verified with excellent correlation between the measured and modeled S-parameters up to 50 GHz.

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