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An Insight Into Self-Heating Effects and Its Implications on Hot Carrier Degradation for Silicon-Nanotube-Based Double Gate-All-Around (DGAA) MOSFETs

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ABSTRACT Silicon-Nanotube-based ultra-thin DGAA MOSFETs have been extensively studied for their superior immunity to short channel effects (SCEs) and better drive current capability; however, the reliability issues owing to self-heating effects (SHEs) and hot carrier injection (HCI) degradation are yet to be investigated systematically. In advanced non-planar device structures, an increase in power density due to ultra-scaled device dimensions can aggravate both the carrier heating as well as lattice heating. In this paper, 3-dimensional (3-D) electrothermal (ET) simulations using coupled hydrodynamic and thermodynamic transport models are performed to analyze the electrothermal behavior and SHEs in ultra-thin DGAA MOSFET. 3-D TCAD simulation parameters are calibrated with the data obtained from the literature. Through advanced 3-D ET simulations, we demonstrate that the device thermal contact resistance adversely influences both the carrier temperature as well as lattice temperature. The implication of SHE on the device output drive current reduction is also analyzed. The effective drive current method is used to observe the impact of SHE on the intrinsic delay of the device. Further, the performance of the device due to HCI is also highlighted. HCI significantly degrades the overall device performance leading to increased gate leakage current. Finally, the reliability issues induced by SHEs with on-chip ambient temperature variations have also been interpreted using Sentauras based TCAD simulator.

INDEX TERMS DGAA MOSFETs, silicon-nanotube, HCI, SHE, gate leakage current, negative-differential-conductance (NDC), thermal contact resistance quantum confinement.

I. INTRODUCTION

Multi-gate MOSFET architecture like FinFETs, Tri-gate, and Gate-all-around (GAA) nanowire FETs are regarded as the viable option to continue the aggressive downscaling of CMOS technology down under to 22nm thereby sustaining Moore's law-driven scaling and ITRS roadmap [1]. GAA Nanowire FETs, in particular, offer high electrostatic control, significantly improved SCEs, better subthreshold characteristics making it highly attractive for low power applications [2]–[3]. However, despite all these attractive electrical characteristics, Nanowire FETs are plagued with low drive current capability, thereby limiting its ability for high-performance computation application [3]. The stacking of the nanowires may result in improved drive current capability but at the cost of reduced device density over the chip area. In order to have a balance between high performance and device density over the chip area, silicon-nanotube based double gate all around (DGAA) MOSFET with core-shell architecture was introduced by *Fahad et al.* in 2011 [4]. This 3-D device architecture having channel wrapped around by both inner and outer gates render effective charge control inside the channel region providing excellent immunity to short channel effects (SCEs) as well as enhanced output drive current capability owing

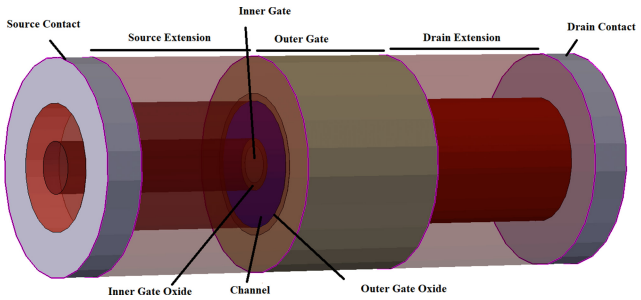

FIGURE 1. 3-D simulated structure of DGAA MOSFET.

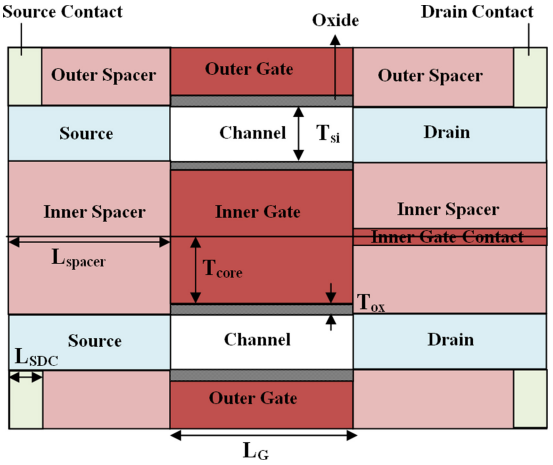

FIGURE 2. 2-D cross-sectional schematic of DGAA MOSFET.

TABLE 1. Device parameters used for DGAA MOSFETs simulation.

Sl. No.	Parameter	Symbol	Value
1	Channel length	L_G	20 nm
2.	Gate to source voltage	V_{GS}	0 -1V
3.	Drain to source voltage	V_{DS}	0 -1.5V
4.	Channel thickness	T_{si}	5nm, 8nm
5.	Inner gate (core) radius	T_{core}	4nm,5nm
6.	Gate oxide thickness	T_{ox}	1nm
7.	Spacer Length	L_{spacer}	5-25nm
8.	Source/Drain contact thickness	L_{SDC}	5nm
9.	Source & Drain doping	N_D	10^{20} cm^{-3}
10.	Channel doping	N_A	10^{15} cm^{-3}

to volume inversion phenomenon [5]–[8]. Because of the high drive current capability and excellent SCEs characteristics, the DGAA MOSFETs have been extensively studied, analyzed, and presented in earlier works [7]–[12]. In post Moore's law era, the non-scaling of the supply voltage with a shrinking device dimension results in a high electric field (∼1 MV/cm) in the device active (channel) region. Under the influence of such a high electric field, the amount of energy absorbed by the carriers exceeds the amount of energy dissipated to the lattice [13]. This results in the " heating" of carriers and flooding the device channel region with hot carriers. The carrier heating affects device performance and thus needs to be investigated [14]. Moreover, device performance also suffers from the electrothermal issues due to self-heating effects (SHE) like hot-carrier injection (HCI), ambient temperature variations, etc. because of the low thermal conductivity of the gate oxide material, spacer region material, and thermal contact resistance (R_{th}) values [15]–[16].

The device dimension is downscaled both in the lateral and radial directions leading to an ultra-thin channel. Furthermore, semi-classical analysis for SHE has been done for other devices in the past [14], but they are not applicable to deal with the ultra-thin device whose behavior is dominated by quantum confinement effects (QCEs) [17]. Due to this QCEs, the thermal conductivity of the channel region (silicon) is much lower than the source/drain region (because of phonon confinement and boundary scattering) [18]. All these aspects cause severe SHE that determinately impact the carrier mobility, thereby exhibiting the negative differential conductance (NDC) effect in the saturation region of device operation. All these physical effects are not investigated for DGAA MOSFETs till date, and thus it is imperative to have an insight into for better thermal management and device designing and operation. Therefore, in this work, we present a comprehensive insight into the estimation of carrier and lattice temperature in ultra-thin DGAA MOSFET using 3-D quantum electrothermal (ET) numerical simulation. The contents of this work are arranged as follows. Section II reports the device structure, numerical simulation set-up, and calibration efforts using the reported results of DGAA MOSFETs. Results and discussion are presented in Section III highlighting thermal behavior and heat transport in DGAA MOSFET with different device dimensions. Finally, Section IV concludes the paper giving a brief summary of the work.

II. DEVICE STRUCTURE AND SIMULATION FRAMEWORK

The 3-D simulated short channel ultra-thin DGAA MOSFET structure considered for analysis is shown in Fig. 1. The silicon-tubular channel region is wrapped by thin oxide layers and sandwiched between inner and outer gates. The radial and lateral directions are considered to be along the radius and the length of the cylindrical channel.

The physical parameters used for DGAA MOSFET structure simulation are explained in Table 1, and the thermal parameters used for ET simulations are explained in Table 2. 3-D ET device simulation has been performed using the Sentauras TCAD device simulator [19]. In order to have simulation accuracy, TCAD results obtained from the Sentauras TCAD simulator are calibrated with the data obtained from [6, Fig. 3]. For simulating DGAA MOSFETs, the simulation set-up was calibrated by reproducing the results of

TABLE 2. Thermal parameters used for ET simulation using [21].

Sl. No.	Material	Thermal conductivity (W/K-cm)
1	Gate Metal (TiN)	0.192
2.	Source/Drain Contact (W)	1.7
3.	Source/Drain Region (Si)	0.62
4.	Channel Region (Si)	0.25
5.	HfO_2	0.023
6.	SiO_2	0.014
7.	Si_3N_4	0.185

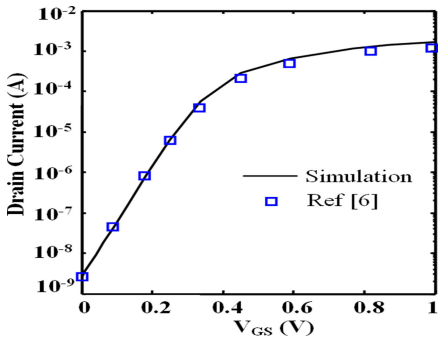

FIGURE 3. Comparison of transfer characteristics of TCAD simulation with data obtained from the [6, Fig.3] for DGAA MOSFET. 3-D TCAD simulations are calibrated with results of [6] for the same device dimension and a drain bias voltage of V_{DS} = 1V.

the Si-NT based DGAA MOSFET of channel thickness 10 nm and a gate length of 20 nm as shown in Fig. 3. The simulation results are in close agreement with the reported data of [6] indicating that our simulations efficiently reproduce the desired results and can be used to investigate the electrothermal behavior. The carrier transport model considered in this analysis is coupled Hydrodynamic (HD) and Thermodynamic (TH) transport model. The HD model captures the electrothermal aspect of carrier transport along with carrier temperature profile (T_C) estimation. The lattice heat flow equation is solved for quantitative estimation of the device lattice temperature (T_L) variation. The density gradient (DG) model is enforced for capturing the quantum confinement of the charge carriers in the ultra-thin channel region. Concerning the ET simulation, Temperature-dependent thermal conductivity [19] model is used to capture the silicon thermal conductivity dependence on thin-film thickness. Source/Drain contact is of Tungsten (W) material, and the gate electrode material used is TiN having work-function tunability [20]. The channel region thermal conductivity is approximately 60% less than the source/drain region, and this is due to phonon confinement and boundary scattering as well as strong QCEs in the channel region of the ultra-thin DGAA MOSFETs [18], [21]. The carrier mobility models used for the simulations are Philips unified mobility model, Lombardi model, and high field saturation model. Regarding the terminal boundary conditions, an isothermal 300K ambient temperature is considered with finite thermal contact resistance (R_{th}) values.

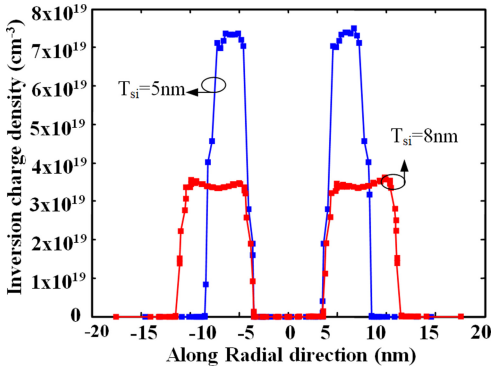

FIGURE 4. Comparison of Inversion charge density along the radial direction for different channel thickness for V_{DS} = 0.8V and V_{GS} = 1V.

III. RESULTS AND DISCUSSION

Figure 4 shows the charge density profile of DGAA MOSFET for different channel thicknesses (T_{si} = 5nm and 8nm) along the radial direction for T_{ox} = 1nm, T_{core} = 4nm, V_{DS} = 0.8V, and V_{GS} = 1V. The DGAA MOSFET with channel thickness of 8nm exhibits inversion at high gate biasing with charge density peak located slightly away from the channel/oxide interface. Reducing the channel thickness increases the effect of carrier profile interaction to the point that now the carrier concentration resembles a parabola peak at the center of the channel region, thereby exhibiting volume inversion [4]. Due to the volume inversion, there is a significant overlap of the electronic wave function, and the carriers in the lower energy states are also able to participate in current conduction. In addition to this, volume inversion enables increased carrier mobility due to reduced surface scattering and enhanced output drive current [4]. Therefore, a DGAA MOSFET with ultra-thin channel thickness will offer better drive current capability and thus considered in further analysis.

A. CARRIER AND LATTICE TEMPERATURE VARIATIONS

In this part, the DGAA MOSFETs were simulated to analyze the carrier temperature (T_C) and device lattice temperature (T_L) variation against drain voltage biasing (V_{DS}) for different channel thicknesses. Here, we have considered the same value of channel thermal conductivity for both cases of DGAA MOSFET with different channel thicknesses. As seen from Fig. 5, the DGAA MOSFET with 8nm channel thickness exhibits 4.3% higher maximum carrier temperature and 6.54% higher maximum lattice heating compared with a 5nm channel thickness at V_{GS} = 1V and V_{DS} = 1V. Strong QCEs in DGAA FETs with an ultra-thin channel thickness of 5nm influences the distribution of inversion carriers strongly leading to volume inversion phenomenon and undergoes less surface scattering whereas the carriers scattering rate is enhanced with the optical phonon for 8nm channel case, thereby increasing the lattice temperature (T_L). Moreover, it can also be observed that for V_{DS} < 0.2V,

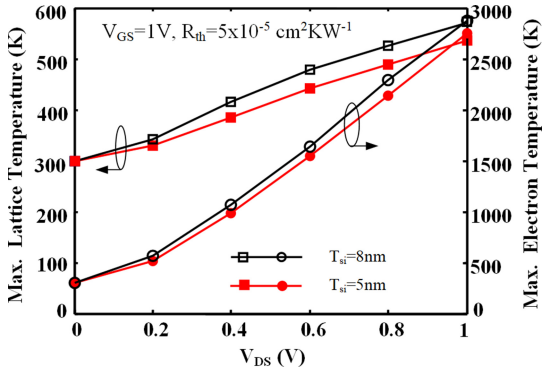

FIGURE 5. Variation of maximum lattice temperature (T_{Lmax}) and maximum electron temperature (T_{Cmax}) against drain voltage for different values of channel thickness.

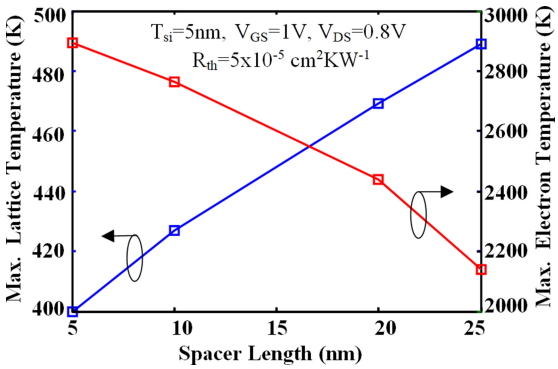

FIGURE 6. Variation of maximum lattice temperature (T_{Lmax}) and maximum electron temperature (T_{Cmax}) against spacer length.

T_{Lmax} increases slowly due to low-field transport, but beyond $V_{DS} > 0.2$V, both the T_{Lmax} and T_{Cmax} increase rapidly due to high field transport leading to enhanced carrier heating and carriers start undergoing energy relaxation with optical phonons. The T_{Lmax} and T_{Cmax} variation for different spacer length is shown in Fig. 6. As can be noticed from Fig, the T_{Cmax} decreases with an increase in spacer length. However, the T_{Lmax} increases with an increase in spacer length. This happens because of the fact that spacer length increase leads to a reduction of the rate of dissipation of heat generated inside the device lattice to the thermal cooling reservoirs (S/D metal contacts). Figure 7 shows the contour plot of both the lattice temperature (T_L) and carrier temperature (T_C), respectively along the channel length for $V_{DS} = 0.8$V and $V_{GS} = 1$V exhibiting the hot spot near the drain end.

Figure 8 shows both the T_L and T_C variation along the channel length plotted by taking a cut-line of contour at the center of the channel thickness. The T_L varies from 429K to 465K with a peak of 489K inside the drain region, whereas the T_C varies from 442K to 515K with a maximum value of 2136K at the drain end. As can be seen from Fig. 7, high energy electrons (hot carriers) coming from the source side are scattering heavily with the phonon emission on the drain side of the device locally increasing the lattice temperature inside the drain region.

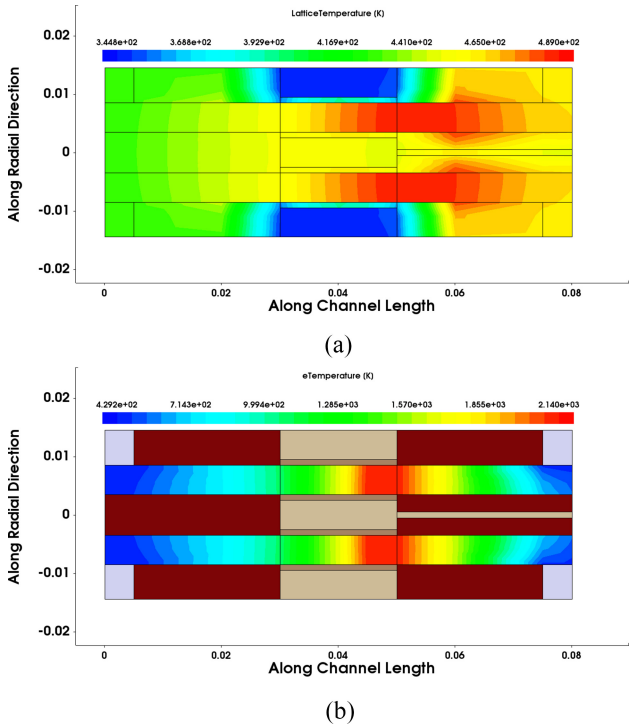

FIGURE 7. Contour plot of (a) lattice temperature and (b) electron temperature profile along the channel length (μm).

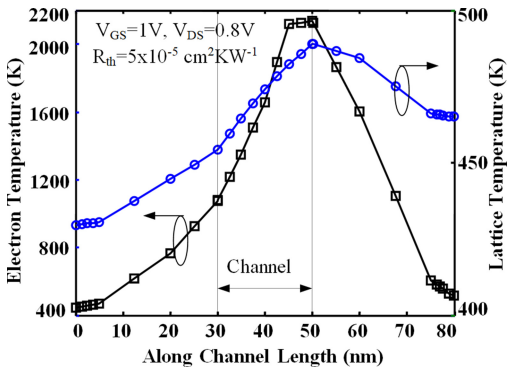

FIGURE 8. Cut-line plot of the variation of lattice temperature and electron temperature against channel length.

B. TRANSFER AND OUTPUT CHARACTERISTICS UNDER SHE

Figure 9 shows the transfer characteristics of the DGAA MOSFETs for different values of channel thickness and drain voltages. The curves obtained from coupled ET simulation are compared with the isothermal results where no self-heating is observed. As can be seen from Fig. 9, the self-heating induced current reduction (SHCR) effect is observed due to carrier scattering with an enhanced optical phonon population. The current reduces by almost half for $T_{si} = 5$nm when the gate voltage and drain voltage are set to 1V and 0.6V, respectively, as shown in Fig. 9. The SHCR effect, therefore, measures the difference between the drive current with an equilibrium phonon population and drive

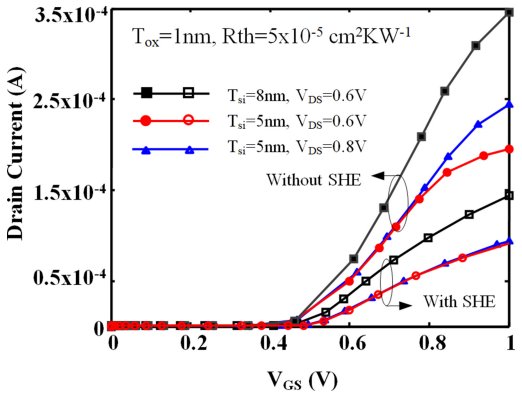

FIGURE 9. Comparison of transfer characteristics of DGAA FETs with SHE and without SHE for different values of channel thicknesses and drain voltage biasing.

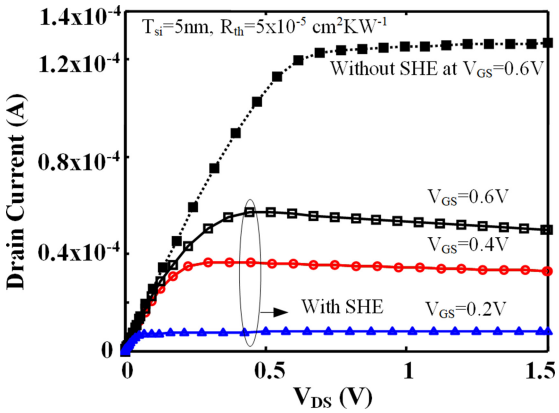

FIGURE 10. Output characteristics of DGAA FETs for different gate voltages and comparison between output characteristics of DGAA FETs with SHE and without SHE for $V_{DS} = 0.6V$.

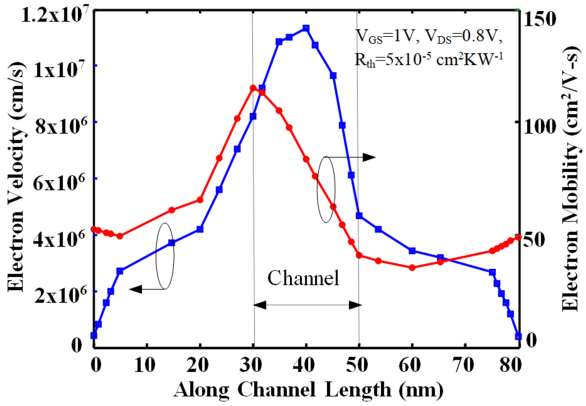

FIGURE 11. Cut-line plot of the variation of electron velocity and electron mobility against channel length.

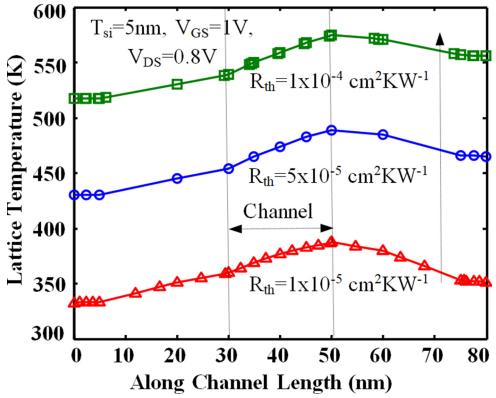

FIGURE 12. Cut-line plot of the variation of lattice temperature (T_L) against channel length for different values of thermal contact resistance.

current with a non-equilibrium enhanced phonon population. Moreover, the SHCR effect increases with increasing drain voltage from 0.6V to 0.8V.

The output characteristics of the DGAA MOSFETs for $T_{si} = 5$nm at different values of the gate voltage is shown in Fig. 10. The HD transport model simulation displays NDC in the saturation region of the device operation. The higher carrier-optical phonon scattering and enhanced hot carriers population at higher gate voltages detrimentally degrade the carrier mobility in the channel region. The I_D-V_{DS} curve of the device with and without the SHE at $V_{GS} = 0.6V$ is also depicted in Fig. 10. As can be observed from Fig, the temperature rise is high enough to cause the drain current to suffer from SHE and reducing it to about half of its value. The variation of carrier velocity and carrier mobility for $V_{DS} = 0.8V$ and $V_{GS} = 1V$ along channel length is shown in Fig. 11. It is interesting to observe that the carrier velocity increases rapidly with the peak value of 1.1×10^7 cm/s in the channel region and tends to decrease following an interaction between the hot carriers (velocity$> 1 \times 10^7$ cm/s) and the optical phonons generated due to high electric field signifying that the carriers lose its velocity in the vicinity of the channel/drain interface. As a consequence of the enhanced hot electron population, the carrier mobility decreases by about 50%, thereby offering NDC at the output, as shown in Fig. 10.

C. EFFECT OF THERMAL CONTACT RESISTANCES R_{TH} ON SHE

This section highlights the influence of thermal contact resistance (R_{th}) of electrodes on the electro-thermal behavior of this device. The variation of T_L and T_C along the channel length for different values of thermal contact resistance (R_{th}) is shown in Figs. 12 and 13, respectively. In order to maintain uniformity for all the contacts, we have maintained all the contacts (G, S, D) at the same value of R_{th}. As can be seen from Fig. 12, the T_{Lmax} increases from 387K to 574K(48% increase) with increasing R_{th} (cm^2KW^{-1}) from $1 \times 10^{-5} cm^2KW^{-1}$ to 1×10^{-4} cm^2KW^{-1}. However, the contact thermal resistance has no significant impact on the T_{Cmax} (shown in Fig. 13) and virtually remains unchanged. The drive current (I_D) variation for different types of oxide having different values of dielectric constant against varying R_{th} is shown in Fig. 14. The drive current decreases from 92μA to 68μA (26% decrease), 80μA to 60μA (25%

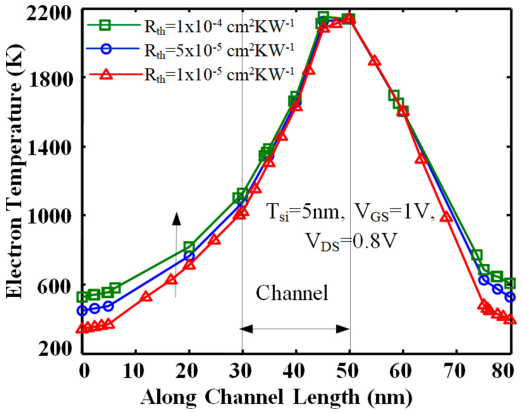

FIGURE 13. Cut-line plot of the variation of electron temperature (T_C) against channel length for different values of contact thermal resistance.

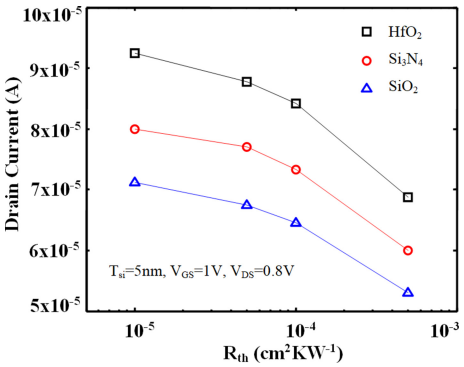

FIGURE 14. Variation of drain current against increasing thermal contact resistance for different types of the gate oxide.

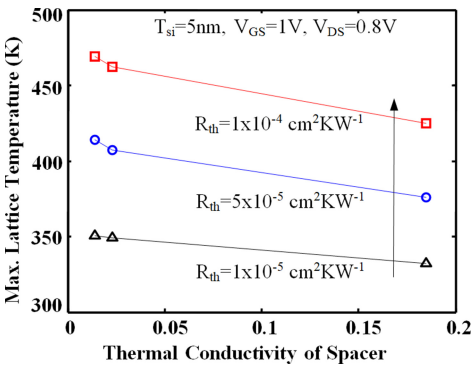

FIGURE 15. Variation of maximum lattice temperature (T_{Lmax}) against varying thermal conductivity of spacer for different values of thermal contact resistance.

decrease), and 71μA to 53μA (25.3% decrease) for HfO_2, Si_3N_4, and SiO_2 oxide type respectively.

Figure 15 depicts the change in hot spot temperature (T_{Lmax}) against the different thermal conductivity of spacers at different values of R_{th}. As can be seen from Fig. 15, with increasing the thermal conductivity values from 0.016 W/K-cm to 0.18 W/K-cm (i.e., SiO_2 to Si_3N_4), the T_{Lmax} reduces from 414K to 376K (9 % decrease) for

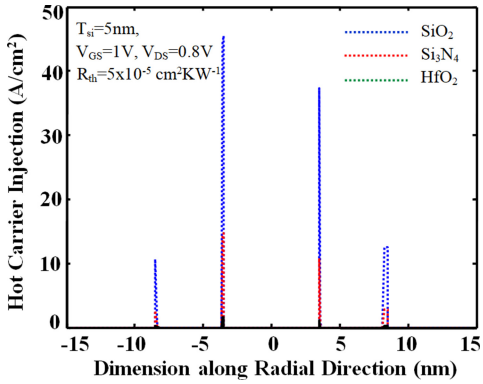

FIGURE 16. Variation of HCI along the radial direction for different gate oxide type.

$R_{th} = 5 \times 10^{-5}$ cm^{2}KW^{-1}. The one crucial design consideration to reduce the hot spot temperature (T_{Lmax}) and increase I_D by using high conductivity spacer material.

D. HCI DEGRADATION AND GATE DIRECT LEAKAGE CURRENT

This section presents the HCI degradation and gate leakage current analysis of the device due to SHE. We have already discussed that the energized carriers with hot electron velocity greater than 1x10^7 cm/s make a hot spot near the drain end. Thus, some of the carriers have a finite probability of tunneling through the interface barrier and entering into the oxide [22]. HCI degradation has been correlated to the injection of field-heated channel electrons into the gate oxide. These injected electrons break chemical bonds (Si-O) and create defects, thereby degrading the on-current and increases the gate leakage current of the device [23]. Therefore, a close examination for HCI degradation (where $T_C >> T_L$) would help the chip designers to develop a new class of device with reliability for sub-22nm applications. Fig. 16 shows the plot of hot electron injection against radial direction at both the channel/oxide interfaces for different types of oxide dielectrics at $V_{DS} = 0.8$V and $V_{GS} = 1$V. The HCI is plotted by taking a cut-line along the radial direction at 0.5nm inside the channel region from the channel/drain interface. Since the hot spot is usually located in the channel region towards the drain end, as shown in Fig. 7, therefore, we considered taking the cut-line at this point.

A contour plot for HCI injection is also depicted in Fig. 17. LUCKY hot carrier injection model is used to extract the amount of carrier injection into the gate oxide [24]. As can be seen from Fig. 16, the maximum injection occurs for gate oxide with low dielectric value facilitating the trapping of hot electron and kinetic dissociation of Si-O bonds by hot electron dictating HCI degradation. The HCI injection at the inner surface is approximately four times higher than at the outer surface due to the reduced rate of heat dissipation at the inner surface and enhances 2-D QCEs and can be verified from Fig. 17.

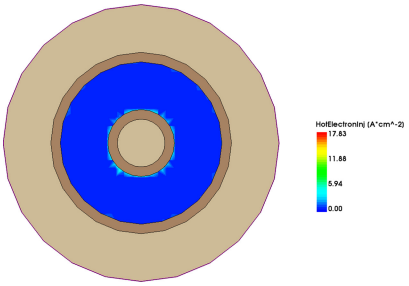

FIGURE 17. Contour plot of Hot Carrier Injection along the radial direction.

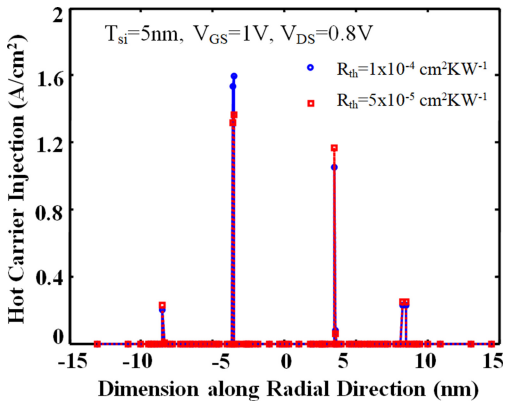

FIGURE 18. Variation of HCI along the radial direction for different thermal contact resistance values.

The HCI values for different values of thermal contact resistance are shown along the radial direction of the device in Fig. 18. With increasing the R_{th} value from 1×10^{-5}cm^{2}KW^{-1} to 1×10^{-4} cm^{2}KW^{-1}, the HCI injection increases from 1.3 A/cm^2 to 1.6 A/cm^2 (23 % increase) due to enhanced lattice temperature of the device structure elevating HCI degradation. The formation of traps inside oxide due to HCI consequently leads to threshold voltage variation and other performance issues. Moreover, the trap formation and dissociation of Si-O bonds affect the oxide reliability and enhance the gate direct tunneling current due to tunneling mechanism where the hot carrier tunnels from the channel region into the conduction band of the oxide layer constituting gate direct leakage current [22], [24]. The severity of the gate tunneling current increases with an increase in the carriers and lattice temperature due to an increase in R_{th} values, as shown in Fig. 19. It can be noticed that, with an increase in R_{th} value from 10^{-5}cm^{2}KW^{-1} to 10^{-4} cm^{2}KW^{-1}, the gate current increase from 5×10^{-13} A to 5×10^{-12} A nearly by one order of magnitude for the case of HfO_2 as a high-K dielectric. The gate current variation is also described for different oxide type, the gate oxide with high-K dielectric value experiences less gate tunneling as compared with its counterpart. The direct gate tunneling current (I_G) variation against the spacer length is shown in Fig. 20. As the length of the spacer increases from 5nm to 25nm, I_G decreases by more than two orders of magnitude. This is happening because the carrier temperature is reduced with an increase

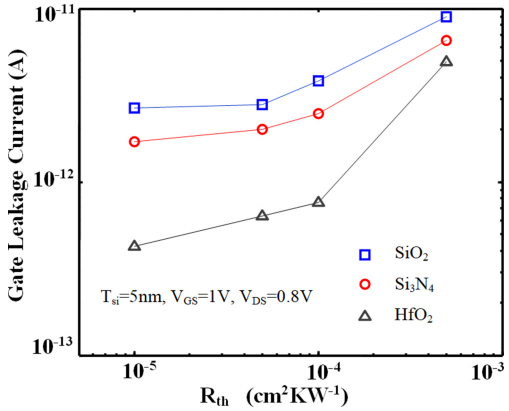

FIGURE 19. Variation of gate leakage current against increasing thermal contact resistance for different types of gate oxide.

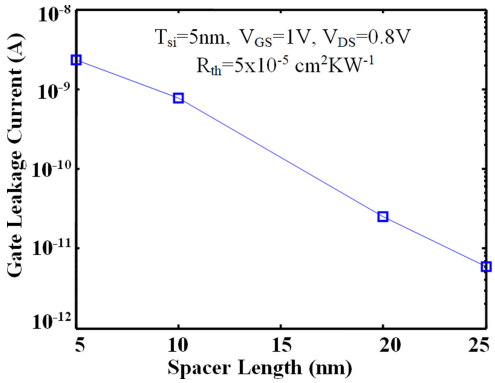

FIGURE 20. Gate direct leakage current variation against increasing spacer length values.

in the source/drain extension length and is also described earlier in Fig. 6.

E. EFFECTS OF AMBIENT TEMPERATURE VARIATIONS

The SHE related degradation strongly depends on the on-chip ambient temperature variations [25]. As the number of transistor count in a chip increases with technology, the average temperature (ambient temperature) of the chip will increase, leading to performance degradation. Here, we have simulated the DGAA MOSFETs using ET simulation to analyze the effect of ambient temperature (T_A). The T_{Lmax} is plotted against increasing ambient temperature values at different R_{th} values in Fig. 21. T_{Lmax} value increases from 489K to 561K with increasing T_A from 300K to 380K at R_{th} value of 5×10^{-5}cm^{2}KW^{-1}. A higher R_{th} value will enhance the lattice temperature values and is reflected in the plot with an upward shifting of the curve. The drain current (I_D) and gate leakage current (I_G) are plotted in Fig. 22 for varying T_A from 300K to 380K. At higher values of T_A, T_{Lmax} increases consequently decreasing the I_D from 9.32×10^{-5}A to 8.84×10^{-5}A due to reduced carrier mobility at $R_{th} = 5\times10^{-5}$cm^{2}KW^{-1}, on the contrary; the I_G increases from 5.04×10^{-12}A to 7.69×10^{-12}A supporting the fact already described that temperature rise leads to HCI and

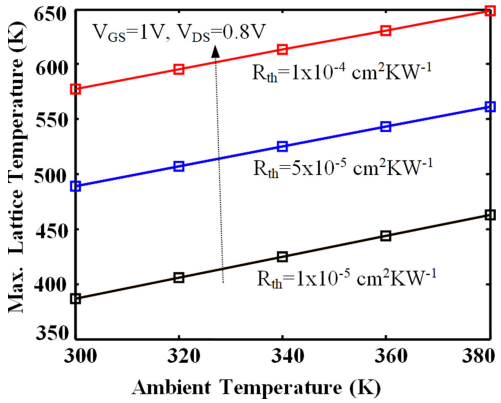

FIGURE 21. Variation of hot spot (lattice) temperature against increasing ambient temperature values for different thermal contact resistance.

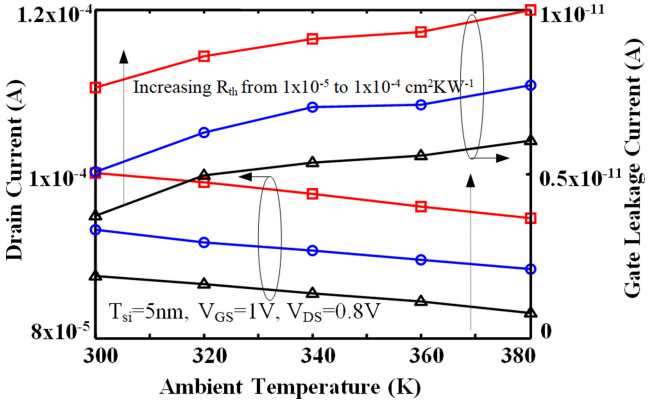

FIGURE 22. Variation of drain current and gate direct leakage current against increasing ambient temperature values for different thermal contact resistance.

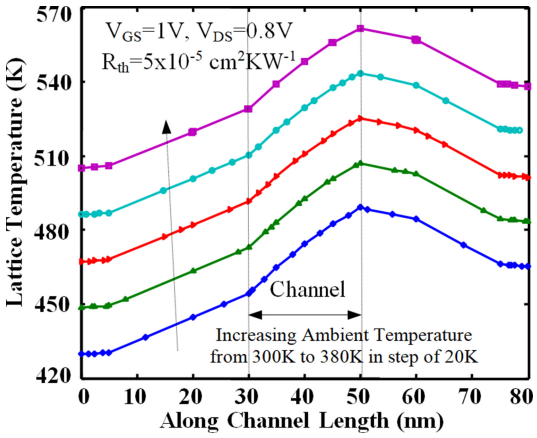

FIGURE 23. Cut-line plot of the variation of lattice temperature against channel length for increasing ambient temperature values.

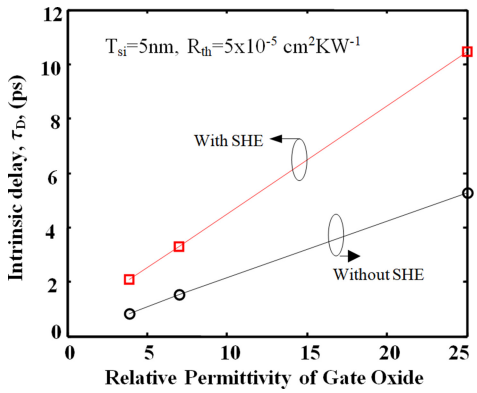

FIGURE 24. Comparison of intrinsic delay against a different type of gate oxide with SHE and without SHE.

thereby enhancing the gate leakage current. Fig. 23 shows the cut-line plot of T_{Lmax} along the channel length for different values of T_A (300K to 380K in a step of 20K). The lattice temperature variation shows a peak in the channel region due to the fact that the channel thermal conductivity is 60% less than the source and drain region. The reduction in thermal conductivity is due to phonon boundary scattering and strong QCEs in the channel region.

F. EFFECTIVE DRAIN CURRENT AND INTRINSIC DELAY

In addition, the dynamic performance of the DGAA MOSFETs is also investigated in this work. We have compared the dynamic performance of DGAA MOSFETs with and without the SHE. We have used the effective drive current method to calculate the intrinsic delay of the device. The effective drive current method is evaluated using the method suggested by [26] as follows

$$I_{eff} = \frac{(I_H + I_L)}{2} \tag{1}$$

$$\text{where, } I_H = I_{sat}\left(V_{DS} = \frac{V_{DD}}{2},\ V_{GS} = V_{DD}\right) \tag{2}$$

$$\text{and } I_L = I_{sat}\left(V_{DS} = V_{DD},\ V_{GS} = \frac{V_{DD}}{2}\right) \tag{3}$$

The intrinsic delay is given by-

$$\tau_D = \left(C_{gg} \times V_{DD}\right) \cdot \left(I_{eff}\right)^{-1} \tag{4}$$

where, C_{gg} is gate capacitance and V_{DD} is drain supply voltage.

Figure 24 compares the intrinsic delay variation against different oxide relative permittivity values. As can be seen, a gate dielectric with higher permittivity value will offer high oxide capacitance, thereby increasing the intrinsic delay. Moreover, the intrinsic delay is increased when SHE is considered, and this is because the effective drive current is reduced by SHE which reflects in the intrinsic delay increasing from 5.26ps to 10.47ps for HfO_2 dielectric oxide case. The plot of effective drive current (I_{eff}) and intrinsic delay (τ_D) against different oxide dielectric values for $R_{th} = 5 \times 10^{-5}$cm^{2}KW^{-1} and $R_{th} = 5 \times 10^{-4}$cm^{2}KW^{-1} are shown in Fig. 25. As expected, the I_{eff} decreases with an increase in the R_{th} value, consequently increasing the intrinsic delay. The rigorous investigation of the electro-thermal behavior of DGAA MOSFETs suggests that the device dimension and bias parameters have a significant impact on the overall performance of the device.

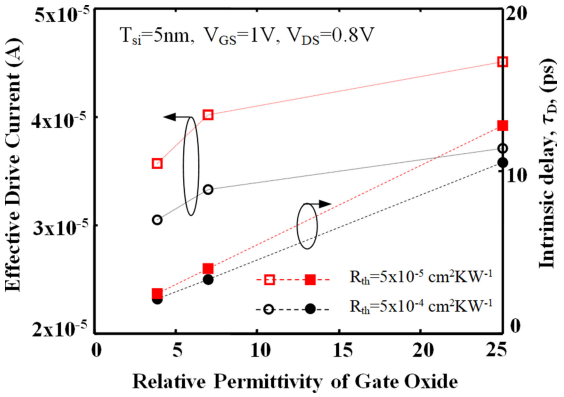

FIGURE 25. Variation of effective drive current and Intrinsic delay against different types of gate oxide for varying thermal contact resistance values.

IV. CONCLUSION

In conclusion, we have demonstrated that the interaction of carriers with the phonon generated inside the channel region leads to SHE which gives rise to severe electrothermal issues such as HCI degradation, ambient temperature variations, intrinsic delay, etc. We have performed 3-D quantum E-T simulation using coupled HD and TH transport equations for silicon-nanotube-based DGAA MOSFETs. The carriers' dynamics and the lattice temperature are strongly influenced by the geometrical confinement of the carriers in the ultra-thin channel region of the device. The SHE analysis demonstrates that the device thermal contact resistance adversely influences both the carrier temperature as well as lattice temperature. This study validates the observation of NDC at the saturation region of the device output characteristics. We have further established the relationship for mobility reduction induced by SHE and for carrier velocity. In addition to this, the effective drive current method has been used to observe the impact of SHE on the intrinsic delay of the device. Furthermore, our study also confirms the implication of SHE on device performance due to HCI. HCI degradation significantly impacts the overall performance leading to increased direct gate leakage current. Finally, the degradation mechanism of SHE with on-chip ambient temperature variations have also been interpreted using Sentauras based TCAD simulator.

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