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An Integrated 13.56-MHz RFID Tag in a Printed Organic Complementary TFT Technology on Flexible Substrate

Vincenzo Fiore, *Student Member, IEEE*, Placido Battiato, Sahel Abdinia, Stephanie Jacobs, Isabelle Chartier, Romain Coppard, Gerhard Klink, Eugenio Cantatore, *Senior Member, IEEE*, Egidio Ragonese, *Senior Member, IEEE*, and Giuseppe Palmisano, *Senior Member*

Abstract— This paper presents the first printed organic 13-MHz RFID on flexible substrate. The proposed solution includes a planar near field antenna bonded to an RFID tag, which is printed on flexible foil using an organic complementary TFT technology. Thanks to an active envelope detector, ASK modulation with modulation depth as low as 20% can be adopted to increase the available input power for the rectifier. The RFID functionality is demonstrated at the internally generated supply voltage of 24 V, for a reading range of 2-5 cm and a bit-rate up to 50 bit/s. With more than 250 transistors on the same foil, this work represents the most complex circuit ever published in a printed organic complementary TFT technology.

Index Terms— ASK modulation, active detection, mixed analog-digital circuits modulation index, organic circuits, pentacene, polyimide, radio frequency identification, sub-threshold, silent tag, spiral antenna, thin film transistor.

I. INTRODUCTION

Printed organic electronics has gained increasing consideration as a cost-effective alternative to silicon, especially in those applications where cheap or disposable devices are required [1]-[5]. In the roadmap of printed electronics, radio frequency identification (RFID) has an important place due to the huge available market still covered by bar codes. Despite this great interest, state-of-the-art printed organic technologies do not enable the implementation of a complete RFID tag yet. This is mainly due to the complexity of a tag, which includes a near-field antenna, radio frequency (i.e., 13-MHz) detection, mixed analog/digital

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V. Fiore, P. Battiato, and G. Palmisano are with DIEEI, Università di Catania, Catania, I-95125, Italy. (e-mail: vincenzo.fiore@dieei.unict.it, battiatoplacido@gmail.com, giuseppe.palmisano@dieei.unict.it).

S. Abdinia and E. Cantatore are with Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands (e-mail: S.Abdinia@tue.nl, E.Cantatore@tue.nl).

S. Jacobs, S. Chartier and R. Coppard are with CEA-LITEN, Grenoble, F-38054, France (email: stephanie.jacob@cea.fr, isabelle.chartier@cea.fr, romain.coppard@cea.fr).

G. Klink is with Fraunhofer EMFT, 80686 Munich, Deutschland (email: Gerhard.Klink@emft.fraunhofer.de)

E. Ragonese is with STMicroelectronics, Catania, I-95121, Italy (e-mail: egidio.ragonese@st.com).

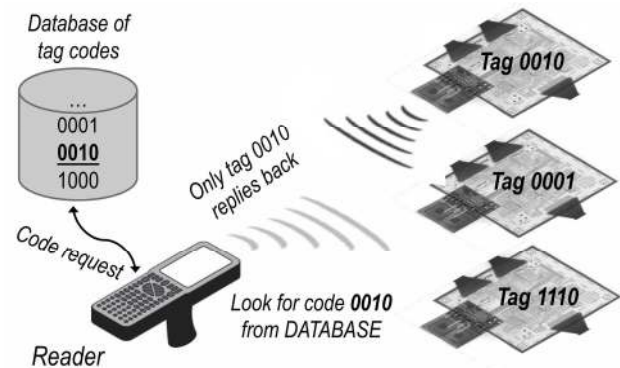


Fig. 1. “Silent tag” identification scheme used by the proposed organic RFID.

functionalities and harvesting capability (for passive RFID). Moreover, RFID security typically requires a level of circuit complexity that cannot be achieved nowadays by organic electronics. Recently, several promising results based on lithographic organic processes have been published. Specifically, an inductive-coupled organic RFID operating at 13.56 MHz has been demonstrated using a p-type organic technology on foil [6]. A complementary organic technology has been used for the 13.56-MHz transponder in [7]. A complementary hybrid organic/metal-oxide process has been exploited to demonstrate bidirectional communication in an HF RFID [8], [9]. This last solution adopts passive diode-based envelope detection together with OOK modulation, resulting in limited sensitivity and reduced reading range.

In recent years, a printed complementary organic TFT (C-OTFT) technology has been developed [10], [11] and successfully employed to design digital and analog circuits [12], [13], a 4-bit analog-to-digital converter [14] and a light sensor [4]. This technology has been recently used to explore the feasibility of a RFID tag with active envelope detection, making possible to demodulate ASK PWM-coded signals with modulation depth (h) as low as 25% [15]. Starting from this result, a fully integrated solution for a printed 13.56-MHz RFID tag on flexible substrate has been designed. The RFID has been manufactured using an improved version of the C-OTFT process used in [15] and includes a 13-MHz planar antenna bonded to the printed organic tag. The tag integrates a rectifier for power supply, a receiver with an active envelope detector, and a digital section for code recognition and reply.

The proposed RFID exploits an identification scheme called “silent tag” [16]. Each silent tag is customized with its own

code and answers only to readers sending this code, thus avoiding the need of anti-collision or disabling mechanisms. The main advantage is that a tag search is possible only if a list of the tags that can be offered to the reader (e.g., the tags in the shop) is known in advance (see Fig. 1). In this way, tag security is ensured with no need for encryption, which makes this solution especially suitable for organic printed electronics.

The paper is organized as follows. Section II describes the RFID architecture, fabrication technologies and circuit design. Measurements of both building blocks and overall tag are discussed in Section III. Conclusions are drawn in Section IV.

II. SYSTEM DESCRIPTION: TECHNOLOGY AND DESIGN

The architecture of the proposed RFID tag is shown in Fig. 2. The tag includes a receiver, consisting of an active envelope detector (ED) and clock/data recovery circuitry, a rectifier, and a code recognition unit. Both ED and the rectifier are inductively coupled to the reader by means of a two-coil antenna on a polyimide foil. A PWM coding is adopted with bit “1” and “0” corresponding to a duty cycle of 70% and 30% high, respectively. A bit rate of 50 bit/s has been chosen. The rectifier provides the internal supply voltage, V_{DD} , to the other blocks. The ED extracts the ASK envelope from the 13.56-MHz carrier and drives the recovery circuitry. The clock decoder detects the rising edge of the envelope signal, ENV, thus providing a synchronizing clock, CLOCK, to the code recognition unit. Signal CLOCK is properly delayed and then used by the D-flip-flop (D-FF) to extract the received data stream, DATA, by sampling signal ENV. The code recognition unit is designed to receive a sequence of “reset” and “identity” codes and consists of two modules. The reset module (RM) synchronizes all the tags in the reader range with the start of the following identity transmission code. The identity verification module (IVM) compares the received code with the tag identity and in case of code matching enables the response back to the reader by using the modulator (not included in the block diagram for the sake of simplicity). It is driven by a ring oscillator, which is activated by signal MOD.

A. Complementary Organic TFT Technology

The adopted printed complementary organic technology is manufactured on an $11 \times 11 \text{ cm}^2$ flexible foil by CEA-Liten [10], [11]. The TFTs are implemented in a top-gate bottom-contact multi-finger structure with a 20- μm channel length on 125- μm thick polyethylene-naphthalate (PEN) substrate. A simplified cross-section of both p-type and n-type TFTs is shown in Fig. 3. A microphotograph of a multifinger OTFT ($W = 2000 \mu\text{m}$, $L = 20 \mu\text{m}$) is shown in Fig. 4. Since the present printing resolution of metallic inks can barely reach line/spacing resolution of 20 μm as well as the required flatness, a direct patterning approach by means of laser ablation was chosen to pattern the source/drain electrodes. Fig. 5 summarizes main process steps of the adopted printed C-OTFT technology. Gold is sputtered to a thickness of 30 nm on the PEN and then patterned using laser beam to form the

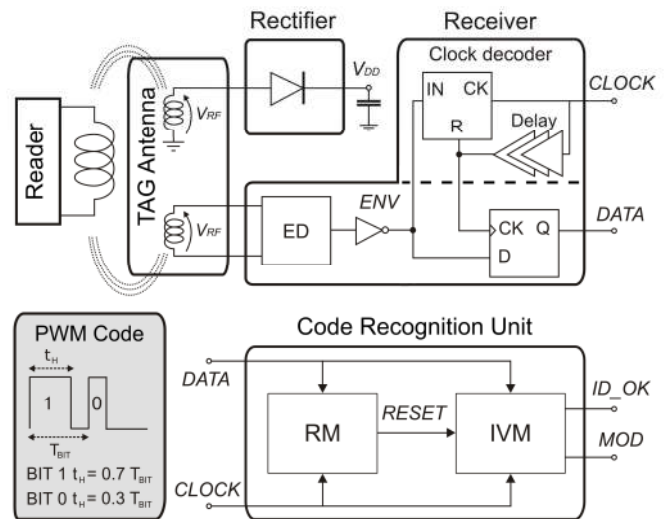


Fig. 2. Block diagram of the 13.56-MHz RFID tag and PWM coding scheme.

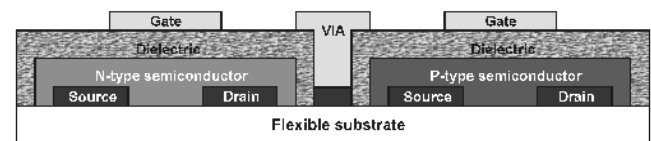


Fig. 3. C-OTFT cross-section of the adopted technology.

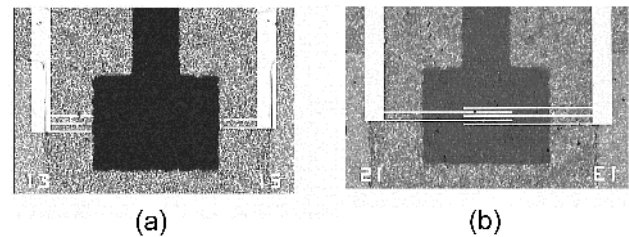


Fig. 4. Multifinger OTFT photo. (a) Top view. (b) Bottom view ($W = 2000 \mu\text{m}$, $L = 20 \mu\text{m}$).

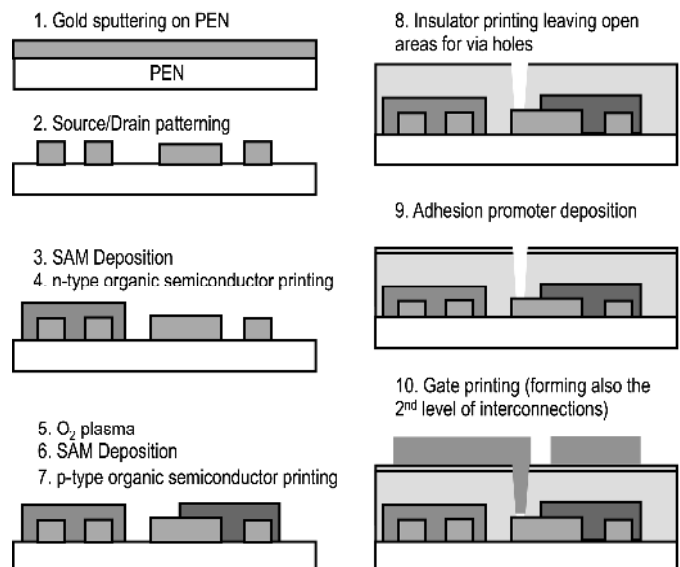


Fig. 5. Simplified process flow of the adopted C-OTFT technology.

source and drain electrodes as well as the first level of interconnections. Then, the n-type organic semiconductor (Polyera ActivInk®) is patterned by printing methods. The source/drain electrodes and the PEN are cleaned with an O₂ plasma to prepare the surface for the self-assembled monolayer (SAM) deposition and p-type organic semiconductor (Merck Lisicon S1200) printing. The common fluoropolymer dielectric (Merck Lisicon D139, 750 nm thickness) is then screen-printed on top of both semiconductors and then annealed, leaving open areas for via holes. Finally, a silver-ink conductor is screen-printed, forming OTFT gate electrodes and the second level of interconnections. Reliability and performance of TFTs were improved for this work by re-engineering the gate stack, using an adhesion promoter. Firstly, the gate leakage current was reduced, thus improving hard yield and also dielectric robustness during circuits test. Secondly, the gate capacitance was increased. Actually, in a former gate stack the silver-ink was formulated with adhesive to guarantee adhesion on the fluoropolymer dielectric. However, it was found that this approach added a parasitic capacitance in series with the dielectric one [17]. This drawback was overcome with a silver ink that no longer needs adhesive and results in a higher gate capacitance. Measurements performed on a 1-mm² Metal/Insulator/Metal (MIM) capacitor showed a 23% increase of the capacitance (i.e., 2.15 nF/cm²), which in turn leads to an increase of the OTFT mobility (μ_{SAT}) typically by around 80% and 27% for the p-type and n-type transistors, respectively. The process also provides optional carbon-ink resistors that are screen-printed after organic semiconductors patterning and before the final screen-printing of the gate layer. Main electrical parameters of both p-type and n-type TFTs are summarized in Table I for channel length of 100 μm and 20 μm . It is worth noting that the adoption of the new silver ink allows an outstanding μ_{SAT} of 2.7 cm²/V·s to be achieved for 100- μm p-type TFTs. The better performance can be easily highlighted by comparing the output characteristics of both p-type and n-type transistors with standard and new silver ink, as shown in Fig. 6. The OTFT current capability is more than doubled for both 2000/20 p-type and n-type transistors for a gate voltage of 40 V, that is the maximum supply voltage adopted in previous work [15]. Most importantly, the curves at 20-V gate voltage show that both devices can operate in sub-threshold region. Moreover, transistor output impedance is high even for drain voltages as low as 10 V. This feature was extensively used in this work to enable both analog and digital circuit operation at reduced supply voltage.

B. Antenna Fabrication Technology and Design

The 13.56-MHz antenna was fabricated with a semi-additive electroplating process in a roll-to-roll manufacturing mode. A substrate polyimide foil was chosen as highly temperature stable substrate to enable assembly of surface mount devices (SMDs) by soldering. As shown in Fig. 7, the process starts with metallizing the 50- μm thick polyimide film with 500-nm copper in a roll-to-roll sputter

TABLE I. COMPARISON OF MAIN ELECTRICAL PARAMETERS OF C-OTFTS DEPENDING ON THE GATE SILVER-INK

Parameters	p-type TFT		n-type TFT	
	Standard silver ink	New silver ink	Standard silver ink	New silver ink
L = 100 μm				
Carrier mobility [cm ² /V·s]	1.5	2.7	0.55	0.7
Threshold voltage [V]	-20	-22	18	17
I_{ON}/I_{OFF}	$\sim 10^7$	$> 2 \cdot 10^7$	$> 2 \cdot 10^7$	$> 10^7$
L = 20 μm				
Carrier mobility [cm ² /V·s]	0.8	1.5	0.19	0.24
Threshold voltage [V]	-24	-25	15	14
I_{ON}/I_{OFF}	$> 2 \cdot 10^7$	$> 5 \cdot 10^7$	$\sim 10^7$	$> 10^7$

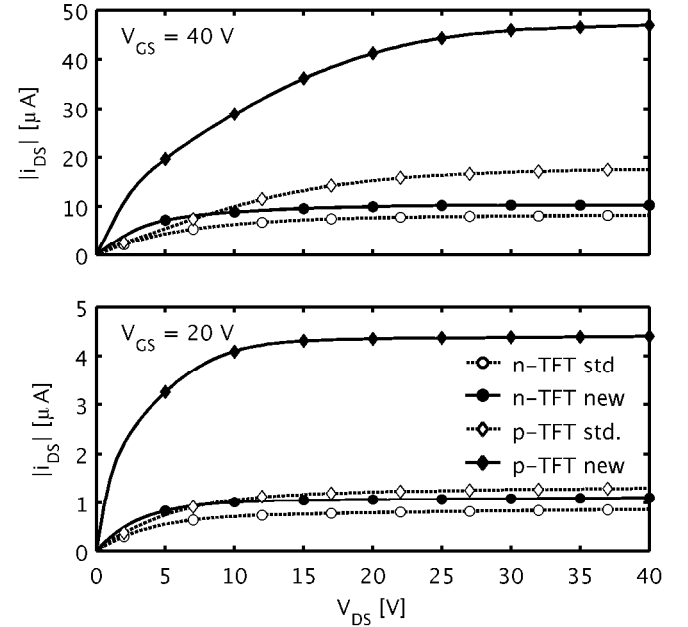


Fig. 6. Output characteristics of OTFTs with standard and new silver ink ($W = 2000 \mu\text{m}$, $L = 20 \mu\text{m}$) for $V_{GS} = 40 \text{ V}$ and $V_{GS} = 20 \text{ V}$.

machine. To get good adhesion between substrate and metallization a very thin tie layer of chromium ($\sim 7 \text{ nm}$) is applied. Afterwards, a photolithography step is performed, starting with laminating a 18- μm thick dry resist on the substrate foil and its exposure to a broadband UV source through a 9" mask with an exposure field of 200 by 200 mm². Development is done with an alkaline soda solution in a pass-through spray developer line. Subsequently, the copper conductor lines are electroplated in the resist openings to a height of 9 μm . The resist is removed and finally the sputtered copper layer and the chromium tie layer are etched away. Due to the copper etching process, the conductor thickness is slightly decreased, ending up in a total thickness of 8 μm , which corresponds to a sheet resistance of 2.5 m Ω /sq. For closing the antenna coil a conductor bridge was fabricated by screen printing. The coil windings are first insulated by printing and curing a dielectric paste (ESL1901-D). Then, the

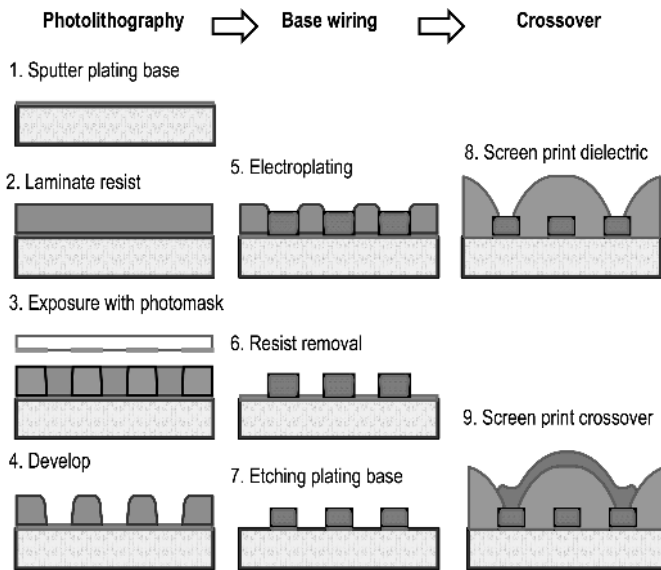


Fig. 7. Antenna fabrication process flow.

bridge is printed with silver paste (ESL1901-S). Curing is done in a belt oven with a peak temperature of 90 °C. The conductive bridge has a sheet resistance of 21 mΩ/sq. A value of 8.1 pF/mm² was measured for the parasitic capacitance between silver bridge and copper coil. A photograph of the fabricated antenna on foil is shown in Fig. 8, whereas its main parameters are detailed in Table II. As highlighted in the photo, the antenna actually consists of two windings. The outer single-ended coil and the inner differential coils with center tap are used by the rectifier and the receiver, respectively, for the coupling with the reader antenna. Two capacitors (C_{RECT} and C_{RX}) are adopted to tune the antenna resonance at 13.56 MHz. This two-coil antenna structure highly complies with the proposed RFID architecture (see Fig. 2), which exploits a single-ended rectifier and a differential-like ED to maximize ac-dc conversion efficiency and compensate for the high TFT parasitic capacitances, respectively. The use of two antennas also gives a degree of freedom in the design of the coil inductances, which can be independently optimized. Since the estimated input capacitance of the rectifier was 70 pF, the single-ended coil inductance and the external capacitance, C_{RECT} , were set to about 725 nH and 120 pF, respectively, thus maintaining adequate tuning against process tolerances. Given the inductance specification of the outer coil, its geometrical parameters were set by using simple equations for planar inductors [18], [19] (constrained to an area of about 5×2.5 cm²). Thanks to the lower input capacitance of the envelope detector with respect to the rectifier one, the differential coil was designed to maximize the inductance value by filling the available internal space, thus achieving a high QL product. Finally, to better estimate the overall antenna performance, which is also affected by a magnetic coupling between the two coils, 2-D electromagnetic simulations were carried out in Momentum MW. Based on these simulations, a value of capacitor C_{RX} of about 60 pF was required to tune the receiver antenna at 13.56-MHz for a distance of 5 cm from the

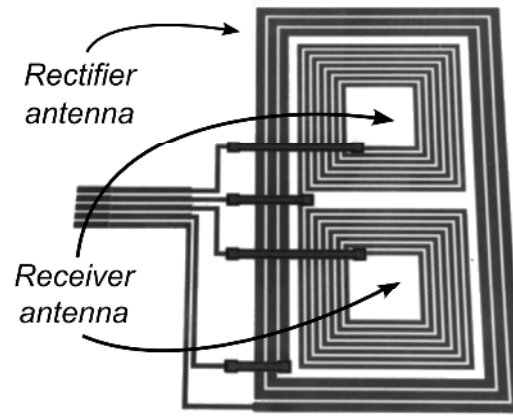


Fig. 8. Photograph of the fabricated 13-MHz antenna on polyimide foil.

TABLE II. 13-MHZ ANTENNA DESIGN PARAMETERS

Parameters	Rectifier single-ended coil	Receiver differential coil
Number of turns	3	7 (× 2)
Width [mm]	1	0.5
Spacing [mm]	0.3	0.3
Inner diameters [mm]	40 / 20	7.4
Inductance [nH]	725	838 (× 2)

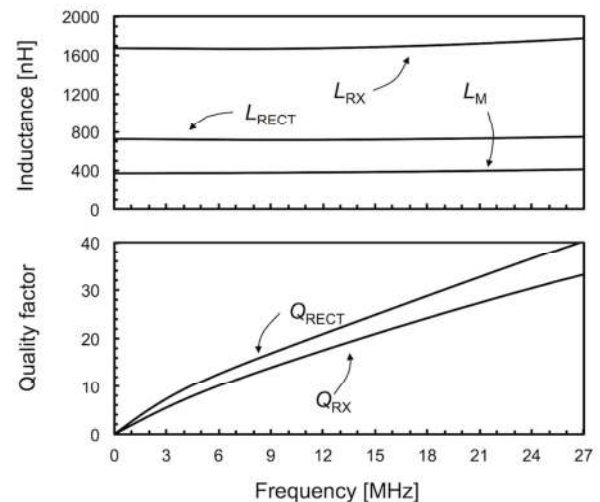


Fig. 9. Antenna electrical performance.

reader antenna and a 190-pF capacitance on the rectifier coil. The simulation results were further confirmed by S -parameter measurements of the fabricated samples, shown in Fig. 9. On the basis of the displayed antenna performance, for an equivalent load of 11 kΩ // 190 pF at the rectifier coil, the estimated 13-MHz voltage induced on both antenna coils is about 60 V_{pp}, provided that the maximum allowable magnetic field of 7.5 A/m is used according to ISO-IEC 14443-2. Moreover, system simulations confirmed that the induced voltage on antenna coils remains quite constant when reducing the reading distance. Indeed, the coupling coefficient increases at lower distances, but at the same time it worsens the impedance matching.

C. Rectifier and Modulator

The rectifier is often the bottleneck of passive RFIDs, especially in printed OTFT technologies whose transistor performance is affected by a high threshold voltage (V_T), typically in the order of several volts. Moreover, low carrier mobility and high parasitic capacitances further limit the frequency performance and hence the rectifier sensitivity. An experimental analysis on the rectifying potentiality of our technology in its first generation is carried out in [20] by testing diode-connected structures. This study pointed out the validity of threshold voltage cancellation techniques to improve the rectifier performance, even at high frequencies, when the mobility degradation plays a significant role in OTFTs. The schematic of the rectifier included in the RFID tag is shown in Fig. 10. It employs a 4-stage topology based on the Dickson charge pump [21], [22]. Differently from the previously adopted topology [15] that is a second-order solution [23], first-order threshold voltage compensation was preferred. The circuit uses mainly p-type transistors that perform better than n-type ones with only an n-type TFT first stage to make possible threshold-voltage compensation. Actually, the gate of the p-type (n-type) transistors is not shorted to the drain, but is connected to another node on the chain, which provides a lower (higher) dc voltage with the same ac phase of the drain signal. Specifically, the gates of M1 and M4 are connected to V_2 and the gates of M2 and M3 to ground and V_1 , respectively, according to the first-order threshold compensation scheme. This compensation technique, together with the multiple-stage approach, allows a reasonable V_{OUT} (i.e., V_{DD}) to be achieved, even at input voltages that are rather small compared with the TFT threshold voltages.

The modulator is implemented with an n-type transistor, which is connected to the rectifier input. The modulator changes the overall load of the rectifier coil according to the bit to be transmitted, thus performing backscattering.

D. Receiver

The key block of the receiver is the envelope detector (ED). Indeed, its performance determines the sensitivity of the overall receiver and the capability of demodulating ASK PWM-coded signals with low h , which is important to preserve high average power at the rectifier input. A simplified schematic of ED is shown in Fig. 11 along with a qualitative sketch of the main waveforms. The core of ED includes the p-type pair, M1-M2, the self-biased load performed by M3 and the low-pass filter $R_L C_L$, and the comparator, M4-M7. The input pair driven by the 13.56-MHz RF signal produces a pulsed current, i_O , whose slowly variable component within the RF period is related to the input envelope signal. Specifically, current i_O is composed of a high-frequency component, i_{RF} , (i.e., mainly even harmonics of the RF signal), an average component, I_{AV} , and the envelope signal, i_{ENV} . Component i_{RF} flows into the high parasitic capacitance, C_P , at the drain node of M1-M2, hence it is filtered out in a large amount. Current I_{AV} flows into M3 and produces the average output voltage, V_{AV} , thanks to the

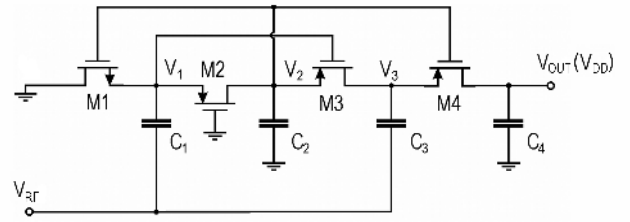


Fig. 10. Schematic of the rectifier.

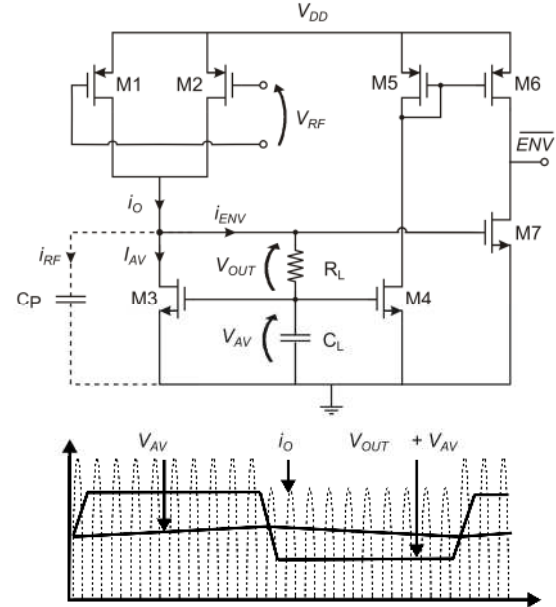


Fig. 11. ED schematic and qualitative sketch of the main waveforms.

diode connection of M3 through resistance R_L . Provided that $C_L \cdot R_L \gg C_L / g_{m3} \gg T_{BIT}$, low-pass filter $R_L C_L$ makes the gate of M3 a virtual ground and envelope signal i_{ENV} flows into R_L thus producing the output voltage, V_{OUT} , i.e. $R_L \cdot i_{ENV}$.

The “conversion gain” of the detector is related to R_L and the non-linear transconductance gain of the input pair. The self-biased load is a robust solution to deal with wide threshold tolerances and large RF input ranges. In our implementation, a resistance R_L of 40 M Ω was integrated. A discrete capacitor of 6 nF was mounted for C_L on the same foil of the antenna for testing purposes. In comparison with more traditional diode-based ED schemes, the proposed topology shows several advantages.

- It guarantees a high output voltage thanks to the higher conversion gain with respect to traditional solutions (diode-connected rectifiers [8]-[9] or common drain topologies [24]). This avoids further amplification before the comparator, which would entail high ac-coupling capacitors to arrest offset and further current consumption.
- It has high input impedance, thus minimizing the power drawn by the reader.
- It is suitable for ASK signals with low h thanks to the envelope-signal gain.

It is also worth noting that the differential-like topology of the input transistors allows compensation of the detrimental effect of the gate-drain capacitances. Indeed, a single-ended ED is

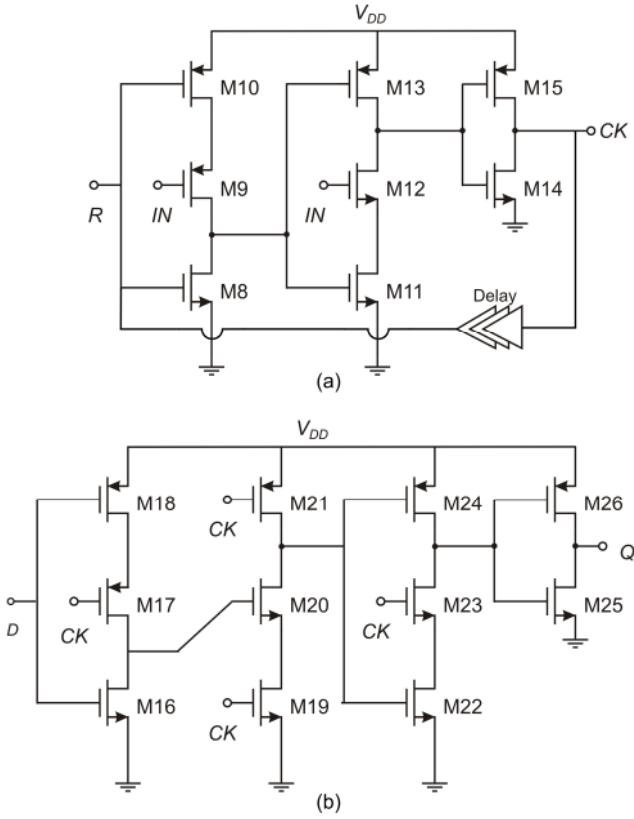


Fig. 12. Schematics of the clock decoder (a) and D-FF (b) [15].

not a good solution in this technology, due to the large overlap capacitance. Finally, a simple pseudo-differential comparator, M4-M7, provides at the ED output a quasi-rail-to-rail signal, \overline{ENV} , which is large enough to drive the digital circuits.

The decoder digital circuits that recover data and clock (see Fig. 2) are implemented with dynamic logic cells to reduce transistor count and current consumption. The schematics of the clock decoder and the D-FF used for data recovery are shown in Figs. 12(a) and 12(b), respectively. The clock decoder exploits a customized topology, which minimizes the transistor count with respect to the traditional D-FF with reset. This simplification is made possible since both inputs R and IN are low before the beginning of a new bit, according to the coding scheme. The delay is implemented by a cascade of four inverters loaded by a capacitance (C_{DELAY}).

E. Code Recognition Unit

The code recognition unit shown in Fig. 2 includes the two modules, RM and IVM, responsible for the tag synchronization and identity recognition, respectively. Both modules were designed using a transmission gate (TG) based approach. Indeed, TG-based logic guarantees presently lower area compared to fully-static implementations (around four times smaller in our technology) and higher robustness compared to dynamic logic and therefore is a good solution for complex digital circuitry. A detailed schematic of the code recognition unit is shown in Fig. 13. In RM, a 2-bit counter adds up the number of zeros in the input code (any “one” in the input resets the counter). After receiving four consecutive

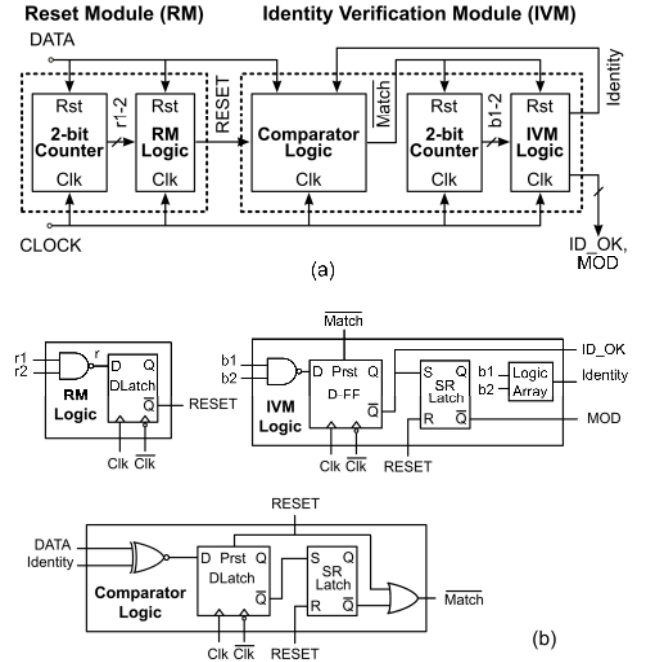


Fig. 13. Code recognition unit. (a) Block diagram. (b) Simplified schematics.

zeros (i.e., $r_1 r_2 = 11$ and $r = 0$), RM sends the reset signal, RESET, to IVM. This will announce the arrival of a new identity code to IVM by clearing all its FFs and latches. If there is a discrepancy between clock and data (e.g., the data is delayed with respect to the clock), signal “ r ” may go temporarily high, before the counter is reset by the arrival of next “1” in the data flow. Since RESET is used to activate/lock some SR-latches asynchronously, it is important to prevent such temporary wrong activations. The D-latch in RM Logic block eliminates the possibility of sending such a false reset. The identity comparison is performed in the Comparator Logic block through an XOR gate. At each clock, the 2-bit counter and a logic array generate at the output of the Comparator Logic the correct tag identity code corresponding to the bit being received (the logic array is included in the IVM Logic block). In case of un-match the comparator output, $\overline{\text{Match}}$, goes high and resets the counter. In this case $\overline{\text{Match}}$ remains active till the next RESET is received, resetting $\overline{\text{Match}}$ to zero. Otherwise, the operation will continue till all bits of the identification code are received and successfully compared. When this happens, the counter “Carry” bit generated in IVM Logic will go high and set ID_OK active, thus triggering the reply back by the tag. The output signal, MOD, which activates a ring oscillator, remains high until the next RESET is received. It is worth noting that the tag answers with a message (using the modulator) only after the correct code is received, according to the silent tag identification scheme.

III. EXPERIMENTAL RESULTS

The tag was fabricated on a PEN foil, as shown in Fig. 14. The photo highlights the macro-blocks constituting the circuit that are the rectifier, the receiver, and the code recognition unit. The overall active area of the circuit is 54 cm^2 . The area

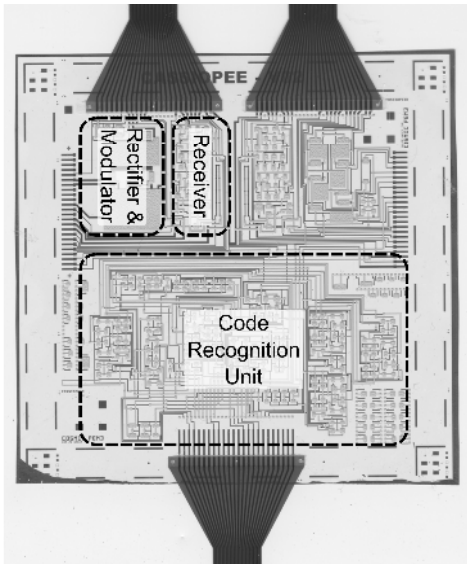


Fig. 14. Photo of the RFID tag foil bonded to flexible flat cables.

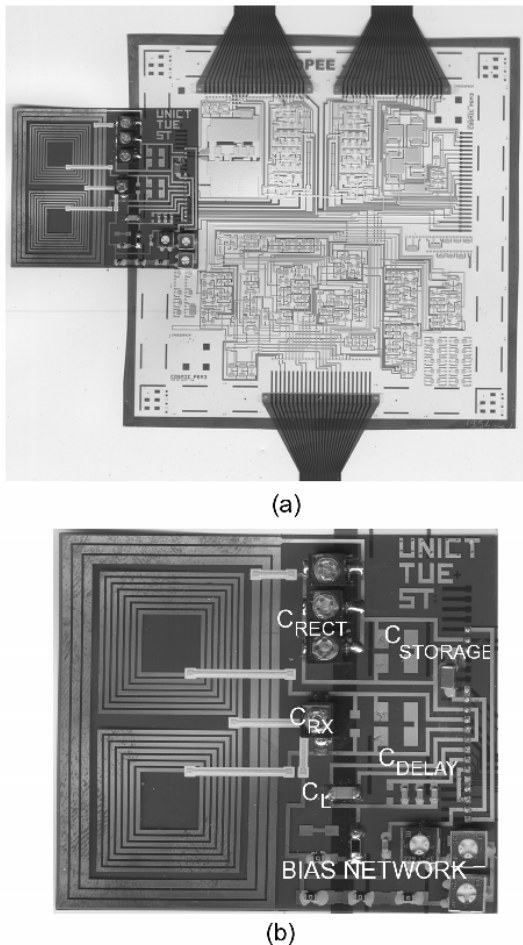


Fig. 15. (a) Photo of the complete RFID tag. (b) Detail of the 13-MHz antenna foil with SMD components soldered on it.

in the right top quarter of the foil was used for other circuitry. Two flexible flat cables were bonded on the top and bottom of the foil using isotropic conductive glue. The flat cables were adopted to interface the tag with the lab instruments by means of a test board and make possible a complete characterization

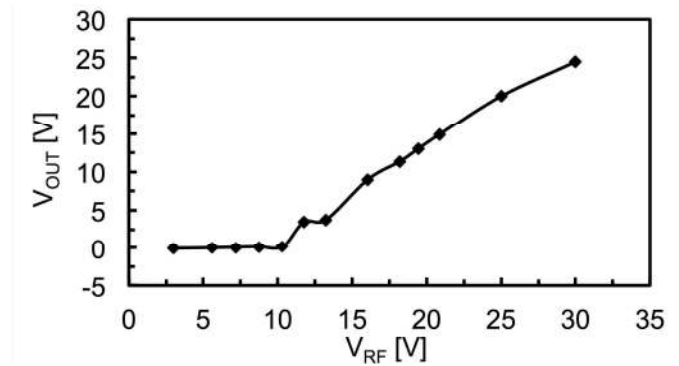


Fig. 16. Measured output voltage of the rectifier versus the RF input.

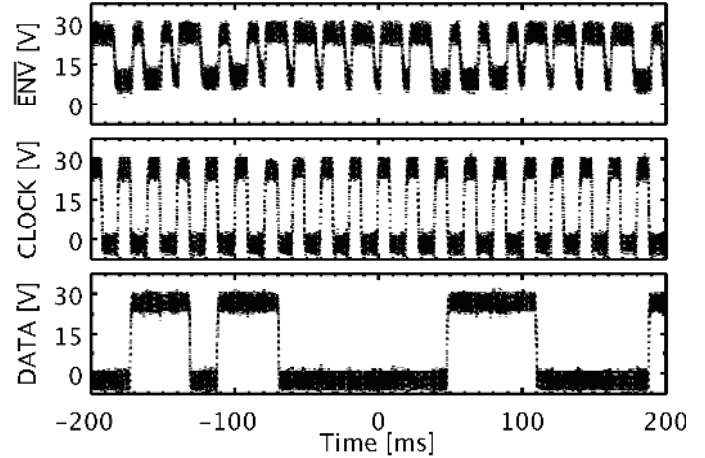


Fig. 17. Measured output signals of the receiver ($V_{DD}=30$ V, $h=30\%$).

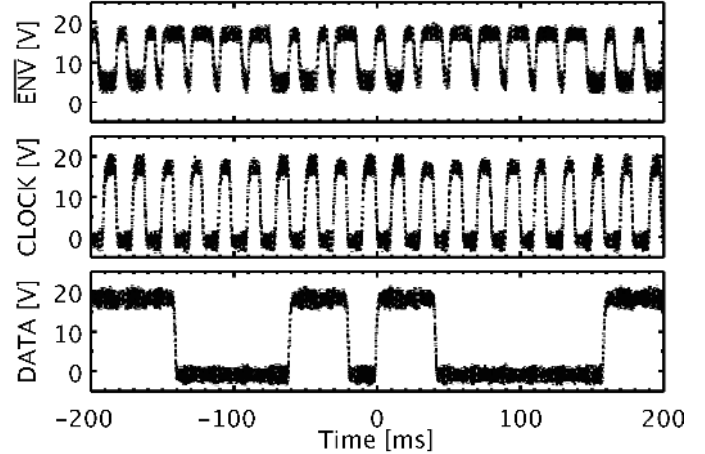


Fig. 18. Measured output signals of the receiver ($V_{DD}=20$ V, $h=30\%$).

of both the overall circuit and the single macro-blocks before antenna assembling. To allow this test flexibility, the circuit macro-blocks were not directly connected on the PEN foil, but connections were performed by taking advantage of the antenna foil. To complete the tag, the PEN foil was then bonded to the polyimide foil with the antenna, as shown in Fig. 15. The polyimide foil was also used to house the two capacitors for the antenna matching networks (i.e., C_{RECT} and C_{RX}), few passive components of the receiver (i.e., bias resistances, C_L , and C_{DELAY}), and the storage capacitor of the rectifier, $C_{STORAGE}$. The discrete capacitors, C_{RECT} , C_{RX} , C_L , and C_{DELAY} , can be directly printed on the RFID foil thanks to

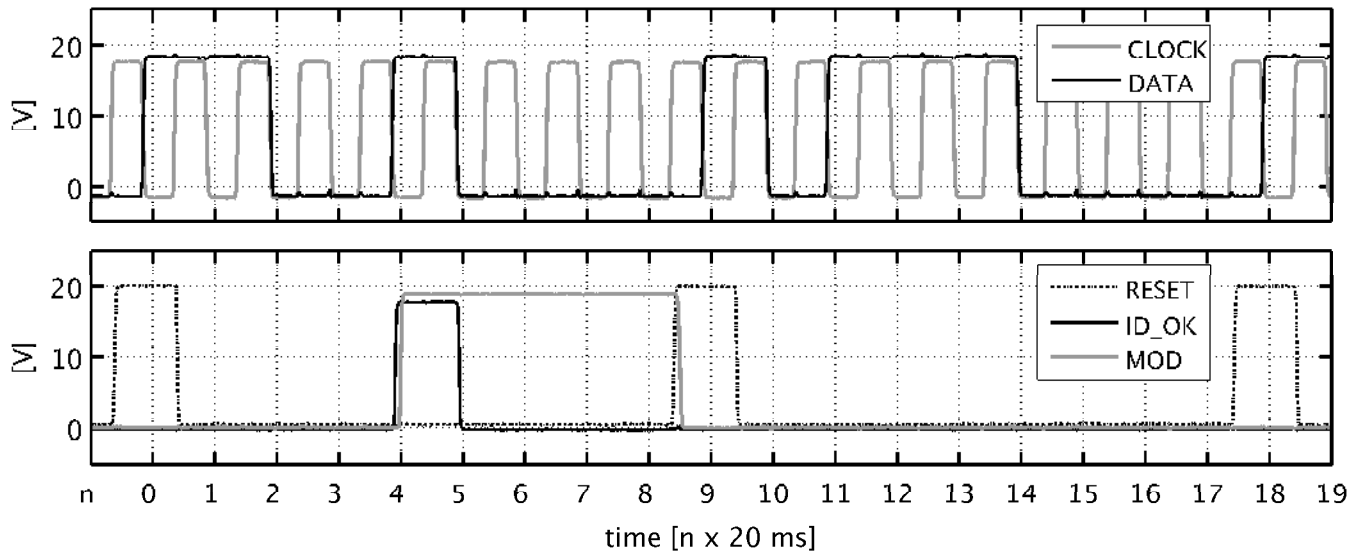


Fig. 19. Measurements of the code recognition unit for a 60- V_{pp} , 30% modulated RF input at 20-V supply voltage.

the high-density (i.e., 2.15 nF/cm²) MIM capacitor provided by the adopted C-OTFT technology. As mentioned before, the antenna foil was also used to connect together the tag macro-blocks thus allowing their standalone characterization in the PEN foil. The available 8- μ m thick Cu metal was exploited for connections. In the following, experimental results of each macro-block and the complete tag are discussed. Measurements were carried out on a total of 7 RFID samples.

The rectifier was characterized under different amplitudes of the sinusoidal RF input with an equivalent full-tag load of 0.7 M Ω . It generates an output voltage (V_{DD}) of 25 V for a 13.56-MHz input signal, V_{RF} , of 60 V_{pp} . Output voltage measurements as a function of the RF peak voltage are summarized in Fig. 16. Figs. 17 and 18 show the main measured signals of the receiver for a 60- V_{pp} RF input with h of 30% at 30-V and 20-V power supply, respectively. It is worth noting that due to the lower supply voltages and hence the reduced current capability at sub-threshold operation, ED requires an RF input signal larger than the supply voltage. Fig. 19 shows the measurement of the code recognition unit at 20-V supply voltage for a 60- V_{pp} , 30% modulated ASK RF input. Two different identity codes were adopted in this work, with one time programmability enabled by laser trimming. In the reported test, the reset signal code is “10000”, the tag identity code is “0011”, and the un-match code is “1011”. As expected, the measured signal ID_OK goes high only after the sequence “1100” is received (i.e., $n=4$ in Fig. 19), thus triggering the reply back. Signal MOD is high only after the correct identity code is received. It goes low after subsequent signal RESET goes high (i.e., $n=9$ in Fig. 19). The functionality of the code recognition unit was successfully verified for several supply voltages, from 40 V to 20 V.

The complete RFID tag together with the flexible antenna was tested thanks to two interface boards, as shown in the measurement setup in Fig. 20. The RFID was successfully

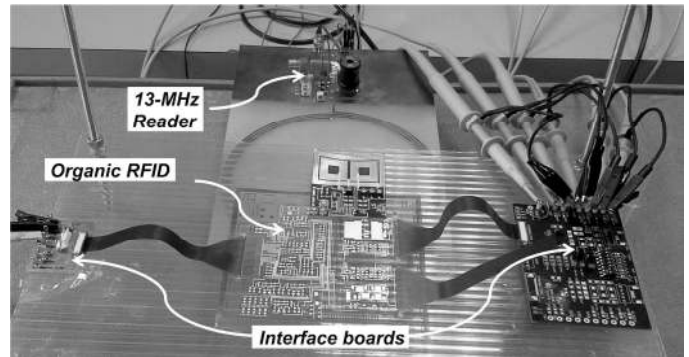


Fig. 20. Measurement setup for the printed C-OTFT RFID tag.

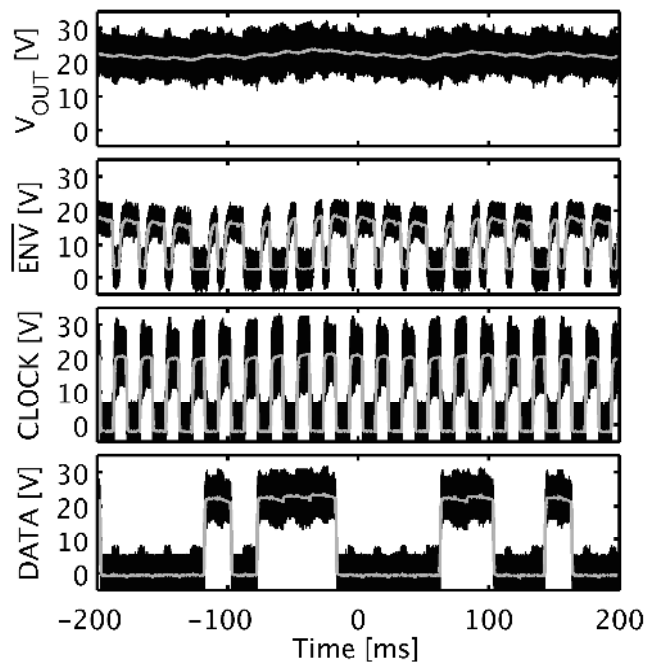


Fig. 21. Tag measurement waveforms for a 60- V_{pp} , 20% modulated 13.56-MHz input signal.

tested with a 60-V_{pp} RF input voltage. For h of 50%, 30%, and 20%, the measured rectifier output, V_{OUT} , was 20 V, 22 V, and 24 V respectively. Little variation was observed for a reading range from 2 cm to 5 cm. The rectifier output and receiver main signals for a 60-V_{pp} RF input are shown in Fig. 21 with and without averaging. The 20% ASK modulation of the input signal can be recognized by looking at the RF noise in signal DATA. As far as the modulator is concerned, the glue attachment affected the functionality of some TFTs since the modulator was placed too close to top flat cable contacts. This drawback prevented from characterizing the transmission link.

Main performance of the proposed organic RFID tag is summarized in Table III.

TABLE III. SUMMARIZED RFID PERFORMANCE

Parameter	Values
RF frequency (f_{RF})	13.56 MHz
Modulation depth (h)	50–20%
Supply voltage	20–24 V
Reading range	2–5 cm
Code bits	4
Max. bit rate	50 bit/s
Antenna area	15 cm ²
Circuit area	54 cm ²

IV. CONCLUSION

The implementation of an integrated 13.56-MHz RFID tag in a printed C-OTFT technology on flexible substrate has been successfully demonstrated for the first time. The circuit is the most complex mixed-signal integrated system ever published in printed C-OTFT technology, with more than 250 organic TFTs on the same foil. Its functionality was verified at a supply voltage as low as 24 V, thus demonstrating the potential of sub-threshold operation for C-OTFTs.

This work advances the state of the art since it demonstrates the implementation of a very complex system on a printed organic technology using several techniques at different levels: system (i.e., secure identification scheme and ASK modulation), technology (i.e., flexible antennas and C-OTFT technology), tag architecture (i.e., three-coil antenna), and circuit (i.e., active envelope detector and sub-threshold operation).

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Vincenzo Fiore (M'13) received the Master degree in microelectronics, from the University of Catania, Italy, in 2012. He is currently pursuing the Ph.D. in Systems Engineering at the same university. Since 2011, he has been with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by University of Catania and STMicroelectronics, where he is involved in the design of mixed signal and RF ICs, mainly focused on galvanic-isolated integrated systems. In last years, he worked in the field of organic electronics within the framework of the COSMIC European Research Projects.



Projects.

Placido Battiato received the Bachelor degree in electronic engineering from the University of Catania, Italy, in 2012. He is currently pursuing the Master degree in Microelectronics at the same university. From November 2012 to May 2014 he was with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics. In this period, he worked in the field of organic electronics within the COSMIC European Research



Sahel Abdinia received her M.Sc. degree in Electrical Engineering from K.N.Toosi University of Technology, Tehran, Iran, in 2009. Since 2010, she has been a Ph.D. candidate at Eindhoven University of Technology, in mixed-signal microelectronics group. Her research activities include Analog, digital, and mixed-signal IC design for large-area electronics based on organic technologies.



Stephanie Jacob received the M.S. degree in Microelectronics and Telecommunications from the Ecole Polytechnique Universitaire de Marseille, France, in 2004 and the Ph.D. degree in microelectronics from the University of Provence, France, in 2008. Her Ph.D. work was carried out in CEA-LETI and ATMEL Rousset, France, on the integration, characterization and modelling of silicon nanocrystal memories. Since 2008, she has joined CEA-LITEN, France to work on the electrical characterization and modelling of organic transistors on flexible substrate. She is the co-author of more than 20 papers in international journals and conference proceedings.



image sensor, user interfaces, conformable sensing surfaces etc.

Isabelle Chartier is graduated as an engineer in general optics from the Institut d'Optique – Paris, France in 1986 and joined CEA-Grenoble in 1989. She is currently Business manager for Printed Electronic at CEA-LITEN. Since 2012 she is director of PICTIC, the French Printing Platform for Organic Electronics development, prototyping and industrialization focused on Large Area Sensing Surface integrating printed OTFT, sensors and actuators. PICTIC is addressing applications such as



Romain Coppard obtained the Ph.D. degree in semiconductor device physics in 1984. He has been working in the field of organic electronics since 2007, and held before various positions at major silicon microelectronics companies (Alcatel, Applied Materials, ATMEL). He is currently heading the Laboratory of Printed Electronics Devices in CEA Liten (Grenoble, France), in charge of developing the sheet-to-sheet printed organic CMOS technology for the COSMIC project. He held 5 patents and co-authored more than 50 papers.



Gerhard Klink studied physics with focus on surface science at the Technical University Munich. After finishing his studies with the diploma degree in 1987 he joined the Fraunhofer Society, where he started to work on microsystems technology. During different research projects he acquired a profound knowledge on thick and thin film technology in the fields of hybrid circuits, electronic packaging, sensors and actuators. Since 1998 he is working on process development for flexible electronic systems and corresponding roll-to-roll manufacturing methods. At present he is managing the Polytronic technology group and has lead several projects in Organic and Large Area Electronics.



Eugenio Cantatore (M'98-SM'14) received his Master and Ph.D. Degree in Electrical Engineering from Politecnico di Bari, Bari, Italy in 1993 and 1997 respectively. From 1994 to 1999 he was first a Ph.D. student and then a fellow at the European Laboratory for Particle Physics (CERN) Geneva, Switzerland. In 1999 he moved to Philips Research, Eindhoven, The Netherlands as senior scientist and in 2007 joined the Eindhoven University of Technology where he is associate professor. His research interests include the design and characterization of electronic circuits exploiting emerging technologies as well as the design of ultra-low power micro-systems for medical applications. Dr. Cantatore authored or co-authored more than 120 papers in journals and conference proceedings, and 13 patents or patent applications. He is active in the Technical Program Committees of ESSDERC, ESSCIRC and ISSCC and has been member of the Executive Committee of ISSCC. Since 2013 he is chair of the Technology Directions subcommittee of ISSCC. In 2006 he received from ISSCC the Beatrice Winner Award for Editorial Excellence and was nominated in the Scientific American top 50 list. He received the Philips Research Invention Award in 2007 and in 2012 the Best Paper Award from ESSDERC.



Egidio Ragonese (M'03-SM'12) received the Laurea degree in electronic engineering and the Ph.D. degree in electronics engineering from the University of Catania, Italy, in 1999 and 2003, respectively. Since 1999 he has been with the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by the University of Catania and STMicroelectronics. In 2003 and 2008, he joined the DIEEI at the University of Catania as Research Associate and Assistant Professor, respectively. Since October 2011, he has been with STMicroelectronics, Catania, Italy. His research interests included RF transceivers for wireless communications and mm-wave circuits for radar applications. Dr. Ragonese is co-author of 60 papers, several patents and two books. Recently, he has been also active in the field of organic electronics within two European Research Projects.



Giuseppe Palmisano (M'08-SM'09) received the Laurea degree in electronic engineering from the University of Pavia, Pavia, Italy, in 1982. From 1983 to 1991, he was Researcher with the Department of Electronics, University of Pavia, where he was involved in CMOS and BiCMOS analog integrated circuit design. In 1992, he was a Visiting Professor with Universidad Autonoma Metropolitana (UAM), Mexico City, Mexico, where he taught microelectronics for Ph.D. students. In 1993 and 2000, he joined the Faculty of Engineering at the University of Catania, Catania, Italy, as Associate Professor and Full Professor, respectively, teaching microelectronics. Since 1999, he has been leading the Radio Frequency Advanced Design Center (RF-ADC), a joint research center supported by University of Catania and STMicroelectronics, Catania, Italy. He has supervised the design of several innovative analog integrated circuits and systems within the framework of national and European research projects and in collaboration with electronic industries. He is the coauthor of more than 250 papers in international journals and conference proceedings, around 50 international patents, and 3 books. His research interests lie in the area of analog integrated circuit design with special emphasis to RF applications. Recently, he has been facing remotely-powered transceivers with RF energy harvesting and printed electronics with organic thin film technologies.