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An Integrated 16-channel CMOS Time-to-Digital Converter

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ABSTRACT

An integrated 16-channel time-to-digital converter (TDC) for use in the NA48 experiment at CERN has been developed in a 1 μm CMOS technology. The resolution is 1.56 ns and the total time history is 204.8 ms. Buffering of up to 128 hits is done in on-chip FIFOs. The chip area is 25 mm^2. The vernier circuit consists of a 16-tap voltage-controlled delay chain controlled by a delay locked loop (DLL). Readout is possible at 40 MHz. A JTAG/IEEE 1149.1 protocol has been incorporated to allow in-site testing of the chip. The JTAG data path is also used to access internal control and status registers.

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Abstract

An integrated 16-channel Time to Digital Converter (TDC) for use in the NA48 [1] experiment at CERN has been developed in a 1μm CMOS technology. The resolution is 1.56ns and the total time history is 204.8ms. Buffering of up to 128 hits is done in on-chip FIFOs. The chip area is 25 mm². The vernier circuit consists of a 16-tap voltage-controlled delay chain controlled by a Delay Locked Loop (DLL). Read out is possible at 40 MHz. JTAG/IEEE 1149.1 protocol has been incorporated to allow in-site testing of the chip. The JTAG data path is also used to access internal control and status registers.

1. INTRODUCTION

The high number of measuring channels in future high energy physics experiments requires the use of highly integrated electronics. With high integration comes lower power consummation and cost per channel as a supplementary benefit. The present chip allows the NA48 experiment at CERN to build boards containing 256 TDC channels.

NA48 is a fixed target experiment designed to measure CP violation with high precision. The experimental apparatus includes a magnetic spectrometer consisting of two sets of two drift chambers [2] separated by a central dipole magnet. Each drift chamber consists of four wire planes, measuring the X, Y, U and V coordinates. The (U,V) frame is rotated 45 degrees with respect to the (X,Y) frame. Each drift chamber view consists of 512 wires. The total number of used wires is 6144. A spatial resolution of 100μm is expected to be achieved by off-line reconstruction, provided the timing resolution of the TDC is better than 2ns. For the NA48 TDC we chose to divide the 40MHz global synchronization clock in 16 bins, resulting in a theoretical time resolution of 1.56ns.

In the NA48 data acquisition system the hits in the chambers are individually time-stamped at capture time. The data flow is thus not required to be in strict temporal order, since all data carry their detection time-stamp.

2. CHIP ARCHITECTURE

A block-diagram of the TDC chip is shown in Figure 1. It consists of the vernier measurement block with its associated delay locked loop circuitry and a coarse time measuring circuit. The TTL compatible hit inputs set the hit flip-flops which act as glitch filters. Data is stored internally in a FIFO before being read out. The vernier allows time measurements with a resolution of 1/16th of the 40MHz reference clock. The coarse-time circuitry measures time with 25 ns resolution.

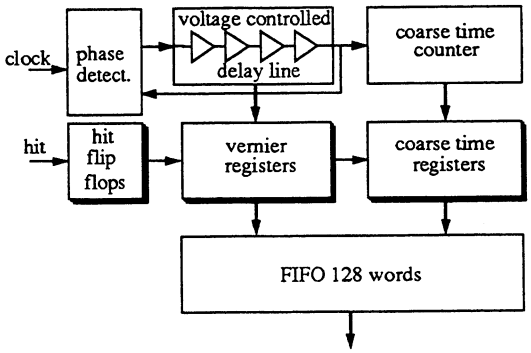

Fig. 1 : Block diagram of the TDC.

3. VERNIER MEASUREMENT

3.1 Principle of operation

The vernier measuring circuit contains 16 timing registers. It achieves a time resolution of 1/16 th of the 25ns clock period [3]. A Delay Locked Loop (DLL) containing a delay chain controlled in such a way that the total delay between the reference input clock and the output of the delay chain is maintained at exactly one clock cycle.

The vernier timing measurement for each channel is performed by storing the state of the delay chain when a hit signal is asserted. The timing of the hit can then be determined by finding the position of the 0 to 1 transition in the vernier register.

Loading of the vernier register is controlled by an internal D-type flip-flop for each channel. This flip-flop prevents a new time measurements to be loaded into the vernier register before the current value has been transferred into the read-out FIFO.

3.2 The voltage controlled delay element

As shown in Figure 2, each delay element consists of four inverters: one to delay the falling edge, one to delay the rising edge and two inverters performing buffering and signal reshaping.

The delay of the signal is performed by current starving the NMOS transistors of the inverters. This configuration has been chosen because it allows building delay elements without control of PMOS transistors. The current starving transistors (M6, M10) are shunted by weak transistors (M5, M9) in order to limit the delay at low control voltage. The shunt devices have been dimensioned so as to ensure symmetrical rising and falling edges.

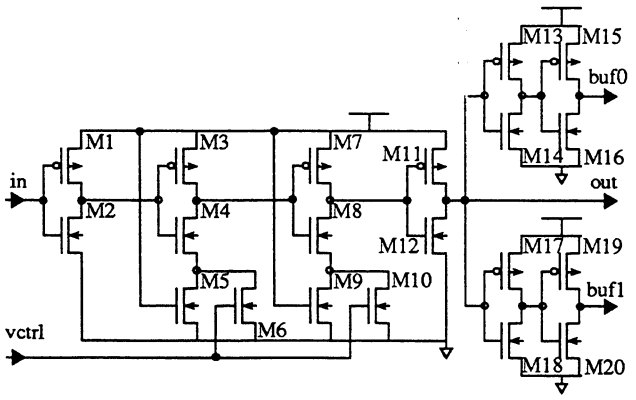

Fig. 2 : Schematic of the four inverter delay element

The voltage vs. delay characteristics has been designed to cover the full range between worst and best case with respect to process, voltage and temperature. As shown in Figure 3, the delay element has been carefully designed to provide a well matched delay of rising and falling edge within the usable control voltage region.

The sensitivity of the delay elements to power supply noise has been analyzed and found to be negligible for this design.

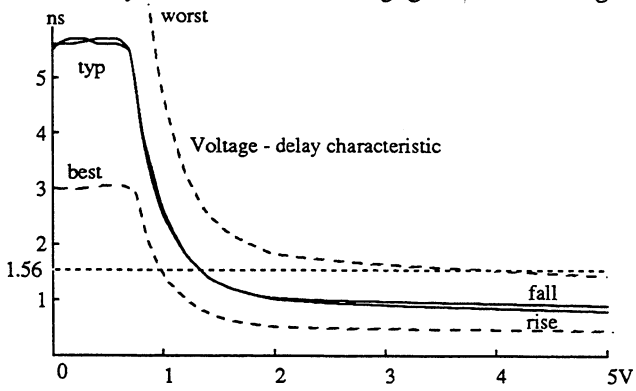

Fig. 3 : Delay characteristics of a delay element

3.3 The delay locked loop

The DLL, shown in Figure 4, continuously measures the phase of the output of the delay chain with respect to the input clock signal and adjusts the delay elements by changing their delay control voltage.

The phase detector controls a charge pump that adds/removes charge from a filter capacitor thereby changing the delay control voltage.

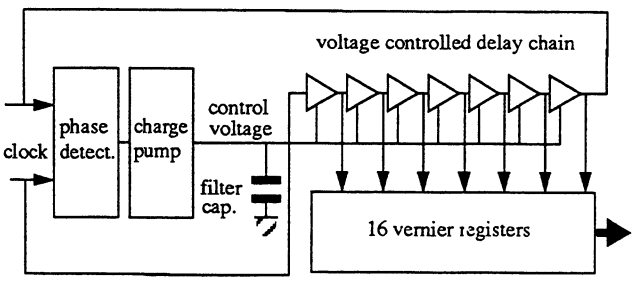

Fig. 4 : Delay locked loop

3.4 The phase detector

Figure 5 shows the phase detector which is made from three cross-coupled RS-latches. It determines if the rising edge of the reference clock (A) occurs before or after the rising edge of the delayed clock (B). If A occurs before B the output is 1 otherwise the output is 0. This output is used directly to control the charge pump either to increase or to decrease the control voltage for the delay elements. The phase detector used in this design ensures locking when the phase difference lies between half a clock cycle and one and a half clock cycles.

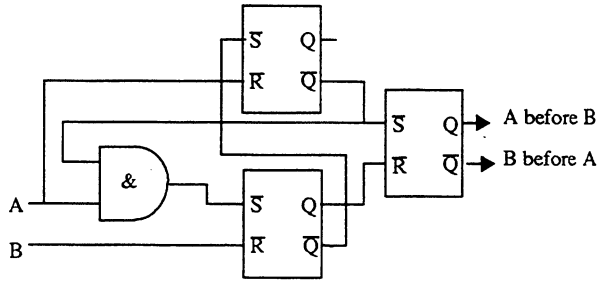

Fig. 5 : Functional diagram of the phase detector.

Special care has been taken to ensure a symmetrical implementation of the phase detector in order to obtain good phase resolution around the locking point. The input load and wiring capacitance seen by the delayed clock signal has been matched to the input capacitance of a delay element. This way all delay elements see the same load.

3.5 Charge pump and loop filter

The charge pump adds or removes charge from the filter capacitor based on the phase comparison performed by the phase detector. Charge is removed/added by turning on current sources/sinks to either vdd or ground.

A significant amount of capacitive coupling exists between the controlling gates of the current starved inverters in the delay chain and the filter capacitor. This coupling can generate noise when the delay element propagates an edge. However, because there is always a rising edge and a falling edge propagating through the delay chain when locked, the total noise contribution averaged over a clock cycle is zero.

The filter capacitor is implemented as a PFET transistor used in accumulation mode with the N well connected to ground. The total capacitance is around 200pF, corresponding to an area of about 0.1 mm^2.

3.6 The vernier register

Loading the state of the delay chain into one of the 16 vernier registers is triggered by a hit signal, as shown in Figure 6. The hit signal is used as the clock for the hit flip-flop. The hit flip-flop allows enabling and disabling of individual channels and at the same time acts as a glitch filter. A buffered version of the output of the hit flip-flop is used by the control logic and to store the coarse counter value.

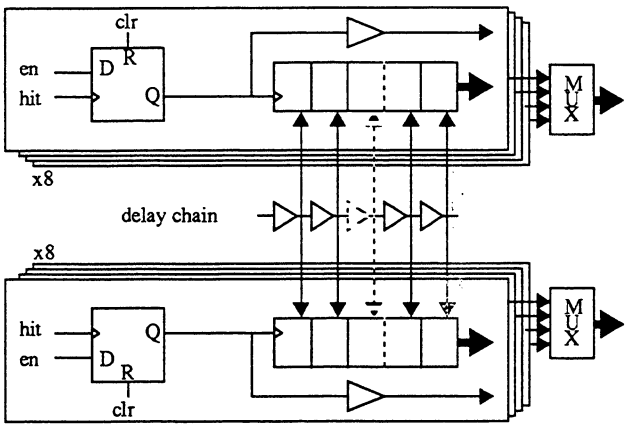

Fig. 6 : The vernier registers.

When sampling a signal asynchronously there is always a finite probability that the sampling clock arrives exactly when the input is changing. In this case the flip-flop may enter a metastable state [4] for an indeterminate time. If this happens the outcome of the sample operation is unpredictable. If several signals are sampled at the same time it is important to make sure that only one signal changes at any one moment. In the TDC under normal working conditions there is only one 0 to 1 transition propagating in the delay chain.This ensures that the sampling uncertainty is less than 1 least significant bit (lsb).

The vernier registers have been carefully designed to minimize the timing difference between the 16 channels. The input capacitance of the hit signals have been matched to minimize time difference between the channels when driven by equally sized drivers. The outputs of the 16 vernier registers are multiplexed in two groups of 8 channels.

Great effort has been made to enable precise timing measurements to be performed by the TDC. The internal delays for the clock input and the hit signal are matched. Changes with voltage and temperature are only minor and can be corrected by recalibrating the system.

4. COARSE TIME MEASUREMENT

A coarse time counter extends the dynamic range of the TDC to cover more than one clock cycle. At the same time as the state of the delay chain is transferred to the vernier register, the value of the counter is transferred to a corresponding coarse time register, Figure 7 shows this. To make sure that the counter is not sampled when it is changing state, a scheme with two coarse time counters is used

Two central 13-bit master counters driven by a delayed system clock are distributed to all channels. The first counter is clocked with the falling edge of a clock derived by delaying the system clock a quarter of a period and the second counter with the rising edge of same clock. When a hit arrives the values of the two counters are stored in the registers corresponding to that channel.

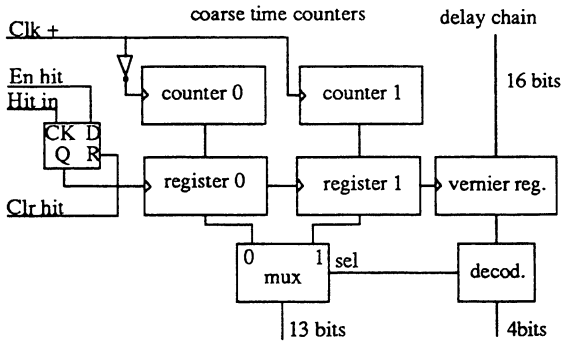

Fig. 7 : Block diagram of the coarse time counters.

The decoded value of the corresponding vernier register determines which coarse time register to choose. If the decoded vernier value is between 0 and 7 then the first register is used, if between 8 and 15 the second register is used. This method ensures that the coarse time registers are not subject to marginal set-up and hold times, as shown in Figure 8, which could produce erroneous coarse time values and thus degrade the precision of the TDC [6].

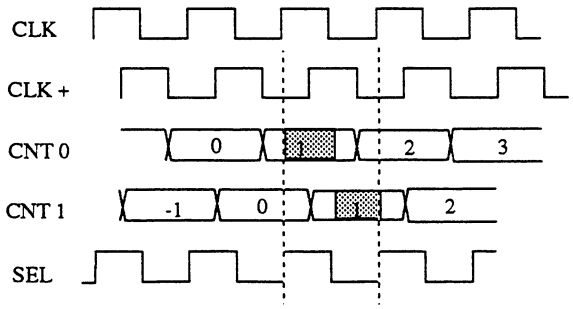

Fig. 8 : Timing diagram for the coarse time counters.

5. BUFFERING AND READ-OUT

When a hit arrives on a channel the hit flip-flop is set, which then clocks the vernier value into its register. At the same time the two coarse time values are latched into their registers. The output of the hit flip-flop is synchronized to the system clock and fed to a priority encoder. A small controller based on a state machine is started as soon as a hit is present in the priority encoder. The output of the encoder is then used to select one of the channels through a set of multiplexors. When the data (channel-identifier and time) from the selected channel has been written into a FIFO, the hit flip-flop is cleared and the state machine proceeds to process a new channel. To speed up buffering there are two independent FIFOs with their corresponding control logic. The cycle-time of the FIFOs correspond to the system clock. If all 16 channels are hit simultaneously the internal buffering takes 275ns (3x25ns + 8x25ns). Since the internal buffering is done on a priority basis, the ordering of the data in the FIFOs is according to the prevailing highest priority during each clock i.e. the data is not necessarily ordered according to

time of arrival. For the NA48 experiment this is acceptable, since an asynchronous data acquisition system relying on time-stamping of hits will be used.

5.1 Read out of the TDC

During read-out, the two FIFOs are multiplexed onto the output drivers. The FIFOs provide an EMPTY signal to the external logic and accept a READ signal. The output of the FIFOs is tristateable to enable several TDC chips to share one read-out bus.

6. SERIAL PROTOCOL AND HIT-COUNT

In the TDC chip the JTAG/IEEE 1149.1 [5] protocol is used for setting up internal control registers and to some extent for testing. JTAG is a simple 4 wire serial protocol consisting of a clock TCK, a mode-select TMS, data-in TDI and data-out TDO. By controlling the TMS line together with the TDI different internal registers can be accessed. Loading of a register is accomplished by feeding serial data onto the TDI pin after having selected the register, at the same time the previous contents are shifted out to the TDO pin. Several chips can be connected in series but still be accessed individually by selecting an internal bypass register in all but one chip.

6.1 Coarse-counter offset

A JTAG register holds an offset for the coarse time counters. An external signal can be used to load the offset value into the coarse time counter. This feature is used in order to align the time-stamps of all TDC chips in a system.

6.2 Test facilities

One register can be pre-loaded with the wire-number and time. When the test input is activated this value is written into the FIFO through the normal data path. By using this method a large part of the data path can be tested. It can also be used to generate events to test the trigger logic.

The channels can be individually enabled through a JTAG register. This can be useful in order to remove faulty or noisy channels.

6.3 Counting of simultaneous hits.

An adder circuit sums the number of hits present for each clock cycle. This is used to indicate to the external trigger logic those events that produced too many hits. In the NA48 experiment the TDC FIFOs are cleared if the current number of hits or the number of hits accumulated by external logic during four clocks exceed a predetermined threshold.

7. RESULTS

As the NA48 TDC is driven by the global synchronization clock the over-all linearity is as good as the stability of that oscillator. The integral linearity error shows the deviation from the ideal linear curve and is shown in Figure 9. The shape is not far from the theoretical, showing very small jitter and bin size variations in the delay chain and no large-scale non-linearities. The curve is obtained by making a sweep with a high precision delay generator then histogramming the residuals after a linear fit. The differences in the width of the bins is of the order of 100ps, including imperfections of the delay generator.

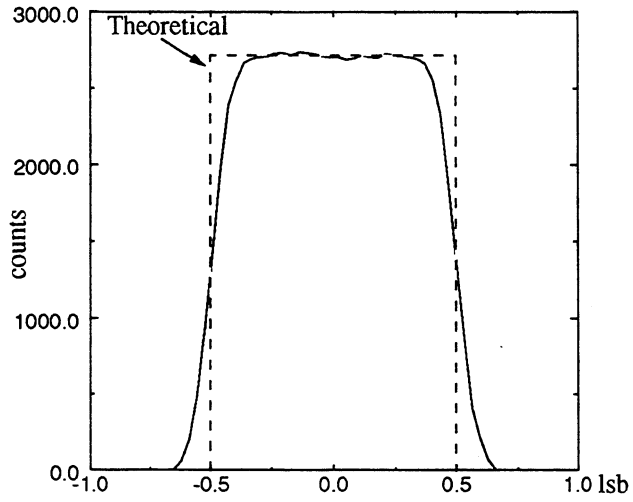

Fig. 9 : Differential non-linearity in lsb's

The performance is also demonstrated by the measurement of the difference in arrival-time between two signals in Figure 10. The signals are fed to different channels with a fixed delay between them. The delay was chosen to be 10 lsb. One would expect a spread over three bins at the most, only taking into account the phenomenon of metastability and disregarding jitter in the delay chain. The signals were random with respect to the TDC clock. The chip shows similar behaviour when the difference between the two signals is larger.

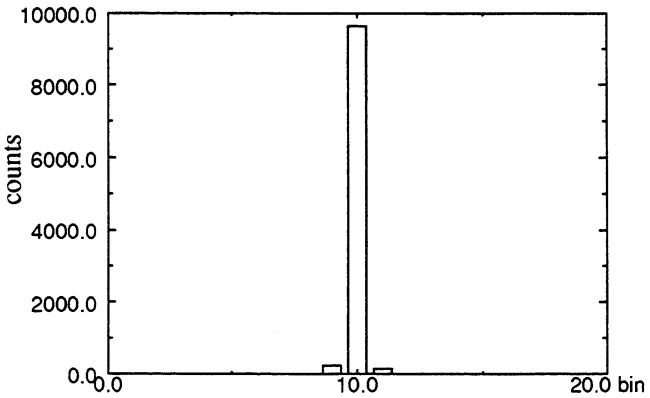

Fig. 10 : Measurement of a fixed delay of 10 lsb's

The power consumption of the chip is approximately 10mW/channel under normal working conditions, thus no special cooling is required for the 68 pin PLCC package.

8. FUTURE DEVELOPEMENTS

The NA48 TDC chip has been designed for a time resolution of 1.56 ns required in this specific application. For future detectors where more accurate time measurements are needed, we are developing improved TDC circuits.

A test chip is being designed containing 32 channels per chip and a time bin size of 0.5ns. To obtain this resolution a two inverter delay element with current starving on both the NMOS transistor side and the PMOS transistor side is being used and a CMOS process of 0.7μm gate length is required. Additional buffering to improve the double pulse resolution is included in this design and a read-out architecture enabling the measurements to be read-out in time sequential order is being considered.

An alternative DLL with a potential time resolution of 100-200 ps is being evaluated for a clock alignment and adjustment system [7]. A TDC of this resolution also have potential applications in time of flight measuring detectors.

9. ACKNOWLEDGEMENTS

Many thanks to E.Murer who designed the test-board and to C. Paillard who in spite of our limited resources managed to build a test-system and write the test-software.

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