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An Integrated Buck and Half-Bridge High Step-Down Converter

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Abstract: In this paper, an integrated buck and asymmetrical half-bridge (IBAHB) high step-down converter utilizing a single-stage driving design for highly efficient energy conversion is proposed. The proposed converter is able to instantly and synchronously transfer energy from input to output within one conversion period. The advantages of high step-down conversion, lower voltage stress and fewer semiconductor elements verify the feasibility of this proposed topology. The turns ratio of the transformer can be reduced to increase the coupling rate, which decreases the leakage inductance. The proposed integrated topology utilizes the single-stage energy transfer control algorithm to verify that the proposed experimental circuit has a full-load efficiency. This development will achieve the market's demand for high-buck converters and other related products and the competitive advantage of growing with the trend.

Keywords: high step-down voltage gain; converter; leakage energy; synchronous rectification

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1. Introduction

High step-down converters and high efficiency energy transformation are increasingly required in many industrial applications such as UPSs, LEDs, voltage regulator for MCUs, battery chargers, EVs and power supply for railways. A buck converter and a modified push−pull converter are merged in a novel conversion topology with galvanic isolation; thus, a high step-down ratio is easily achieved without extremely low duty cycle or high turns ratio of the transformer in [1]. Based on the capacitive voltage division, the main objectives of the converter are storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses. As a result, the converter topology possesses the low switch voltage stress and chooses lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved in [2]. An integrated conventional buck–boost converter with a coupled inductor is proposed. The coupled inductor operates not only as a filter inductor of the buck–boost, but also as a transformer [3]. In [4], for the high step-down multiple output and high conversion ratio, isolated bidirectional distributed energy storage systems in [5] are proposed. A new single-switch (without considering SR switch) coupled inductor high step-down converter with an extended duty cycle and non-pulsating output current is presented in [6]. In order to recover the leakage energy, a simple lossless clamp circuit is also proposed. A non-isolated ultra-high step-down interleaved converter with low voltage stress and common ground between the input and output ports is proposed in [7]. High step-down converters and a new topology ISC-TaB and LLC converter are discussed [8,9]. A single-stage step-down ac–dc universal input voltage application is proposed in [10]. A high step-up/down resonant converter at MHz switching frequency, as well as the circuit design techniques to reduce the parasitic effects are discussed in [11]. High efficiency under both full-load and light-load conditions [12] and auto-balanced hybrid LLC series resonant converters with flying capacitors have been proposed in [13]. A bidirectional dc–dc converter with a coupled inductor is proposed in [14,15], which is suitable for applications requiring a large step-down ratio topology. A high-efficiency SIMO step-down converter was applied well to a single input power source plus two output terminals in [16]. An isolated bidirectional dc–dc converter with low current ripples was discussed in [17]. An isolated double step-down dc–dc converter was proposed in [18]. At present, most of the high step-down converters studied in the literature are 400 V/48 V, and 380 V/5 V converters are rarely studied. The buck converter with coupled winding, showing excellent ZVS operation, was proposed in [19]. In this paper, the proposed topology can lower the voltage on the transformer and thus the turns ratio can be reduced. As shown in Figure 1, the proposed high step-down converter can be used for power supply in renewable energy conversion and high DC conversion systems applications. DC Bus can be regarded as the battery of electric vehicles. In this situation, more converts are needed to lower the DC voltage from high DC voltage for load use. The main consideration of this research is the demand for possible future development, so the commonly used 5V output voltage specification is preliminarily determined. It can be speculated that the power supply system used in green energy applications in the future must rely on high-voltage buck converters to provide stable low-voltage power supplies.

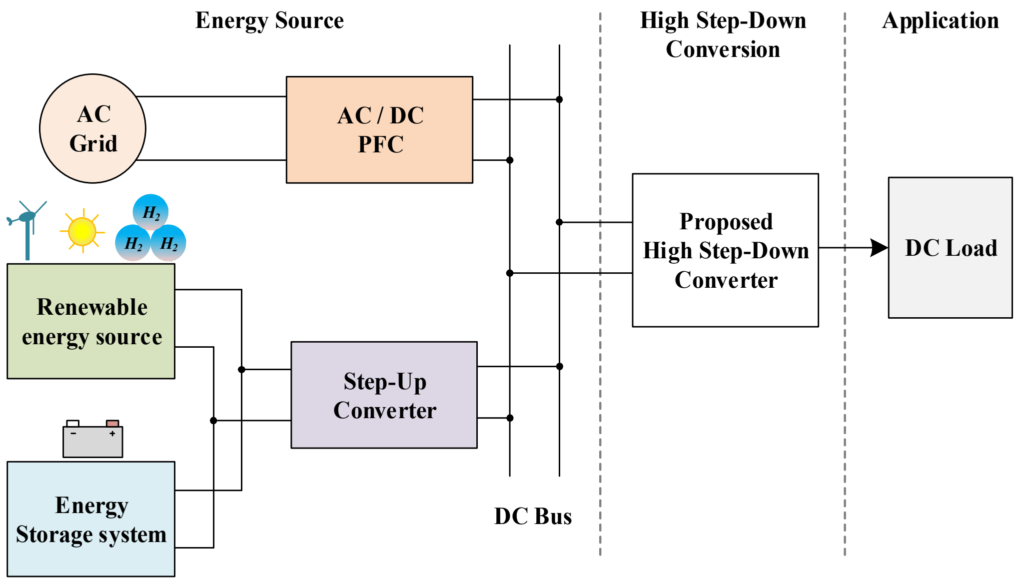

Figure 1. Block diagram of proposed high step-down converter applications.

In order to achieve a very high step-down ratio in the design of the buck converter, the conduction period is extremely low, so the conversion efficiency cannot be improved. Isolated buck conversion topologies are designed to achieve very high step-down voltage gain; the higher transformer turns ratio results in poor coupling, increased leakage inductance and reduced conversion efficiency. Considering that the isolated high step-down conversion ratio design uses an integrated Buck+AHB cascade topology, in order to achieve high conversion efficiency, the power switch switching must achieve the effect of single-stage power flow. Thus, we propose an isolated high step-down converter. The optimized design of single-stage signal-driven power switches in buck and half-bridge cascading topologies enables synchronous power flow from the input stage to the output stage within one switching period, allowing efficient energy conversion.

2. Integrated Buck and Asymmetrical Half-Bridge (IBAHB) Converter

The integrated buck and asymmetrical half-bridge (IBAHB) converter is shown in Figure 2. There are two elements, C_1 and C_{pT}, for reducing the energy of the leakage inductance, which enables the suppression of the peak voltage on the power switches, thus allowing power switches with lower $R_{DS(on)}$ to be utilized; consequently, the reduced voltage stress improves its efficiency. A buck-type circuit is added to the primary side, which makes the voltage on the transformer unequal to V_i Therefore, the turns ratio of the transformer can be reduced to increase the coupling rate, which decreases the leakage inductance. The proposed topology uses four signals that are created by a pair of push–pull signals and a pair of complementary signals to control the power switches. The half-bridge ones are used for the main switches, and the complementary ones are used for synchronous rectification. The secondary side employs a dual-winding center-tapped rectifier circuit to double the frequency of the output inductor current, which can reduce the output current ripple. Therefore, the output inductor and the output capacitor can both be designed with a smaller volume.

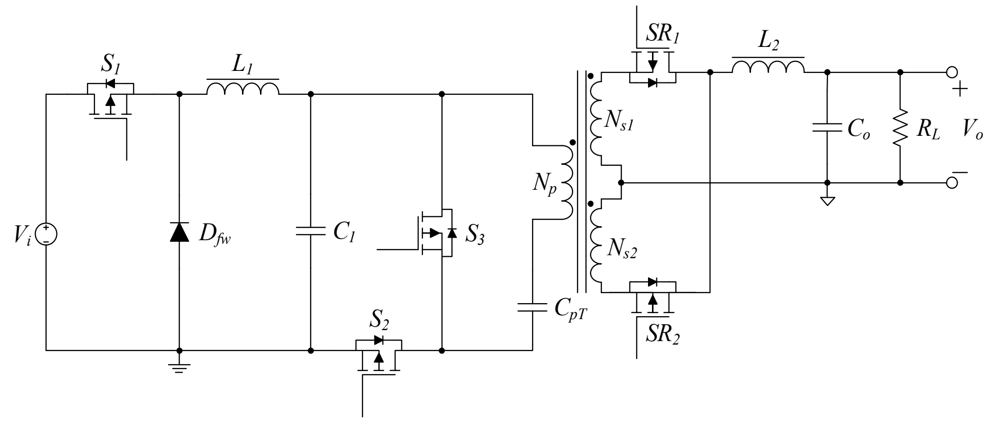

Figure 2. The topology of the proposed converter.

2.1. Operating Principles

The equivalent circuit of the IBAHB is shown in Figure 3. The L_1 and L_2 represent the energy-storing inductor and the output inductor, respectively. Switches S_1, S_2, and S_3 are the main switches of this topology, and switches SR_1 and SR_2 are the synchronous rectifiers.

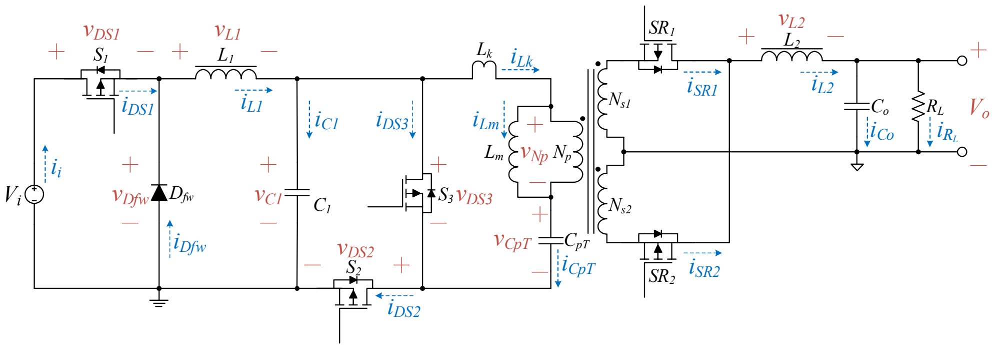

Figure 3. Equivalent circuit of the proposed IBAHB.

Diode D_{fw} is a flywheel diode, C_1 and C_{DS} are the switching capacitors, and C_O is the filter capacitor. The primary side of the transformer is defined as N_p, and the secondary side is defined as N_{s1} and N_{s2}. The turns ratio is defined as n (n = N_{s1}/N_p = N_{s2}/N_p). The transient-state waveforms in CCM are shown in Figure 4. There are eight transient states, which are depicted as follows.

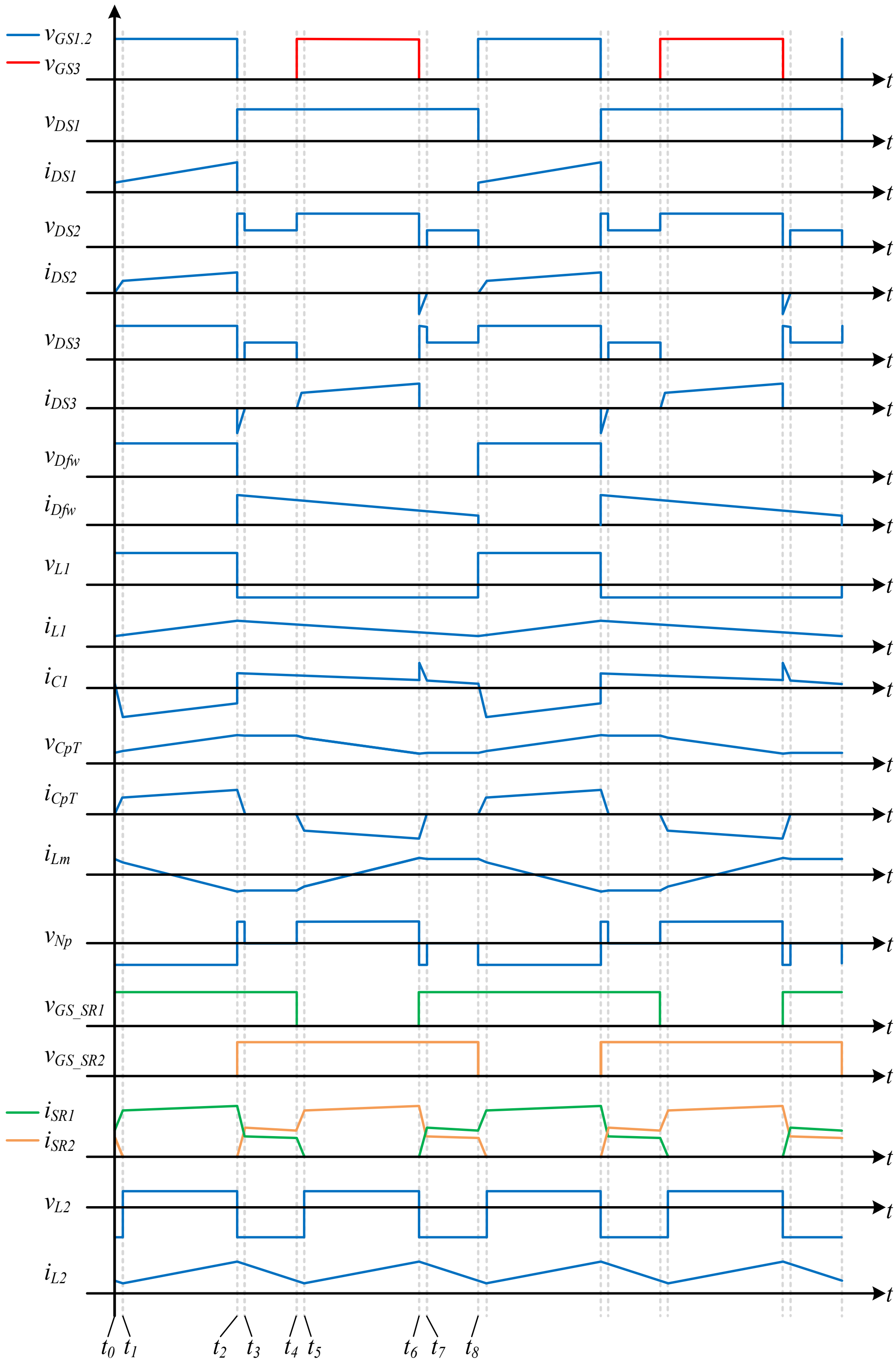

Figure 4. Transient-state waveforms of the proposed IBAHB in CCM.

Mode 1 [t_0~t_1]

In Figure 5a, in this interval, the main switches S_1 and S_2 and the synchronous rectifier SR_1 are in the turned-on state. Voltage source V_i transfers the energy to the inductor L_1 and capacitor C_{pT} through the main switch S_2. At the same time, capacitor C_1 discharges the energy stored by the previous cycle to C_{pT} also through S_2. The transformer starts to send energy from the primary side to the secondary side. The current of the output inductor L_2 maintains its freewheeling state while passing through SR_1 and the body diode of SR_2. However, the current passing through SR_2 decreases, and the current of SR_1 increases. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode1)} = i_{L1}(t_0) + \frac{V_i - V_{C_1}}{L_1} \times (t_1 - t_0) \tag{1}$$

$$i_{N_p(Mode1)} = \frac{N_{s1}}{N_p} \times \left[i_{SR1(Mode1)} - i_{SR2(Mode1)} \right] \tag{2}$$

$$i_{L_m(Mode1)} = \left[i_{L1(Mode1)} + i_{C1(Mode1)} \right] - i_{N_p(Mode1)} \tag{3}$$

$$i_{L2(Mode1)} = i_{SR1(Mode1)} + i_{SR2(\mathrm{Mode1})} \tag{4}$$

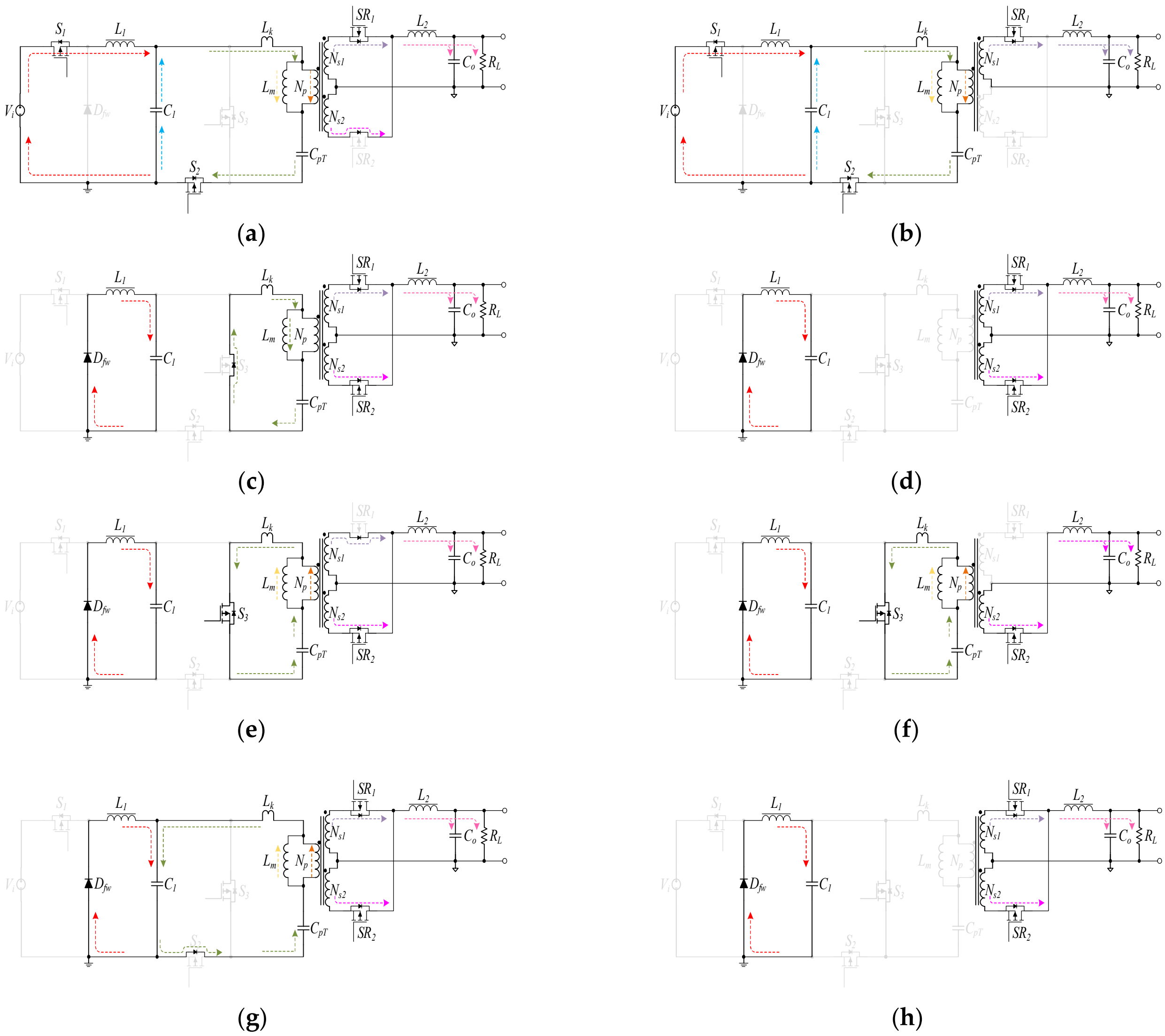

Figure 5. The proposed IBAHB operating modes: (**a**) Mode 1 [t_0, t_1], (**b**) Mode 2 [t_1, t_2], (**c**) Mode 3 [t_2, t_3], (**d**) Mode 4 [t_3, t_4], (**e**) Mode 5 [t_4, t_5], (**f**) Mode 6 [t_5, t_6], (**g**) Mode 7 [t_6, t_7] and (**h**) Mode 8 [t_7, t_8].

Mode 2 [t_1~t_2]

In Figure 5b, in this interval, the main switches S_1 and S_2 and one of the synchronous rectifier switches, SR_1, remain in the turned-on state. The voltage source V_i continues transferring the energy to the energy-storage inductor L_1 and capacitor C_{pT}, and the capacitor C_1 is still discharging to C_{pT}. The transformer continues transferring the energy to the secondary side, and output inductor L_2 and output capacitor C_O are storing the energy provided by the transformer. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode2)} = i_{L1(Mode2)} + \frac{V_i - V_{C1}}{L_1} \times (t_2 - t_1) \tag{5}$$

$$i_{N_p(Mode2)} = \frac{N_{s1}}{N_p} \times i_{SR1(Mode2)} \tag{6}$$

$$i_{L_m(Mode2)} = \left[i_{L1(Mode2)} + i_{C1(Mode2)}\right] - i_{N_p(Mode2)} \tag{7}$$

$$i_{L2(Mode2)} = i_{L2(Mode2)} + \frac{\frac{N_{s1}}{N_p} \times \left(V_{C1} - V_{CpT}\right) - V_o}{L_2} \times t_2 \tag{8}$$

Mode 3 [t_2~t_3]

In Figure 5c, in this interval, the main switches S_1, S_2, and S_3 are in the turned-off state, while the switches of the synchronous rectifier, SR_1 and SR_2, are in the turned-on state. The parasitic body diode of switch S_3 turns ON due to the freewheeling characteristic of leakage inductance. Additionally, the energy of leakage inductance can be retrieved by capacitor C_{pT}. Inductor L_1 releases energy through D_{fw} to capacitor C_1 by its freewheeling state; moreover, the output inductor L_2 starts releasing the energy passing through SR_1 and SR_2 to provide the load R_L. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode3)} = i_{Dfw(Mode3)} \tag{9}$$

$$i_{N_p(Mode3)} = \frac{N_{s1}}{N_p} \times \left[i_{SR1(Mode3)} - i_{SR2(Mode3)}\right] \tag{10}$$

$$i_{L_m(Mode3)} = i_{Lk(Mode3)} \tag{11}$$

$$i_{L2(Mode3)} = i_{SR1(Mode3)} + i_{SR2(Mode3)} \tag{12}$$

Mode 4 [t_3~t_4]

In Figure 5d, in this interval, the main switches S_1, S_2, and S_3 remain in the turned-off state. Inductor L_1 continues releasing energy to C_1 through D_{fw}. Output inductor L_2 also keeps releasing energy to R_L, through SR_1 and SR_2. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode4)} = i_{Dfw(Mode4)} \tag{13}$$

$$i_{N_p(Mode4)} = i_{L_m(Mode4)} = 0 \tag{14}$$

$$i_{L2(Mode4)} = i_{SR1(Mode4)} + i_{SR2(Mode4)} \tag{15}$$

Mode 5 [t_4~t_5]

In Figure 5e, in this interval, the main switch S_3 and one of the synchronous rectifiers SR_2 are in the turned-on state; the other switches are turned off. The inductor L_1 keeps releasing energy to the capacitor C_1. When S_3 turns on, the capacitor C_{pT} starts to release the stored energy, which can transfer to N_{s2} on the secondary side. Because the C_{pT} releases energy, the current passing through SR_1 can decrease to zero, and the current passing through SR_2 can increase. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode5)} = i_{Dfw(Mode5)} \tag{16}$$

$$i_{N_p(Mode5)} = \frac{N_{s2}}{N_p} \times \left[i_{SR1(\mathrm{Mode5})} - i_{SR2(\mathrm{Mode5})} \right] \tag{17}$$

$$i_{L_m(Mode5)} = i_{L_k(Mode5)} - i_{N_p(Mode5)} \tag{18}$$

$$i_{L2(Mode5)} = i_{SR1(Mode5)} + i_{SR2(Mode5)} \tag{19}$$

Mode 6 [t_5~t_6]

In Figure 5f, in this interval, switch S_3 and the switch of the synchronous rectifier SR_2 remain in the turned-on state; the other switches are turned off. This mode is similar to mode 5. However, the current is no longer passing through switch SR_1. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode6)} = i_{Dfw(Mode6)} \tag{20}$$

$$i_{N_p(Mode6)} = (-\frac{N_{s2}}{N_p}) \times i_{SR2(Mode6)} \tag{21}$$

$$i_{L_m(Mode6)} = i_{L_k(Mode6)} - i_{N_p(Mode6)} \tag{22}$$

$$i_{L2(Mode6)} = i_{L2(Mode6)} + \frac{\frac{N_{s2}}{N_p} \times V_{C_{pT}} - V_o}{L_2} \times t_6 \tag{23}$$

Mode 7 [t_6~t_7]

In Figure 5g, in this interval, the main switches S_1, S_2, and S_3 are in the turned-off state, while the switches of the synchronous rectifier SR_1 and SR_2 are in the turned-on state. The switching capacitor C_1 can recover the leakage inductor energy. In this interval, the load energy is absorbed by the output inductor. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode7)} = i_{Dfw(Mode7)} = i_{C1(Mode7)} - i_{L_k(Mode7)} \tag{24}$$

$$i_{N_p(Mode7)} = \frac{N_{s2}}{N_p} \times \left[i_{SR1(Mode7)} - i_{SR2(Mode7)} \right] \tag{25}$$

$$i_{L_m(Mode7)} = i_{L_k(Mode7)} - i_{N_p(Mode7)} \tag{26}$$

$$i_{L2(Mode7)} = i_{SR1(Mode7)} + i_{SR2(Mode7)} \tag{27}$$

Mode 8 [t_7~t_8]

In Figure 5h, in this interval, the main switches S_1, S_2, and S_3 are in the turned-off state and the switches of the synchronous rectifier SR_1 and SR_2 are in the turned-on state. Same as Mode 4, inductors L_1 and L_O release the energy to the switching capacitor C_1 and the load, respectively. The inductor currents i_{L1}, i_{Np}, i_{Lm} and i_{L2} are given, respectively, by

$$i_{L1(Mode8)} = i_{Dfw(Mode8)} \tag{28}$$

$$i_{N_p(Mode8)} = i_{L_m(Mode8)} = 0 \tag{29}$$

$$i_{L2(Mode8)} = i_{SR1(Mode8)} + i_{SR2(Mode8)} \tag{30}$$

2.2. Steady-State Analysis

In order to simplify the analysis, the proposed architecture is presumed to operate in continuous conduction mode (CCM), the method of control is shown in Figure 6. The characteristics of the transient state over the circuit will be ignored, and the currents passing through all of the components will be considered in DC. In addition, there are some assumptions listed as follows:

(1) All components possess ideal characteristics.
(2) The coupling coefficient of the transformer is unity.
(3) The duty cycle is low, under 50%.

(4) The subscript "pft" denotes the average current in the corresponding mode.

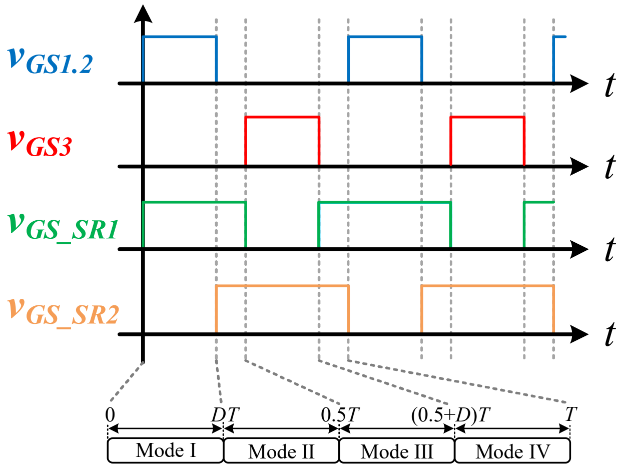

Figure 6. The switching sequence of the proposed topology.

Mode 1 [0, *DT*]

The main switches S_1 and S_2 are in the turned-on state. The input voltage source transfers energy to the inductor L_1 and capacitor C_{pT}. At the same time, the capacitor C_1 also provides energy to C_{pT} through S_2. On the secondary side, the output inductor L_2 and the output capacitor C_o are charging from the transformer and the C_o supplies energy to load R_L. The equivalent circuit is shown in Figure 7 and the formulas can be expresses as:

$$V_{L1(Mode1)} = V_i - V_{Lm} - V_{CpT} = V_i - V_{C1} \tag{31}$$

$$V_{L2(Mode1)} = V_{Ns1} - V_o = n \cdot (V_{C1} - V_{CpT}) - V_o \tag{32}$$

$$I_{C1(Mode1)} = I_{L1} - I_{CpT} = I_i - n \cdot I_{SR1} + I_{Lm} \tag{33}$$

$$I_{CpT(Mode1)} = n \cdot I_{SR1} + I_{Lm} \tag{34}$$

$$I_{Co} = I_{SR1} - I_{R_L} \tag{35}$$

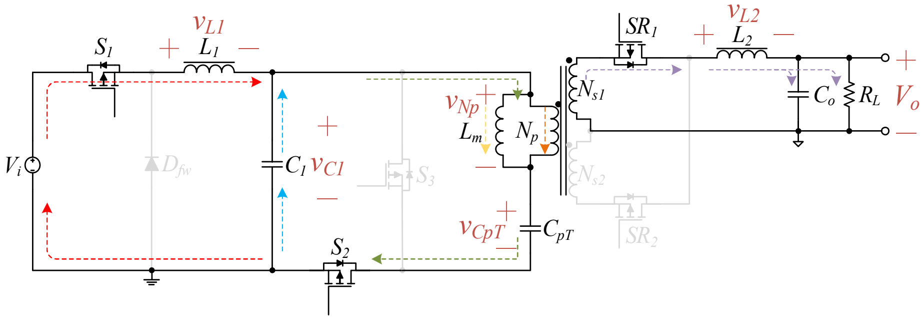

Figure 7. The switches S_1, S_2 and SR_1 are in the turned-on state.

Mode 2 [*DT*, 0.5*T*]

The main switches S_1, S_2 and S_3 are in the turned-off state. Inductor L_1 changes into the freewheeling state to release energy to the capacitor C_1. Output inductor L_o also turns into the freewheeling state to release energy to the capacitor C_o and load R_L. The equivalent circuit is shown in Figure 8 and the formulas can be expressed as:

$$V_{L1(Mode2)} = -V_{C1} \tag{36}$$

$$V_{L2(Mode2)} = -V_o \tag{37}$$

$$I_{C1(Mode2)} = I_{L1} \tag{38}$$

$$I_{CpT(Mode2)} = 0 \tag{39}$$

$$I_{Co(Mode2)} = I_{SR1} + I_{SR2} - I_{R_L} \tag{40}$$

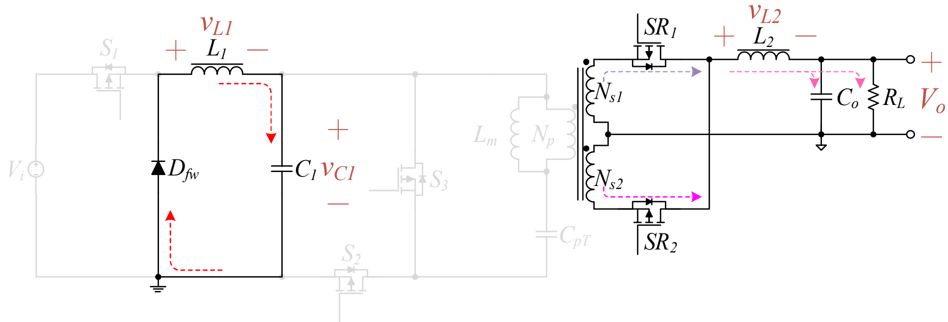

Figure 8. The switches S_1, S_2 and S_3 are in the turned-off state.

Mode 3 [0.5*T*, (0.5+*D*)*T*]

The main switch S_3 is in the turned-on state. Capacitor C_{pT} starts to release energy through the transformer to the secondary side. Inductor L_1 still keeps releasing energy to the capacitor C_1. The output inductor L_2 and the output capacitor C_o are charging using the transformer, and the C_o supplies energy to load R_L. The equivalent circuit is shown in Figure 9 and the formulas can be expressed as:

$$V_{L1(Mode3)} = -V_{C1} \tag{41}$$

$$V_{L2(Mode3)} = V_{Ns2} - V_o = n \cdot V_{CpT} - V_o \tag{42}$$

$$I_{C1(Mdoe3)} = I_{L1} \tag{43}$$

$$I_{CpT(Mode3)} = n \cdot I_{SR2} + I_{Lm} \tag{44}$$

$$I_{Co(Mode3)} = I_{SR2} - I_{R_L} \tag{45}$$

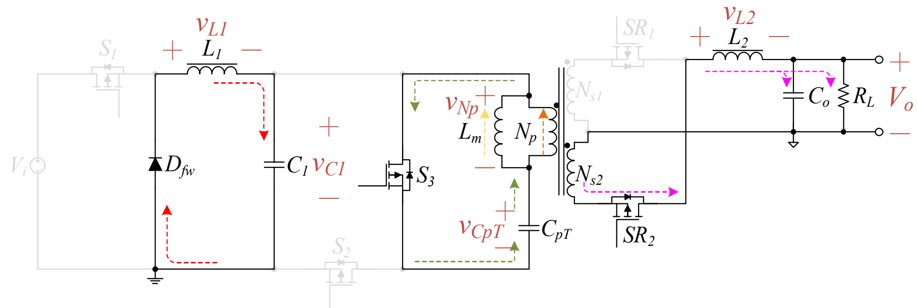

Figure 9. The switches S_3 and SR_2 are in the turned-on state.

Mode 4 [(0.5+*D*)*T*, *T*]

Mode 4 is similar to Mode 2. The main switches S_1, S_2 and S_3 are in the turned-off state. Inductor L_1 still keeps the freewheeling state to release energy to the capacitor C_1. Output inductor L_o turns into the freewheeling state to release energy to the capacitor C_o and load R_L. The equivalent circuit is shown in Figure 10 and the formulas can be expressed as:

$$V_{L1(Mode4)} = -V_{C1} \tag{46}$$

$$V_{L2(Mode4)} = -V_o \tag{47}$$

$$I_{C1(Mode4)} = I_{L1} \tag{48}$$

$$I_{CpT(Mode4)} = 0 \tag{49}$$

$$I_{Co(Mode4)} = I_{SR1} + I_{SR2} - I_{R_L} \tag{50}$$

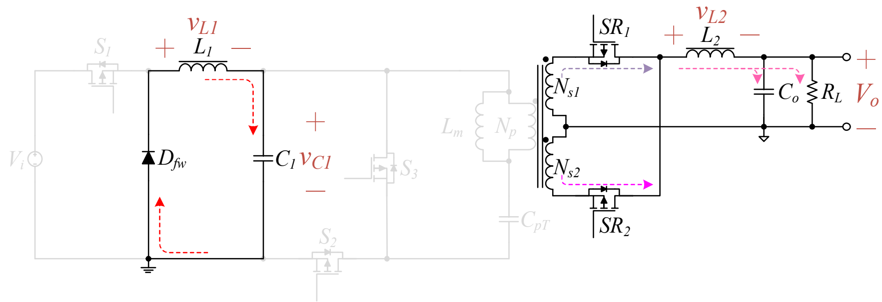

Figure 10. The switches SR_1 and SR_2 are in the turned-on state.

2.3. Voltage Gain

All the voltages of the capacitors can be derived using the charge balance. The relative equations of the energy-storage inductors L_1 and L_2 are given as

$$\int_0^{DT} v_{L1(Mode1)}dt + \int_{DT}^{0.5T} v_{L1(Mode2)}dt + \int_{0.5T}^{(0.5+D)T} v_{L1(Mode3)}dt + \int_{(0.5+D)T}^{T} v_{L1(Mode4)}dt = 0 \tag{51}$$

Substituting (31), (36), (41) and (46) into (51), the voltage of the capacitor C_1 can be given by

$$v_{C1} = D \cdot V_i \tag{52}$$

Because the proposed circuit is an asymmetric architecture, the volt-second balance equation of the output inductor L_2 will be divided into two parts of derivations:

$$\int_0^{DT} v_{L2(Mode1)}dt + \int_{DT}^{0.5T} v_{L2(Mode2)}dt = 0 \tag{53}$$

$$\int_{0.5T}^{(0.5+D)T} v_{L2(Mode3)}dt + \int_{(0.5+D)T}^{T} v_{L2(Mode4)}dt = 0 \tag{54}$$

Substituting Equations (32) and (37) into (53) will give

$$v_o = 2nD \cdot (v_{C1} - v_{CpT}) \tag{55}$$

Substituting Equations (42) and (47) into (54) will give

$$v_o = 2nD \cdot v_{CpT} \tag{56}$$

Equations (55) and (56) will be equal, and substitute (52). The voltage of the capacitor C_{pT} can be obtained by

$$v_{CpT} = \frac{1}{2} D \cdot V_i \tag{57}$$

Finally, use Equations (56) and (57) to obtain the ideal voltage gain of the proposed architecture. The ideal voltage gain curve is shown in Figure 11:

$$\frac{v_o}{V_i} = n \cdot D^2 \tag{58}$$

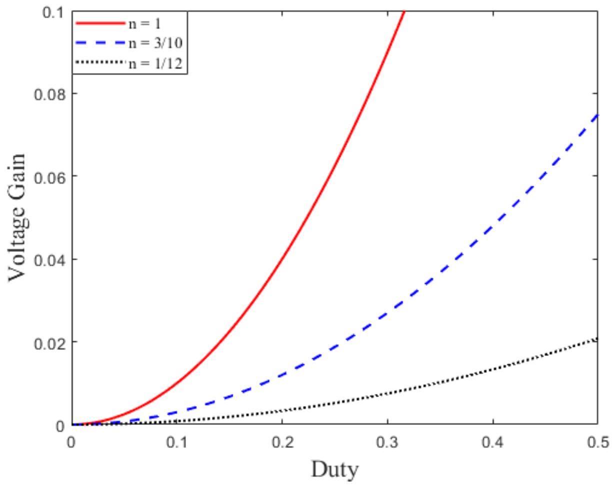

Figure 11. Ideal voltage gain of the proposed topology.

2.4. Voltage Stress

The voltage stresses of semiconductor devices can be derived by the known voltage of all the capacitors. Therefore, when the main switches S_1 and S_2 are in the turned-on state, the voltage stress of switch S_3 will be equal to the voltage of the capacitor C_1, as shown in Figure 7.

$$v_{DS3} = v_{C1} = D \cdot V_i \tag{59}$$

The voltage stress of the freewheeling diode D_{fw} can be given by

$$v_{Dfw} = V_i \tag{60}$$

Additionally, the voltage stress of the synchronous rectifier switch SR_2 will be equal to the sum of V_{Ns1} and V_{Ns2}, which is also equal to V_{C1} minus V_{CpT} and then multiplied two times by the turns ratio 2n.

$$v_{SR2} = v_{Ns1} + v_{Ns2} = 2n \cdot (v_{C1} - v_{CpT}) = nD \cdot V_i \tag{61}$$

when the switch S_3 is turned on, switches S_1 and S_2 are turned off. As shown in Figure 9, the voltage stress of the S_1 is equal to the sum of the input voltage V_i and the capacitor C_1. The voltage stress of S_2 is equal to the capacitor C_1 and the voltage stress can be given by

$$v_{DS1} = V_i + V_{C1} \tag{62}$$

$$v_{DS2} = v_{C1} = D \cdot V_i \tag{63}$$

Because the secondary winding structure is symmetrical, the voltage stress of the synchronous rectifier SR_1 is the same as SR_2. The voltage stress can be given by

$$v_{SR1} = v_{Ns1} + v_{Ns2} = 2n \cdot (v_{C1} - v_{CpT}) = nD \cdot V_i \tag{64}$$

when the input voltage and the turns ratio n equal 380V and $\frac{1}{12}$, respectively, the relationship between the voltage stress and the duty cycle is shown in Figure 12. It can be seen from Equations (53) and (57) that S_2 and S_3 have relatively lower voltage stress. Hence, low-voltage-stress power devices, such as MOSFETs with low $R_{DS(on)}$, can be employed. Similar to switches S_2 and S_3, SR_1 and SR_2 can also adapt low-voltage-stress power devices with low $R_{DS(on)}$ to reduce the loss of semiconductors to improve efficiency.

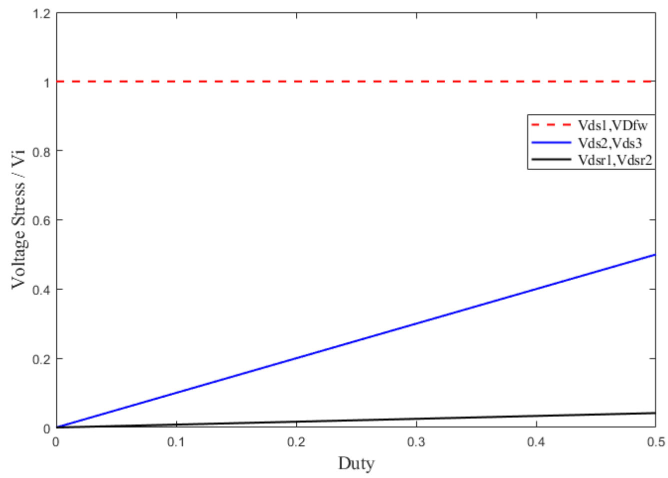

Figure 12. The estimated voltage stresses of switches.

2.5. Current Stresses

Due to the law of conservation of energy, the output current I_{Ro} is equal to the input current I_i divided by the voltage gain, which can be expressed as

$$i_{R_L} = \frac{i_i}{n \cdot D^2} \tag{65}$$

The main switches S_1 and S_2 are in the turned-on state and S_3 is in the turned-off state, which is shown in Figure 7. The current through S_1 and S_2 can be expressed as

$$i_{DS1(ptf)} = i_{i(ptf)} = i_{L1(ptf)} = \frac{i_{i(avg)}}{D} = nD \cdot i_{R_L(avg)} \tag{66}$$

$$i_{DS2(ptf)} = n \cdot i_{SR1(ptf)} \tag{67}$$

$$i_{SR1(ptf)} = i_{R_L(avg)} \tag{68}$$

The main switches S_1, S_2 and S_3 are in the turned-off state, as shown in Figure 8. During this period, the current stresses through other semiconductor devices can be expressed as

$$i_{Dfw(ptf)} = i_{L1(ptf)} = nD \cdot i_{R_L(avg)} \tag{69}$$

$$i_{SR1(ptf)} = i_{SR2(ptf)} = \frac{i_{R_L(avg)}}{2} \tag{70}$$

As shown in Figure 9, the switch S_3 turns into the ON state, while the main switches S_1 and S_2 remain turned off. The current through the semiconductor devices can be expressed as

$$i_{Dfw(ptf)} = i_{L1(ptf)} = nD \cdot i_{R_L(avg)} \tag{71}$$

$$i_{DS3(ptf)} = n \cdot i_{SR2(ptf)} = n \cdot i_{R_L(avg)} \tag{72}$$

$$i_{SR2(ptf)} = i_{R_L(avg)} \tag{73}$$

when the main switches S_1, S_2 and S_3 are in the turned-off state again, the current flowing through the semiconductor devices would be the same as the previous operation mode.

The highest current flowing through each semiconductor element is the criterion for selecting current stress. The current stress of all the semiconductor devices would be reorganized and expressed below

$$i_{DS1(stress)} = nD \cdot i_{R_L(peak)} \tag{74}$$

$$i_{Dfw(stress)} = nD \cdot i_{R_L(peak)} \tag{75}$$

$$i_{DS2(stress)} = n \cdot i_{R_L(peak)} \tag{76}$$

$$i_{DS3(stress)} = n \cdot i_{R_L(peak)} \tag{77}$$

$$i_{SR1(stress)} = i_{R_L(peak)} \tag{78}$$

$$i_{SR2(stress)} = i_{R_L(peak)} \tag{79}$$

When the output current and the turns ratio n equal 40A and $\frac{1}{12}$, respectively, the relationship between the average current stress and the duty cycle is shown in Figure 13.

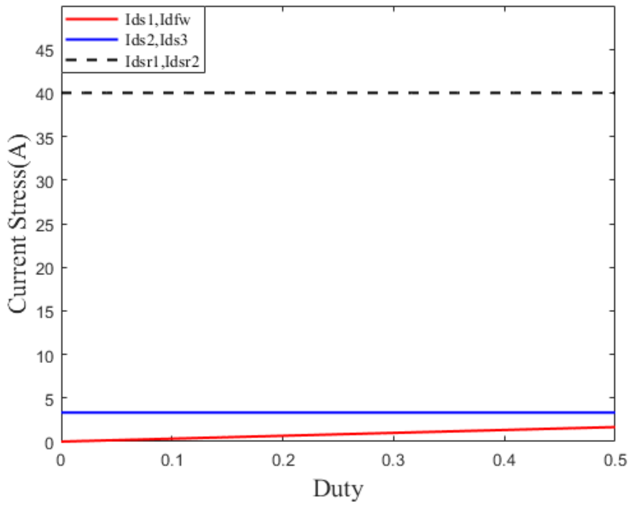

Figure 13. The estimated current stresses of switches and diode.

2.6. Conduction Loss Analysis

The equivalent circuit for analyzing the conduction loss of inductors and semiconductor devices is shown in Figure 14, in which r_{L1} and r_{L2} are the copper resistance of the inductors, r_{Dfw} and V_{Dfw} are the on-resistance and the forward voltage of the diode, respectively, r_{DS_S1}, r_{DS_S2}, r_{DS_S3}, r_{DS_SR1} and r_{DS_SR2} are the on-resistances of the switches.

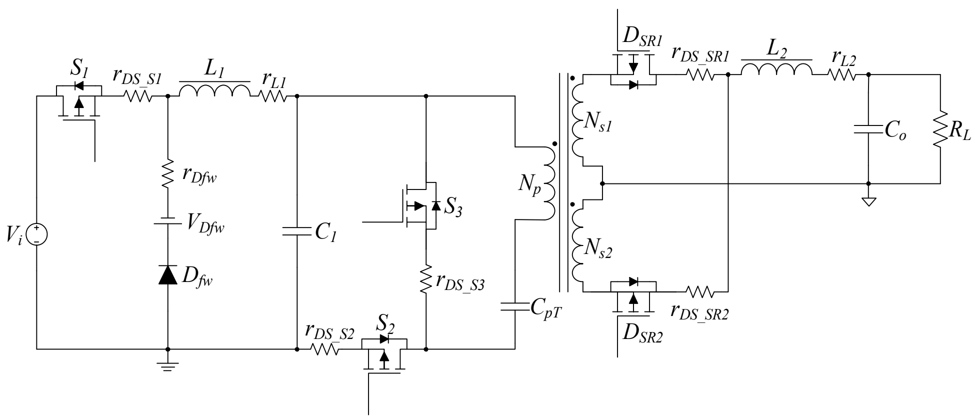

Figure 14. Equivalent circuit with parasitic components of the proposed topology.

Mode 1 [0, *DT*]

The main switches S_1 and S_2 are in turned-on state. The voltage source V_i transfers energy to the inductors L_1 and the capacitor C_{pT} receives energy from V_i and the capacitor C_1.

Simultaneously, the output inductor L_2 and capacitor C_o are charging through the transformer, and then C_o supplies energy to the load R_L. The equivalent circuit is shown in Figure 15 and the formulas are expressed as follows:

$$\begin{aligned} v_{L1(Mode1)} &= V_i - v_{C1} - i_{L1} \cdot (r_{DS\_S1} + r_{L1}) \\ &= V_i - [v_{CpT} + v_{Np} + i_{L1} \cdot (r_{DS\_S1} + r_{L1}) + n \cdot i_{L2} \cdot r_{DS\_S2}] \end{aligned} \tag{80}$$

$$v_{L2(Mode1)} = n \cdot (v_{C1} - v_{CpT} - n \cdot i_{L2} \cdot r_{DS\_S2}) - i_{L2} \cdot (r_{SR1} + r_{L2}) - v_o \tag{81}$$

$$v_{Np(Mode1)} = \frac{1}{n} \cdot [v_o + v_{L2} + i_{L2} \cdot (r_{SR1} + r_{L2})] \tag{82}$$

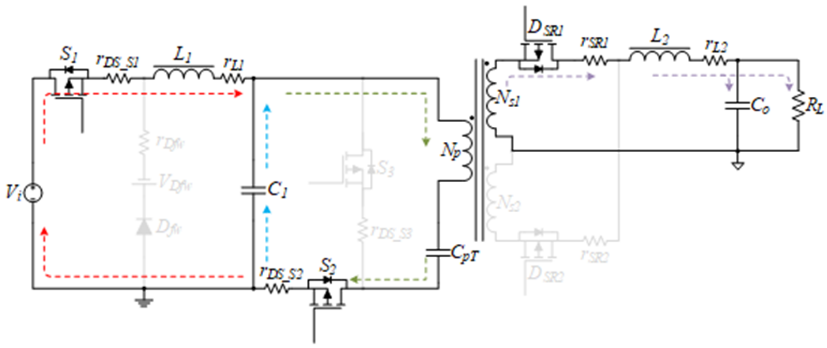

Figure 15. Equivalent circuit operating during [0, *DT*].

Mode 2 [*DT*, 0.5*T*]

The main switches S_1, S_2 and S_3 are in the turned-off state. In this interval, the inductor L_1 releases energy to the capacitor C_1, and the output inductor L_2 changes into the freewheeling state, releasing energy to the output load R_L. The equivalent circuit is shown in Figure 16 and the formulas are expressed as follows:

$$v_{L1(Mode2)} = -[v_{C1} + V_{Dfw} + i_{L1} \cdot (r_{Dfw} + r_{L1})] \tag{83}$$

$$v_{L2(Mode2)} = -(v_o + \frac{i_{L2}}{2} \cdot r_{SR1} + i_{L2} \cdot r_{L2}) \tag{84}$$

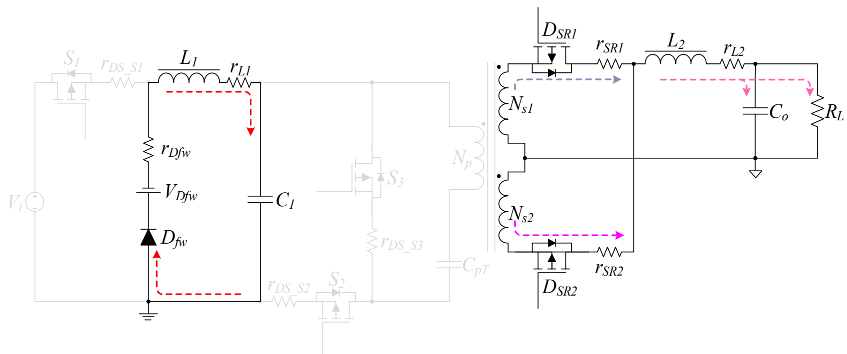

Figure 16. Equivalent circuit operating during [*DT*, 0.5*T*].

Mode 3 [0.5*T*, (0.5+*D*) *T*]

In this interval, the main switch S_3 is in the turned-on state. The inductor L_1 keeps releasing energy to the capacitor C_1, and the capacitor C_{pT} sends the energy to the output inductor L_2 and output capacitor C_o through the transformer. Then, C_o provides energy to the output load R_L. The equivalent circuit is shown in Figure 17 and the formulas are expressed as follows:

$$v_{L1(Mode3)} = -[v_{C1} + V_{Dfw} + i_{L1} \cdot (r_{Dfw} + r_{L1})] \tag{85}$$

$$v_{L2(Mode3)} = n \cdot (v_{CpT} - n \cdot i_{L2} \cdot r_{DS\_S3}) - i_{L2} \cdot (r_{SR2} + r_{L2}) - v_o \tag{86}$$

$$v_{Np(Mode3)} = \left(-\frac{1}{n}\right) \cdot [v_o + v_{L2} + i_{L2}(r_{SR2} + r_{L2})] \tag{87}$$

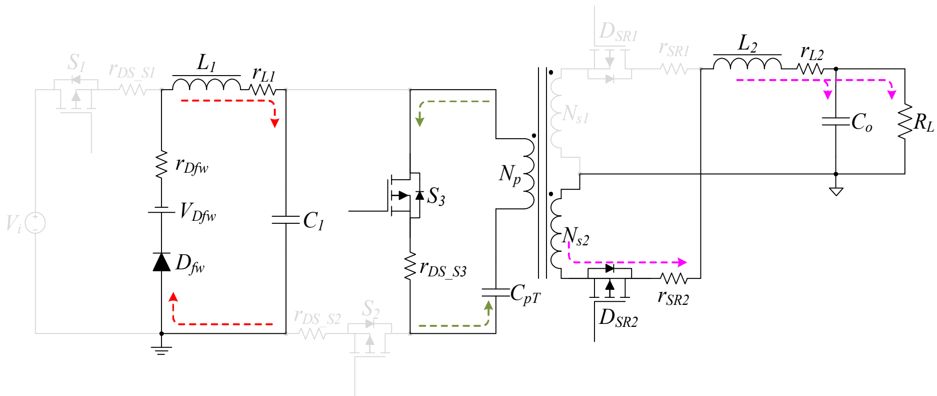

Figure 17. Equivalent circuit operating during [0.5*T*, (0.5 + *D*) *T*].

Mode 4 [(0.5+*D*) *T*, *T*]

Similar to the Mode 2 state, the main switches S_1, S_2 and S_3 are all in the turned-off state. The inductor L_1 keeps releasing energy to the capacitor C_1 and the output inductor L_2 changes into the freewheeling state, releasing energy to the output load R_L. The equivalent circuit is shown in Figure 18 and the formulas are expressed as follows:

$$v_{L1(Mode4)} = -[v_{C1} + V_{Dfw} + i_{L1} \cdot (r_{Dfw} + r_{L1})] \tag{88}$$

$$v_{L2(Mode4)} = -(v_o + \frac{i_{L2}}{2} \cdot r_{SR2} + i_{L2} \cdot r_{L2}) \tag{89}$$

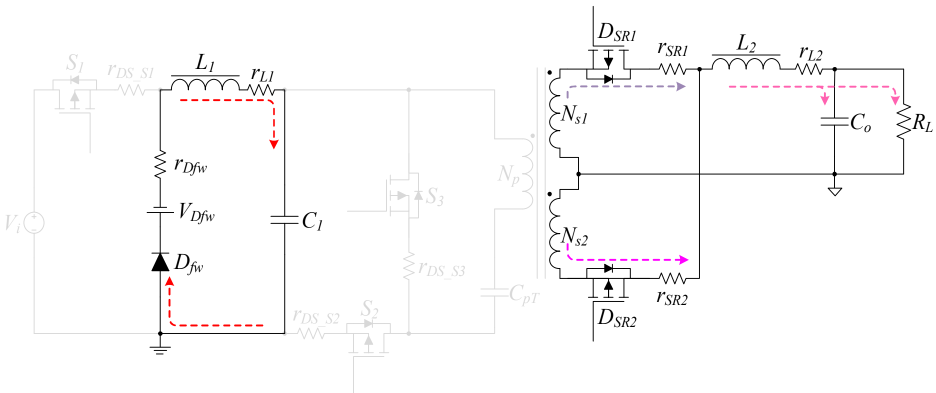

Figure 18. Equivalent circuit operating during [(0.5 + D) *T*, *T*].

First, through volt-second balance, the equation of the inductor L_1 can be expressed as

$$\int_0^{DT} v_{L1(Mode1)}dt + \int_{DT}^{0.5T} v_{L1(Mode2)}dt + \int_{0.5T}^{(0.5+D)T} v_{L1(Mode3)}dt + \int_{(0.5+D)T}^{T} v_{L1(Mode4)}dt = 0 \tag{90}$$

By substituting Equations (80), (83), (85) and (88) into Equation (90), the voltage of the capacitor C_1 which is in the non-ideal state can be derived as

$$v_{C1} = D \cdot V_i - (1 - D) \cdot V_{Dfw} - i_{L1} \cdot \left[D \cdot r_{DS\_S1} + (1 - D) \cdot r_{Dfw} + r_{L1}\right] \tag{91}$$

Second, the proposed circuit is an asymmetric topology, so the volt-second balance equation of the output inductor L_2 should be divided into two parts of derivations:

$$\int_0^{DT} v_{L2(Mode1)}dt + \int_{DT}^{0.5T} v_{L2(Mode2)}dt = 0 \tag{92}$$

$$\int_{0.5T}^{(0.5+D)T} v_{L2(Mode3)}dt + \int_{(0.5+D)T}^{T} v_{L2(Mode4)}dt = 0 \tag{93}$$

Substitute Equations (81) and (84) into (92) and simplify it. Then, replace r_{SR1} with r_{SR}, which is shown below.

$$2nD \cdot (v_{C1} - v_{CpT}) - 2n^2D \cdot i_{L2} \cdot r_{DS\_S2} - i_{L2} \cdot (D \cdot r_{SR} + \frac{1}{2}r_{SR} + r_{L2}) - v_o = 0 \tag{94}$$

Substitute Equations (86) and (89) into (93) and simplify it. Then, replace r_{SR2} with r_{SR}, which is shown below.

$$2nD \cdot v_{CpT} - 2n^2D \cdot i_{L2} \cdot r_{DS\_S3} - i_{L2} \cdot (D \cdot r_{SR} + \frac{1}{2} \cdot r_{SR} + r_{L2}) - v_o = 0 \tag{95}$$

It is known that the summation and subtraction of Equations (94) and (95) are equal to zero, which are expressed as follows, respectively:

$$nD \cdot v_{C1} - n^2D \cdot i_{L2} \cdot (r_{DS\_S2} + r_{DS\_S3}) - i_{L2} \cdot (D \cdot r_{SR} + \frac{1}{2}r_{SR} + r_{L2}) - v_o = 0 \tag{96}$$

$$v_{C1} = 2v_{CpT} \tag{97}$$

Substitute v_{C1} of Equation (97) with Equation (91) and simplify it. Then, into Equation (95), as follows:

$$\begin{aligned} v_o = nD^2 \cdot V_i - nD \cdot (1-D) \cdot V_{Dfw} + n^2D^3 \cdot i_{L2} \cdot (r_{Dfw} - r_{DS_{S1}}) \\ -n^2D^2 \cdot i_{L2} \cdot (r_{Dfw} + r_{L1}) - n^2D \cdot i_{L2} \cdot (r_{DS_{S2}} + r_{DS_{S3}}) \\ -D \cdot i_{L2} \cdot r_{SR} - i_{L2} \cdot (r_{L2} + \tfrac{1}{2}r_{SR}) \end{aligned} \tag{98}$$

Then, transfer Equation (98) into an equivalent circuit module, as shown in Figure 19.

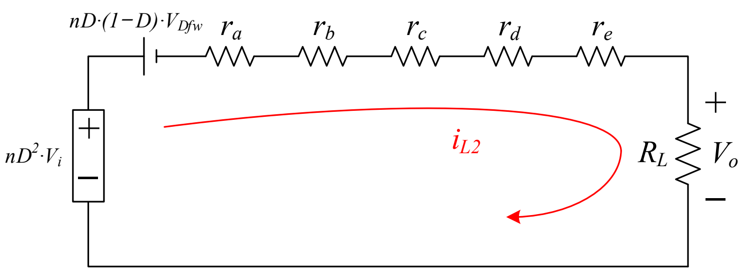

Figure 19. Simple equivalent circuit module using Equation (98).

$$r_a = n^2D^3 \cdot (r_{Dfw} - r_{DS_{S1}}) \tag{99}$$

$$r_b = n^2D^2 \cdot (r_{Dfw} + r_{L1}) \tag{100}$$

$$r_c = n^2D \cdot (r_{DS_{S2}} + r_{DS_{S3}}) \tag{101}$$

$$r_d = D \cdot r_{SR} \tag{102}$$

$$r_e = r_{L2} + \frac{1}{2}r_{SR} \tag{103}$$

Divide Equation (98) by V_i to obtain the voltage gain of the non-ideal state, which is expressed as

$$\frac{v_o}{V_i} = \left[n \cdot D^2 - nD(1-D) \cdot K\right] \times \frac{R_L}{R_L + r_a + r_b + r_c + r_d + r_e} \tag{104}$$

Equation (98) multiplied by $\frac{i_{R_L}}{i_i}$ is the efficiency equation of the non-ideal state, which is expressed as follows:

$$\eta = [1 - (\frac{1-D}{D}) \cdot K] \times \frac{R_L}{R_L + r_a + r_b + r_c + r_d + r_e} \tag{105}$$

where

$$K = \frac{V_{Dfw}}{Vi} \tag{106}$$

$$r_a = n^2 D^3 \cdot (r_{Dfw} - r_{DS_{S1}}) \tag{107}$$

$$r_b = n^2 D^2 \cdot (r_{Dfw} + r_{L1}) \tag{108}$$

$$r_c = n^2 D \cdot \left(r_{DS_{S2}} + r_{DS_{S3}}\right) \tag{109}$$

$$r_d = D \cdot r_{SR} \tag{110}$$

$$r_e = r_{L2} + \frac{1}{2} r_{SR} \tag{111}$$

After calculating, the non-ideal voltage gain and the efficiency curve are shown below, as Figures 20 and 21.

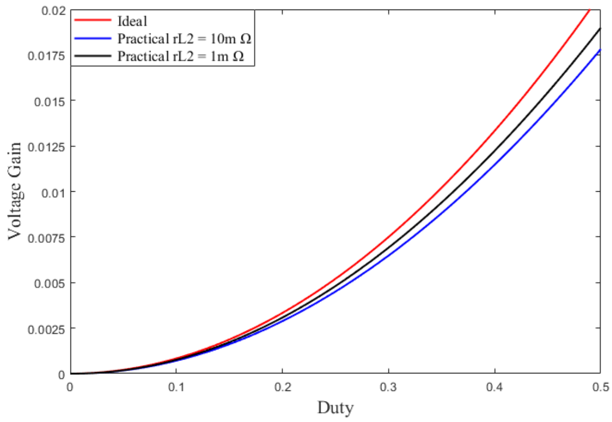

Figure 20. The calculated voltage gain of the proposed topology considering conduction loss.

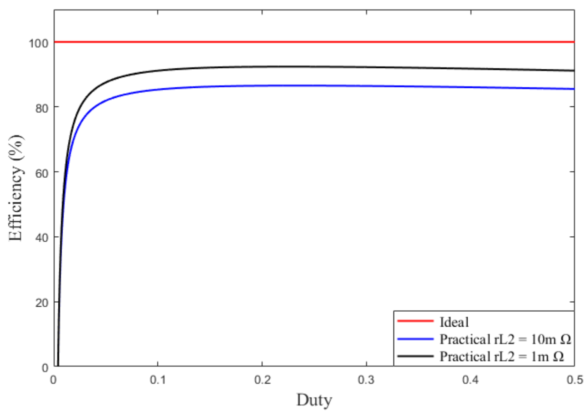

Figure 21. The calculated efficiency of the proposed topology considering conduction loss.

3. Design Considerations

3.1. Inductances

In order to achieve high step-down conversion, the proposed power topology requires components that can store energy and stabilize potential. Thus, this section analyzes and discusses the ripple characteristics of the energy storage elements.

First, the corresponding equation of inductance and current ripple can be expressed as follows:

$$L \cdot \Delta i_L = v_L \cdot \Delta t \tag{112}$$

Substituting Equation (31) into (112) would deduce the relationship between the inductor L_1 and current ripple, which is expressed as follows:

$$L_1 = \frac{v_{L1}}{\Delta i_{L1}} \cdot (1-D) \cdot T = \frac{-v_{C1}}{\Delta i_{L1(-)}} \cdot (1-D) \cdot T \tag{113}$$

The condition of the L_1 working in the boundary conduction mode (BCM) is expressed below:

$$\left|\Delta i_{L1(-)}\right| = 2 \times i_{L1} \tag{114}$$

Obtain the equation of the L_1 working in BCM with (113) and (114), which is shown below:

$$L_{1(BCM)} = \frac{(1-D) \cdot R_L}{2 \cdot (nD)^2 \cdot f} = \frac{(1-D) \cdot {v_o}^2}{2 \cdot (nD)^2 \cdot f \cdot P_o} \tag{115}$$

As shown in Figure 22, the curve shows the value of L_1 working in BCM at each duty cycle with a switching frequency of 50kHz and $\frac{1}{12}$ turns ratio.

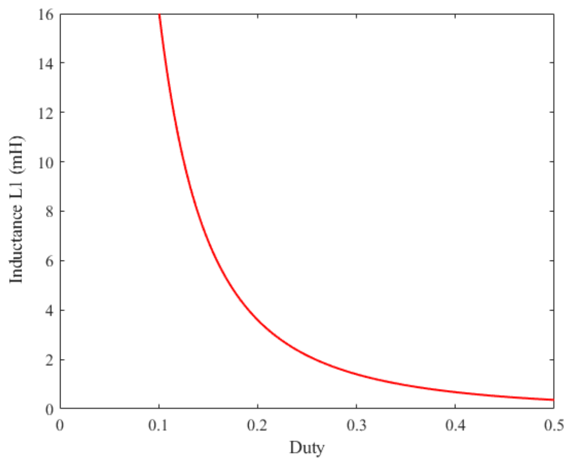

Figure 22. The calculated value of inductance L_1 in the boundary mode.

Next, derivate the equation of the output inductor L_2 in BCM. Substitute Equation (37) into Equation (112), and the relationship between L_2 and its current ripple would be derived as follows:

$$L_2 = \frac{v_{L_2}}{\Delta i_{L2(-)}} \cdot \left(\frac{1}{2} - D\right) \cdot T = \frac{-v_o}{\Delta i_{L2}} \cdot \left(\frac{1}{2} - D\right) \cdot T \tag{116}$$

The condition of L_2 working in BCM is expressed as follows:

$$\left|\Delta i_{L2(-)}\right| = 2 \times i_{L2} \tag{117}$$

Obtain the equation of the L_2 working in BCM with Equations (116) and (117), as follows:

$$L_{2(BCM)} = \frac{\left(\frac{1}{2} - D\right) \cdot {v_o}^2}{2 \cdot f \cdot P_o} \tag{118}$$

As shown in Figure 23, the curve shows the value of inductor L_2 working in BCM at each duty cycle with a switching frequency of 50 kHz and $\frac{1}{12}$ turns ratio.

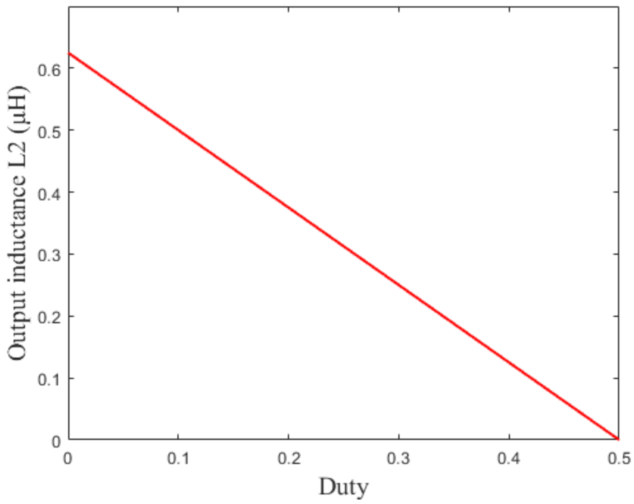

Figure 23. The calculated value of inductance L_2 in the boundary mode.

3.2. Capacitors

The equation of the relationship between all capacitors and voltage ripple in the proposed topology can be expressed as:

$$\Delta Q = C \cdot \Delta v = I \cdot \Delta t \tag{119}$$

According to Equation (119), the relationship between the value of each capacitor and its voltage ripple can be expressed as follows:

$$C_1 = \frac{v_{C_1} \cdot (1 - D)^2}{L_1 \cdot f^2 \cdot \Delta v_{C_1}} = \frac{(1 - D)^2}{L_1 \cdot f^2 \cdot \frac{\Delta v_{C_1}}{v_{C_1}}} \tag{120}$$

$$C_{pT} = \frac{D^2 \cdot \left(n \cdot v_{CpT} - v_o\right)}{L_2 \cdot f^2 \cdot \Delta v_{C_{pT}}} = \frac{nD^2 \cdot (1 - 2D)}{L_2 \cdot f^2 \cdot \frac{\Delta v_{C_{pT}}}{v_{C_{pT}}}} \tag{121}$$

$$C_o = \frac{v_o \cdot \left(\frac{1}{2} - D\right)}{16 \cdot L_2 \cdot f^2 \cdot \Delta v_o} = \frac{\left(\frac{1}{2} - D\right)}{16 \cdot L_2 \cdot f^2 \cdot \frac{\Delta v_o}{v_o}} \tag{122}$$

3.3. Control Block Diagram

As shown in Figure 24, after feedback voltage V_{FB} is calculated and processed, a group of output signals $V_{GS1,2}$ is generated through the comparison result with the sawtooth wave, and then V_{GS3} and the secondary side synchronous rectification control signal V_{GS_SR1} and V_{GS_SR2} are generated through the delay and the reversed signal.

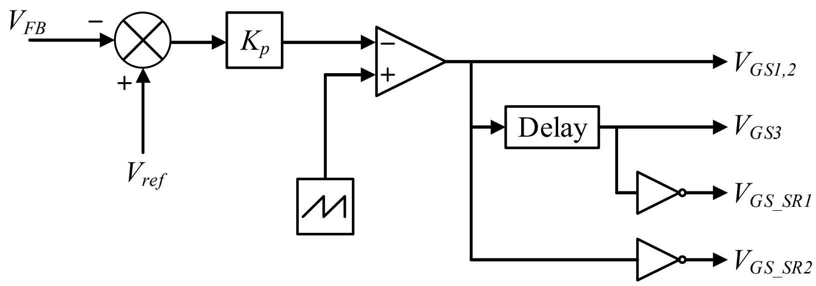

Figure 24. A diagram of the proposed control scheme.

3.4. Design of Storage Elements

The turns ratio of the transformer n is preset to $\frac{1}{12}$, so the duty cycle is almost equal to 0.4 (0.397). The derivation of the duty cycle is shown below.

$$D = \sqrt{\frac{V_o}{V_i} \times \frac{1}{n}} \cong 0.397 \tag{123}$$

The design of the inductance value operating in boundary mode is divided into two parts: the inductor L_1 and the output inductor L_2. Assume the inductor L_1 working in the boundary conduction mode (BCM) is at 20% of full load and use the parameters in Equation (115). The inductance value of L_1 in BCM is shown below:

$$L_{1(BCM)} = \frac{(1-D) \cdot {V_o}^2}{2 \cdot (nD)^2 \cdot f \cdot P_o} \cong 3.443 \text{ mH} \tag{124}$$

In addition, the output inductance L_2 is preset working in BCM at 5% of full load and use the parameters in Equation (118), which is shown below:

$$L_{2(BCM)} = \frac{\left(\frac{1}{2} - D\right) \cdot {v_o}^2}{2 \cdot f \cdot P_o} = 2.575 \ \mu\text{H} \tag{125}$$

Additionally, the number of turns N_p is calculated as follows:

$$N_p = \frac{V_{Np} \cdot dt}{\Delta B \cdot A_e} = \frac{\left(\frac{1}{2} \cdot D \cdot V_i\right) \cdot D}{2 \cdot B_{max} \cdot A_{e(ETD49)} \cdot f} \cong 12 \ Turns \tag{126}$$

At full load, the allowable voltage ripple of the output capacitor C_o would be designed to be less than 0.5%, and the capacitors C_1 and C_{pT} would be designed to be less than 1%. Use the parameters in Equations (120) to (122), and the capacitance value is calculated as follows:

$$C_1 = \frac{v_{C_1} \cdot (1-D)^2}{L_1 \cdot f^2 \cdot \Delta v_{C_1}} = \frac{(1-D)^2}{L_1 \cdot f^2 \cdot \frac{\Delta v_{C_1}}{v_{C_1}}} \cong 16 \ \mu\text{F} \tag{127}$$

$$C_{pT} = \frac{D^2 \cdot (n \cdot v_{C_{pT}} - v_o)}{L_2 \cdot f^2 \cdot \Delta v_{C_{pT}}} = \frac{nD^2 \cdot (1-2D)}{L_2 \cdot f^2 \cdot \frac{\Delta v_{C_{pT}}}{v_{C_{pT}}}} \cong 54 \ \mu\text{F} \tag{128}$$

$$C_o = \frac{v_o \cdot (\frac{1}{2} - D)}{16 \cdot L_2 \cdot f^2 \cdot \Delta v_o} = \frac{(\frac{1}{2} - D)}{16 \cdot L_2 \cdot f^2 \cdot \frac{\Delta v_o}{v_o}} \cong 250 \ \mu\text{F} \tag{129}$$

Using Equations (52) and (57), the voltage generated by the capacitors C_1 and C_{pT} is calculated as follows, respectively.

$$V_{C_1} = D \cdot V_i = 150.86 \text{ V} \tag{130}$$

$$V_{C_{pT}} = \frac{1}{2} \cdot D \cdot V_i = 75.43 \text{ V} \tag{131}$$

At full load, the reverse voltage and forward current of the diode can be calculated by (60) and (69), respectively.

$$V_{D_{fw}} = V_i = 380 \text{ V} \tag{132}$$

$$I_{D_{fw}} = nD \cdot I_{R_L} = 1.323 \text{ A} \tag{133}$$

The voltage stress of the power switches can be calculated using Equations (59) and (61)–(64), and the average current of the ones can be calculated using (74), (76)–(79), which is shown as follows:

$$V_{DS1} = V_i + V_{C1} = V_i + D \cdot V_i = (1 + D) \cdot V_i = 530.86 \text{ V} \tag{134}$$

$$V_{DS2} = V_{DS3} = V_{C1} = D \cdot V_i = 150.86 \text{ V} \tag{135}$$

$$V_{D_{SR1}} = V_{D_{SR2}} = V_{Ns1} + V_{Ns2} = 2n \cdot \left(V_{C1} - V_{CpT}\right) = nD \cdot V_i = 12.57 \text{ V} \tag{136}$$

$$I_{DS1} = nD \cdot I_{R_L} = 1.323 \text{ A} \tag{137}$$

$$I_{DS2} = I_{DS3} = n \cdot I_{R_L} = 3.333 \text{ A} \tag{138}$$

$$I_{SR1} = I_{SR2} = I_{R_L} = 40 \text{ A} \tag{139}$$

4. Experimental Results

The specification and component parameters of the proposed topology are shown in Tables 1 and 2, respectively. Additionally, Figure 25 shows the presented converter and marks the main components. Experimental waveforms for the proposed topology at a full load of 200 W are shown in Figure 26. Figure 26a shows the voltage stress of the main switch S_1 and freewheeling diode D_{fw}, and it can be seen from the waveform that the withstand voltage of the main switch and the flywheel diode D_{fw} is very small. Figure 26b shows the voltage and current stress of S_2, the voltage and current stress of S_2 are reasonable. Figure 26c shows the voltage and current stress of S_3, the voltage stress and current stress of S_3 are reasonable. Figure 26d shows the voltage of C_{pT} and the current through the transformer i_{Lk}, from the i_{Lk} current waveform. It can be seen that the current flowing through the transformer is balanced and symmetrical, and no bias phenomenon occurs. Figure 26e shows the voltage and current stress of SR_1 and SR_2; the voltage and current of the synchronous rectification in the waveform are correct. Figure 26f shows i_{L1} and i_{L2}, respectively, the current of L_2 is twice the switching frequency, effectively reducing the ripple of the output current.

Table 1. Prototype specification of the proposed IBAHB.

Experimental Specifications	
Input Voltage (V_{in})	380 V
Output Voltage (V_o)	5 V
Switching Frequency (f_s)	50 kHz
Maximum Power (P_o)	200 W

Table 2. The component parameters of the proposed topology.

Components	Parameters
Power Switch (S_1)	IXFK 55N50 (500 V/55 A)
Power Switches (S_2, S_3)	FDA38N30 (300 V/38 A)
Synchronous Rectification Switches (SR_1, SR_2)	IRFP4668 (200 V/130 A)
Diode (D_{fw})	DSEI 30-06A
Inductor (L_1)	259 µH
Inductor (L_2)	10 µH
Capacitor (C_1)	120 µF/420 V
Capacitor (C_{pT})	330 µF/200 V
Capacitor (C_o)	1500 µF/15 V
Turns (N_p: N_{s1}: N_{s2})	12:1:1

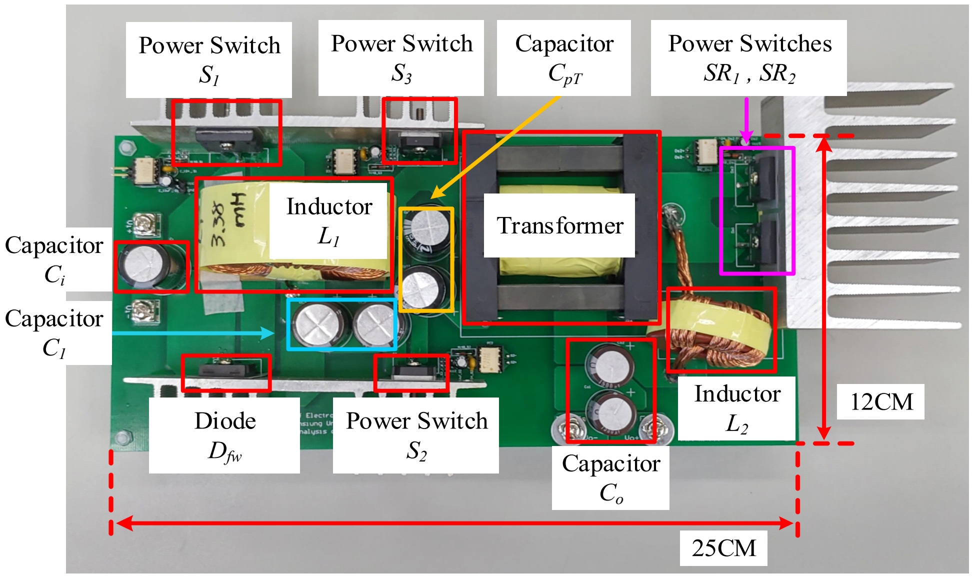

Figure 25. A photo of the proposed IBAHB.

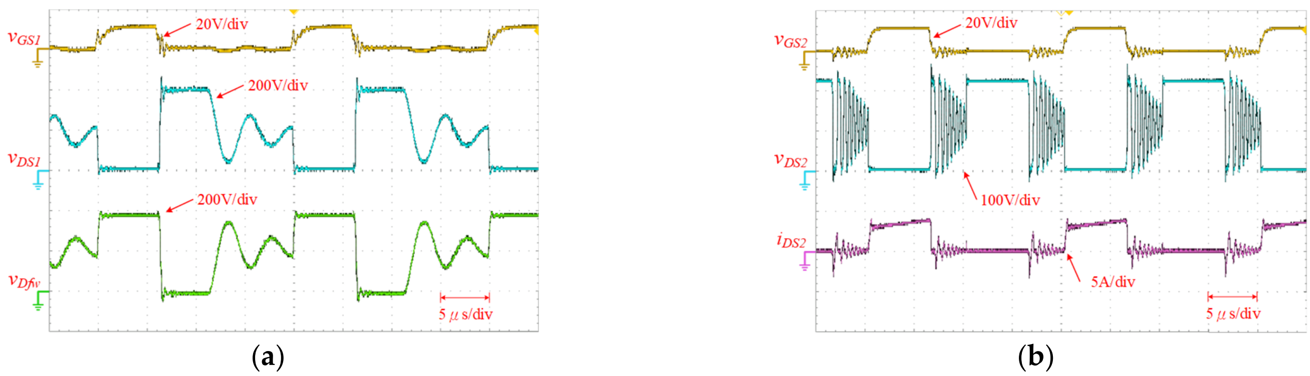

Figure 26. *Cont.*

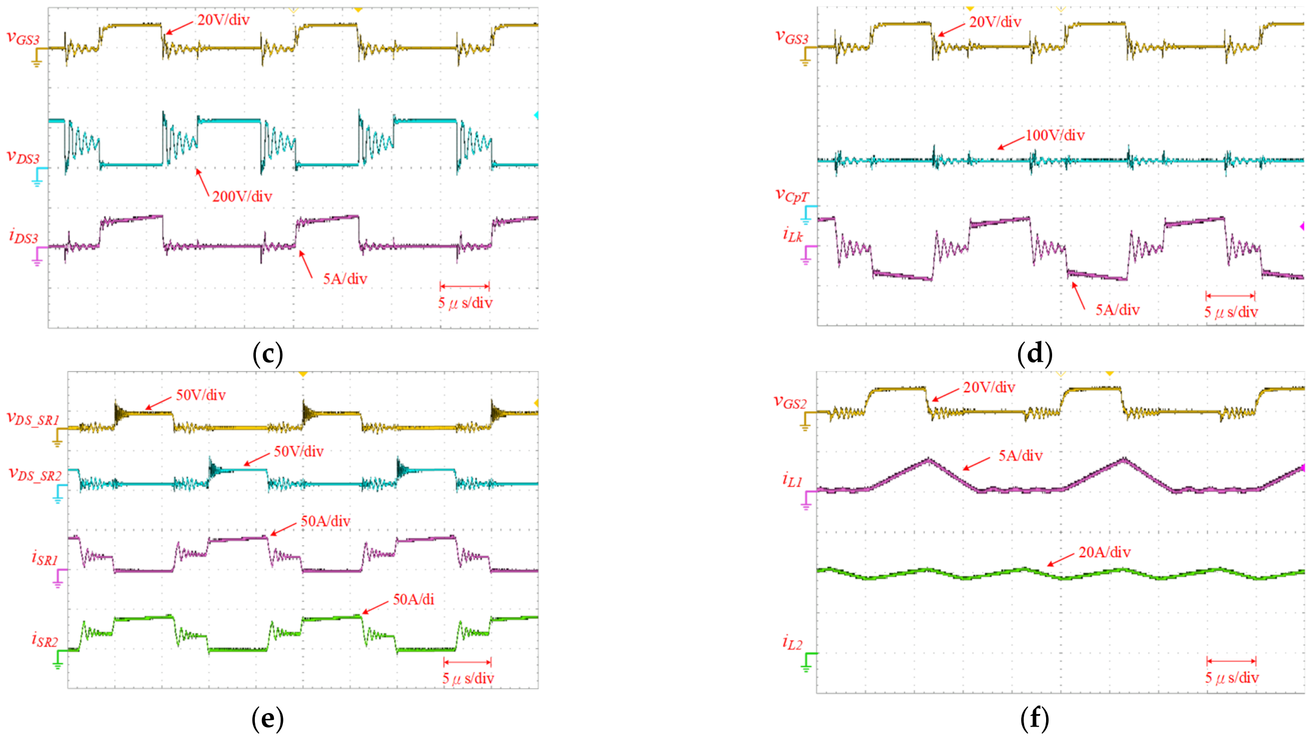

Figure 26. The experimental waveforms for the proposed IBAHB measured at a load of 200 W: (**a**) V_{GS1}, V_{DS1} and i_{DS1}, (**b**) V_{GS2}, V_{DS2} and i_{DS2}, (**c**) V_{GS3}, V_{DS3} and i_{DS3}, (**d**) V_{GS3}, $V_{C_{pT}}$ and i_{L_k}, (**e**) V_{DS_SR1}, V_{DS_SR2}, i_{SR1} and i_{SR2}, (**f**) V_{GS2}, i_{L_1} and i_{L_2}.

Figure 27 shows the reality of the measured data for the proposed converter, obtained by a power analyzer of HIOKI 3390.

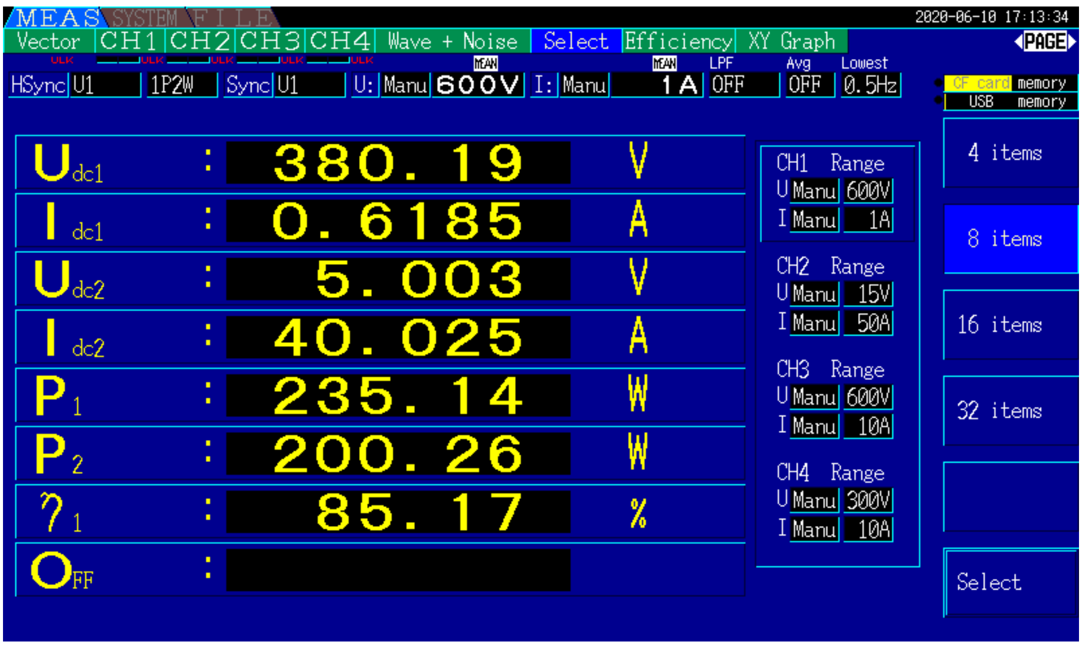

Figure 27. The reality of measured data of the proposed converter.

The maximum efficiency and full-load efficiency of the proposed topology are 86.65% and 85.17%, respectively. The experimental results confirm that the proposed topology is effective and feasible. When the circuit has a full load of 200 W, maximum efficiency occurs at 140 W, as shown in Figure 28.

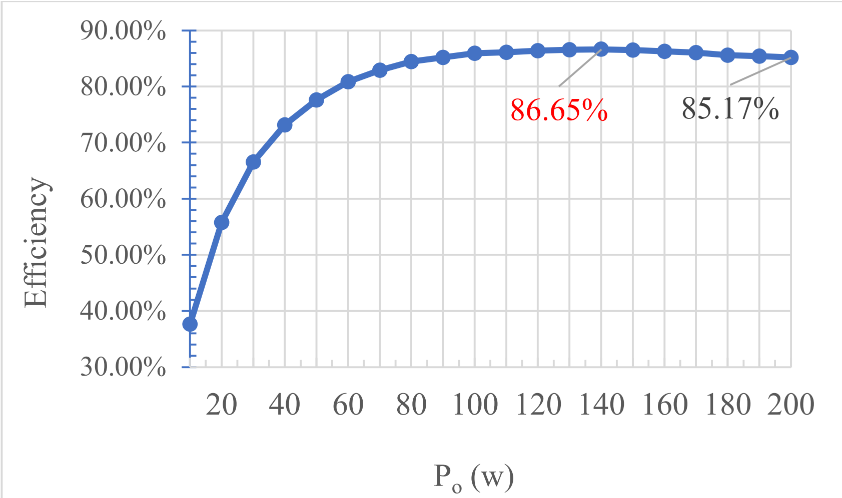

Figure 28. The efficiency curves of the proposed topology.

In Table 3, the proposed topology is compared with the number of MOSFETs and the number of diodes in Ref. [1]. It is shown that in the proposed topology, the main switch is a half-bridge and the synchronous rectification is complementary. The full load (250 W) efficiency of Ref. [1] is 81.44%, while the peak efficiency is 84.45%. Our proposed topology is 85.17% efficient at a full load of 200 W, but the maximum efficiency (86.65%) occurs at 140 W. In the voltage stress comparison, our proposed topology has lower voltage stress.

Table 3. Performance comparison between Ref. [1] and the proposed topology.

	Reference [1]	**Proposed Topology**
Voltage Gain	$\frac{N_s}{N_p} \times D^2$	$\frac{N_s}{N_p} \times D^2$
Quantities of MOSFETs	3	5
Quantities of Diodes	3	1
Quantities of Inductors	2	2
Quantities of Transformers	1	1
Quantities of Capacitors	3	3
Control Strategy	Easy	Normal
Output Current Ripple	Small	Small
Voltage Stress of S_1	$V_i + V_{C1}$	V_i
Peak Efficiency	84.45%	86.65%

The power switch signals are divided into two parts, as shown in Figure 24: the push–pull control type signal and its complementary signals. The push–pull control type signal enables the core of the transformer to be reset without additional reset circuits. The frequency of the current ripple is double the switching frequency, which is helpful for reducing the volume of the inductor L_2 and capacitor C_o. The frequency of the current ripple is twice the switching frequency. Additionally, it is helpful to reduce the volume of the inductor L_2 and capacitor C_o. Simultaneously, if the semiconductor component possesses a low $R_{DS(on)}$, it would help improve efficiency.

5. Conclusions

We propose a new high step-down conversion prototype through references, theoretical analysis and experimental results. The proposed topology has active clamping to recover the energy of leakage inductance, which would reduce the spike voltage. Hence, it could employ a semiconductor component with lower voltage stress. The proposed topology has the following advantage: by adding a step-down conversion architecture on the primary side, the potential of the transformer could be effectively reduced. Then, it could obtain a high step-down conversion ratio without an extremely low duty cycle or a high turns ratio.

The power switch signals are divided into two parts: the push–pull control type signal and its complementary signals. Additionally, the push–pull control type signal could reset the core of the transformer without additional reset circuits. The core of the transformer operates in quadrants I and III, so the utilization rate of the core is high which could reduce the volume of the whole transformer.

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