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An Integrated Four-Port DC/DC Converter for Renewable Energy Applications

Zhijun Qian, Osama Abdel-Rahman, Issa Batarseh

Institutions: University of Central Florida

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An Integrated Four-Port DC/DC Converter for Renewable Energy Applications

Zhijun Qian, *Student Member, IEEE*, Osama Abdel-Rahman, *Member, IEEE*, and Issa Batarseh, *Fellow, IEEE*

***Abstract*—This paper proposes a novel converter topology that interfaces four power ports: two sources, one bidirectional storage port, and one isolated load port. The proposed four-port dc/dc converter is derived by simply adding two switches and two diodes to the traditional half-bridge topology. Zero-voltage switching is realized for all four main switches. Three of the four ports can be tightly regulated by adjusting their independent duty-cycle values, while the fourth port is left unregulated to maintain the power balance for the system. Circuit analysis and design considerations are presented; the dynamic modeling and close-loop design guidance are given as well. Experimental results verify the proposed topology and confirm its ability to achieve tight independent control over three power-processing paths. This topology promises significant savings in component count and losses for renewable energy power-harvesting systems.**

***Index Terms*—DC–DC converter, half-bridge, multiple-input single-output (MISO), multiport, zero-voltage switching (ZVS).**

I. Introduction

AS INTEREST in renewable energy systems with various sources becomes greater than before, there is a supreme need for integrated power converters that are capable of interfacing, and concurrently, controlling several power terminals with low cost and compact structure. Meanwhile, due to the intermittent nature of renewable sources, a battery backup is normally required when the ac mains is not available.

This paper proposes a new four-port-integrated dc/dc topology, which is suitable for various renewable energy harvesting applications. An application interfacing hybrid photovoltaic (PV) and wind sources, one bidirectional battery port, and an isolated output port is given as a design example. It can achieve maximum power-point tracking (MPPT) for both PV and wind power simultaneously or individually, while maintaining a regulated output voltage.

Compared to the effort spent on the traditional two-port converter, less work has been done on the multiport converter [1]–[27]. But, due to the advantages like low cost and compact structure, multiport converters are reported to be designed for various applications, such as achieving three bus voltages of 14 V/42 V/H.V. (high voltage of around 500 V) in electric vehicles or hybrid electric vehicles [8], [9], interfacing the PV panel and a battery to a regulated 28-V bus in satellite platform power systems [19], [20], PV energy harvesting with ac mains [4] or the battery backup [6], hybrid fuel cell and battery systems [11], [15], and hybrid ultracapacitor and battery systems [12]. From the topology point of view, multiinput converters based on buck, boost, and buck–boost topologies have been reported in [1]–[7]. The main limitation of these configurations is the lack of a bidirectional port to interface storage device. Multiport converters are also constructed out of a multiwinding transformer based on half-bridge or full bridge topologies [8]–[17]. They can meet isolation requirement and also have bidirectional capabilities. However, the major problem is that they use too many active switches, in addition to the bulky transformer, which cannot justify the unique features of low component count and compact structure for the integrated multiport converter.

The proposed four-port dc/dc converter has bidirectional capability and also has one isolated output. Its main components are only four main switches, two diodes, one transformer, and one inductor. Moreover, zero-voltage switching (ZVS) can be achieved for all main switches to allow higher efficiency at higher switching frequency, which will lead to more compact design of this multiport converter. The control design is also investigated based on the modeling of this modified half-bridge topology. In addition, a decoupling network is introduced to allow the separate controller design for each power port. Finally, a prototype has been built to verify the four-port converter's circuit operation and control capability. The proposed converter is a valuable candidate for low-power renewable energy harvesting applications.

II. Topology and Circuit Analysis

The four-port topology is derived based on the traditional two-port half-bridge converter, which consists of two main switches S_1 and S_2. As shown in Fig. 1, one more input power port can be obtained by adding a diode D_3 and an active switch S_3. Another bidirectional power path can be formed by adding a freewheeling branch across the transformer primary side, consisting of a diode D_4 and an active switch S_4. As a result, the topology ends up with four active switches and two diodes, plus the transformer and the rectification circuit. The proposed converter topology is suitable for a number of power-harvesting applications, and this paper will target the hybrid PV wind application. It should be noted that since the wind turbine normally generates a three-phase ac power, an ac/dc rectifier needs to be installed before this four-port dc/dc interface and after the wind turbine output. And the rectification stage can utilize either active power factor correction (PFC) or passive PFC. However, the ac/dc solution is beyond the scope of this paper.

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Z. Qian and I. Batarseh are with the University of Central Florida, Orlando, FL 32816 USA (e-mail: zqian@knights.ucf.edu; batarseh@mail.ucf.edu).

O. Abdel-Rahman is with the Advanced Power Electronics Corporation, Orlando, FL 32816 USA (e-mail: sabdel@apecor.com).

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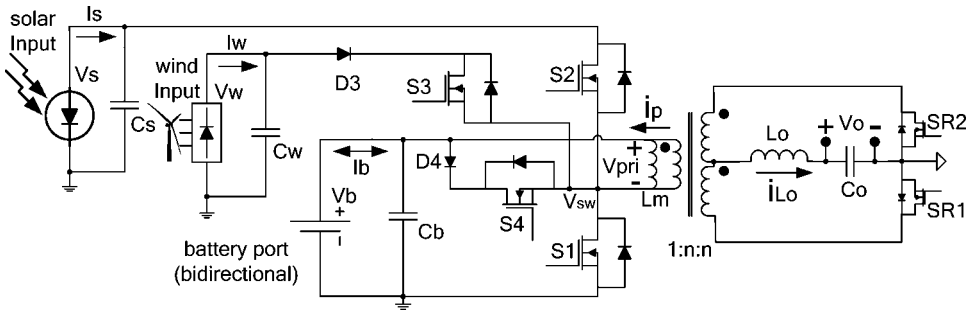

Fig. 1. Four-port half-bridge converter topology, which can achieve ZVS for all four main switches (S_1, S_2, S_3, and S_4) and adopts synchronous rectification for the secondary side to minimize conduction loss.

TABLE I
VALUES OF CIRCUIT PARAMETERS

output inductor	Lo	45 μH	solar port filter capacitor	Cs	100 μF
magnetizing inductor	Lm	45 μH	battery port filter capacitor	Cb	330 μF
output filter capacitor	Co	330 μF	wind port filter capacitor	C_w	100 μF

As shown in Fig. 1, the derived four-port-modified half-bridge converter provides three independent control variables, namely duty cycles d_1, d_2, and d_3 to control S_1, S_2, and S_3, respectively, while S_4 will be controlled by 1–d_1–d_2–d_3. This allows tight control over three of the converter ports, while the fourth port provides the power balance in the system. The switching sequence ensures a clamping path for the energy of the leakage inductance of the transformer. This energy is further utilized to achieve ZVS for all primary switches for a wide range of source and load conditions. The secondary side adopts a synchronous rectifier to minimize the conduction loss. This also simplifies the feedback controller design, because the transition from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) is avoided.

The values of circuit parameters used in the simulation and experimental circuit are listed in the following table (see Table I).

A. Driving Scheme

Fig. 2 illustrates a possible modulation approach to realize the constant frequency pulsewidth modulation (PWM) control, where V_{sawtooth} is the sawtooth carrier waveform for modulation, V_{c1}, V_{c2}, and V_{c3} are control voltages derived from the voltage or current feedback controllers. By modulating these control voltages, driving signals for S_1, S_2, and S_3 can be generated, respectively. Then, by reversing S_1 and S_3 driving signals, S_4 and two SR signals can be obtained. It should be noted that S_2, S_3, and S_4 do not need to be gated ON at the same time; instead, S_3 is only required to turn ON a little earlier before S_2 turns OFF, and S_4 is only required to turn ON a little earlier before S_3 turns OFF. No dead time is necessary between S_2 and S_3, nor between S_3 and S_4, because the existence of diodes can prevent shoot-through problems. But the dead time between S_1 and S_2 and between S_1 and S_4 is necessary to prevent shoot-through, and also to create ZVS conditions for S_1 and S_2.

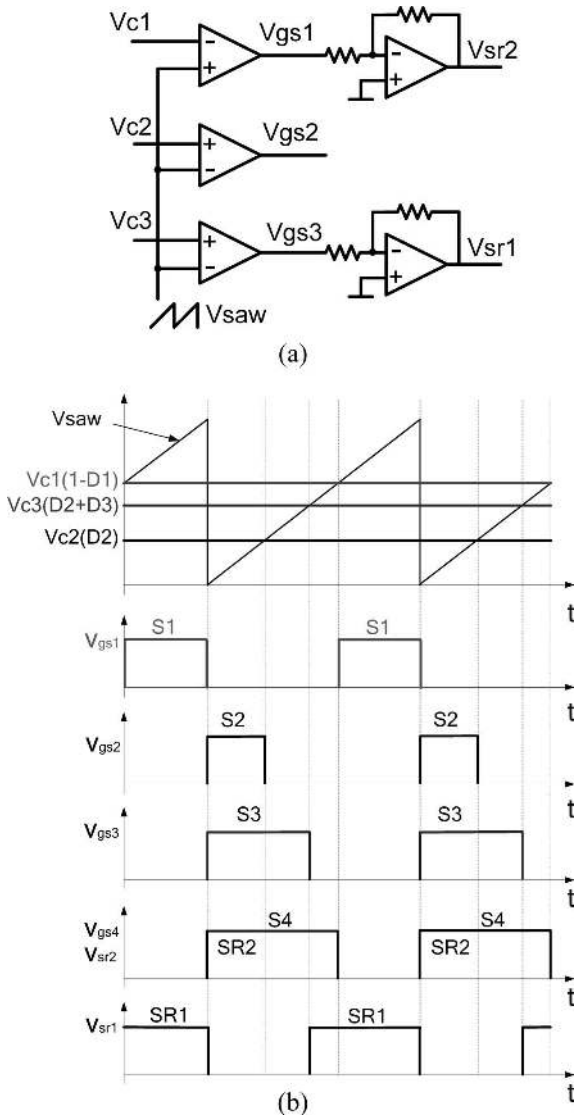

Fig. 2. Proposed modulation scheme. (a) PWM modulation circuits. (b) Driving signal key waveforms.

B. Principle of Circuit Operation

The steady-state waveforms of the four-port converter are shown in Fig. 3, and the various operation stages in one switching cycle are shown in Fig. 4. To simplify the analysis of

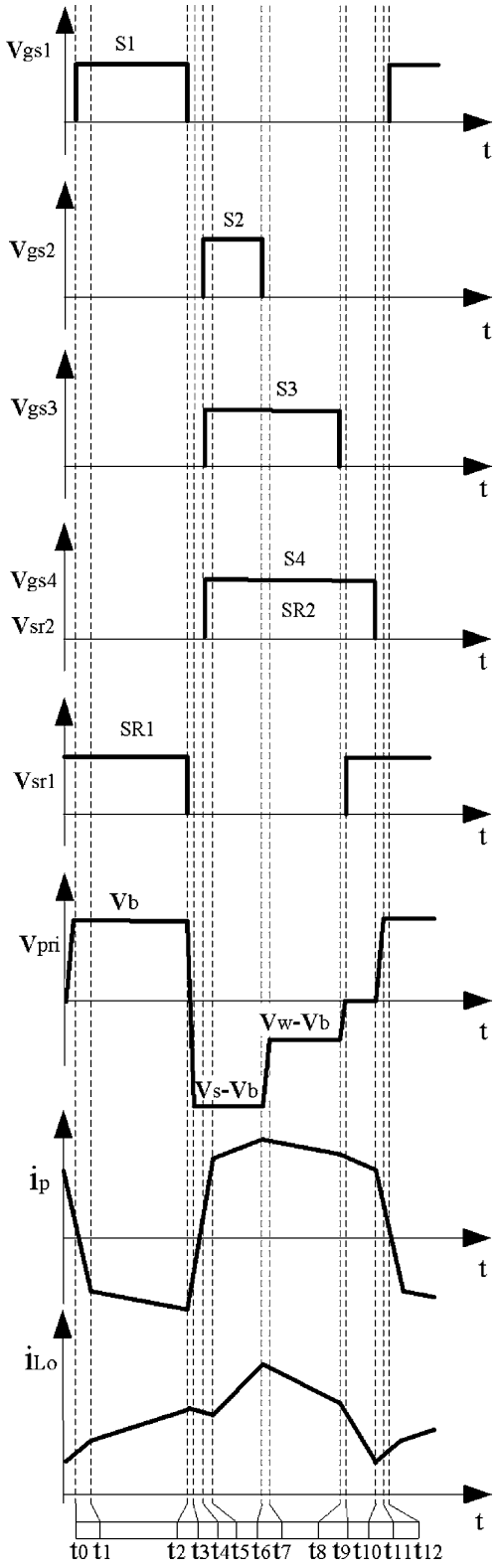

Fig. 3. Steady-state waveforms of the four-port half-bridge converter.

operation, components are considered ideal, except otherwise indicated. The main operation stages are described as follows.

Stage 1 (t_0–t_1): Before this stage begins, the body diode of S_1 is forced on to recycle the energy stored in the transformer leakage inductor, and the output is freewheeling. At time t_0, S_1 is gated ON with ZVS, and then, the leakage inductor is reset to zero and reverse-charged.

Stage 2 (t_1–t_2): At time t_1, the transformer primary current increases to the reflected current of i_{L_o}, the body diode of SR_2 becomes blocked, and the converter starts to deliver power to output.

Stage 3 (t_2–t_3): At time t_2, S_1 is gated OFF, causing the leakage current i_p to charge the S_1 parasitic capacitor and discharge the S_2, S_3, and S_4 parasitic capacitors.

Stage 4 (t_3–t_4): At time t_3, the voltage across the S_2 parasitic capacitor is discharged to zero, and the S_2 body diode conducts to carry the current, which provides the ZVS condition for S_2. During this interval, the output is freewheeling through SR_1 and SR_2 body diodes.

Stage 5 (t_4–t_5): At time t_4, S_2 is gated ON with ZVS, and then, the leakage inductor is reset to zero and reverse-charged. The output inductor current drop from t_2 to t_5 is due to the leakage inductor discharge/charge.

Stage 6 (t_5–t_6): At time t_5, the transformer primary current increases to the reflected current of i_{L_o}, the body diode of SR_1 is blocked, and the converter starts to deliver power to output.

Stage 7 (t_6–t_7): At time t_6, S_2 is gated OFF, thus causing the leakage current i_p to charge the S_2 parasitic capacitor and discharge the S_1 and D_3 parasitic capacitors.

Stage 8 (t_7–t_8): At time t_7, the voltage across D_3 is discharged to zero, and then, D_3 conducts. S_3 is gated ON before this time; therefore, S_3 has natural ZVS. Output inductor current freewheels through SR_2 during this period.

Stage 9 (t_8–t_9): At time t_8, S_3 is gated OFF, thus causing the leakage current i_p to charge S_2 and S_3 parasitic capacitors and discharge S_1 and D_4 parasitic capacitors.

Stage 10 (t_9–t_{10}): At time t_9, the voltage across D_4 is discharged to zero and D_4 conducts. Since S_4 is gated ON before this time, the leakage current freewheels through D_4 and S_4, so that the leakage energy is trapped. On the secondary side, output inductor current freewheels through SR_1 and SR_2.

Stage 11 (t_{10}–t_{11}): At time t_{10}, S_4 is gated OFF, causing the trapped leakage energy to discharge the S_1 parasitic capacitor and charge the S_2, S_3 and S_4 parasitic capacitors.

Stage 12 (t_{11}–t_{12}): At time t_{11}, the voltage across S_1 is discharged to zero, and the S_1 body diode conducts to carry the current, which provides ZVS condition for S_1. During this interval, the output is freewheeling. This is the end of the switching cycle.

C. Steady-State Analysis

Assuming an ideal converter, the steady-state voltage governing relations between different port voltages can be determined by equating the voltage–second product across the converter's two main inductors to zero. First, using volt–second balance across the primary transformer magnetizing inductance L_M in CCM, we have

$$V_b D_1 = (V_s - V_b)D_2 + (V_w - V_b)D_3. \tag{1}$$

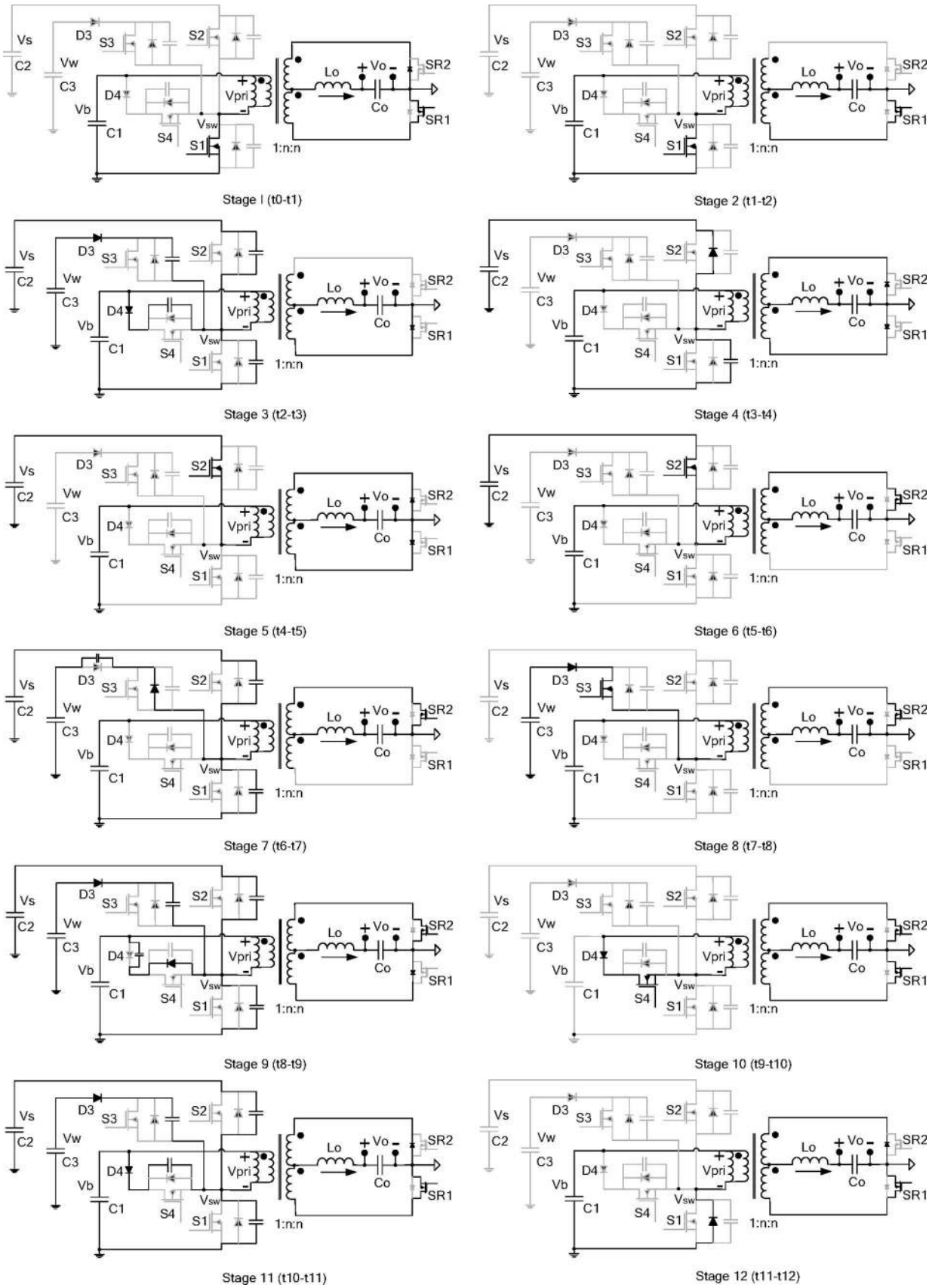

Fig. 4. Operation stages of the four-port half-bridge converter.

Assuming CCM operation, the voltage-second balance across the load filter inductor L_o then yields

$$V_b D_1 + (V_s - V_b)D_2 + (V_w - V_b)D_3 = \frac{V_o}{n} \quad (2)$$

where n is the turns ratio of the transformer, V_s, V_w, V_b, V_o are the solar input, wind input, battery, and output voltages, respectively.

The following equation is based on the power balance principle, by assuming a lossless converter, steady-state port currents can be related as follows:

$$V_s I_s + V_w I_w = V_b I_b + V_o I_o \quad (3)$$

where I_s, I_w, I_b, I_o are the average solar input, wind input, battery bidirectional, and load currents, respectively. The battery current I_b is positive during charging and negative during discharging.

D. ZVS Analysis

ZVS of the switches S_1 and S_2 can be realized through the energy stored in the transformer leakage inductor, while ZVS of S_3 and S_4 is always maintained, because the proposed driving scheme ensures that paralleling diodes of S_3 and S_4 will be forced on before the two switches turn ON.

After S_4 is turned OFF, the leakage energy is released to discharge the S_1 parasitic capacitor and charge S_2, S_3, and S_4's parasitic capacitors, to create the ZVS condition of S_1. And the following condition should be satisfied:

$$\frac{1}{2}L_k(I_M + nI_o)^2 > 2C_{\text{oss}}V_b^2 + C_{\text{oss}}V_s V_b + C_{\text{oss}}V_w V_b, \quad I_M + nI_o > 0 \quad (4)$$

where L_k is the transformer leakage inductance, MOSFET parasitic capacitances of S_1, S_2, S_3 and S_4 are assumed to be equal as C_{oss}, and I_M is the average transformer magnetizing current, which satisfies:

$$I_b = D_1(I_M - nI_o) + D_2(I_M + nI_o) + D_3(I_M + nI_o). \quad (5)$$

Rearranging (5), we can obtain I_M as follows:

$$I_M = \frac{I_b + (D_1 - D_2 - D_3)\, nI_o}{D_1 + D_2 + D_3}. \quad (6)$$

After S_1 is turned OFF, the leakage energy will charge the S_1 parasitic capacitor and discharge S_2, S_3, and S_4's parasitic capacitors to achieve ZVS for S_2

$$\frac{1}{2}L_k(I_M - nI_o)^2 > C_{\text{oss}}V_s^2 + \frac{1}{2}C_{\text{oss}}V_w^2 + \frac{1}{2}C_{\text{oss}}V_b^2, \quad I_M - nI_o < 0. \quad (7)$$

According to (7), when the load current I_o is small and the transformer magnetizing current I_M is large, $I_M - nI_o < 0$ cannot be met. In other words, ZVS of S_2 will be lost. However, in most load/source conditions, ZVS of S_2 is achievable.

It should be noted that ZVS of S_3 and S_4 can be naturally achieved if the voltage relation $V_b < V_w < V_s$ is satisfied to ensure that the paralleling diodes will always be forced on before these switches turn ON. On one hand, $V_w < V_s$ is not difficult to meet since the solar port and wind port can be reversed if the wind port voltage V_w is larger than the solar port voltage V_s. Even if V_w is not always lower than V_s in the whole voltage ranges, the converter itself still works, but may lose some conduction period for the S_2 branch depending on the driving overlap of S_2 and S_3. The solution is to change the driving scheme to avoid the S_2 and S_3 overlap. On the other hand, it is a step-down conversion from PV or wind port to battery port; therefore, the battery voltage V_b will be always lower than the PV voltage V_s and the wind source voltage V_w.

To sum up, ZVS of all main switches can be achieved to maintain higher efficiency when the converter is operated at higher switching frequency, because of the potential savings in switching losses.

E. Circuit Design Considerations

When considering the semiconductor stresses, this modified half-bridge topology shows striking similarity to its traditional half-bridge counterpart. The major difference is that the transformer design of this four-port converter needs to allow for a dc current flow, and therefore, becomes similar to an inductor or a flyback transformer design. The dc biasing current rating is dictated by (6), which determines the amount of the air gap to be inserted. Other than the transformer, the circuit design and optimization technique used for the traditional half-bridge topology can be used here for this four-port topology, which provides great convenience for the practicing engineers to implement the power stage design.

III. Control Structure and Dynamic Modeling

The proposed converter has three freedoms to control the power flow of three power ports, while the fourth port is to maintain the power balance. That means the operating point of up to three ports can be tightly regulated, while the fourth port should be left "flexible" and would operate at any point that satisfies the power balance constraints. The choice of the flexible power port dictates the feedback control layout, which is based on different control objectives. For instance, if the battery is chosen to be left "flexible," the maximal power from the solar and wind sources can be tracked by their port voltages or currents independently, and the load voltage can be regulated by a voltage feedback as well.

A. Control Structure

Fig. 5 shows the control structure for the hybrid PV wind system. Three feedback controllers are as follows: a solar voltage regulator (SVR), a wind voltage regulator (WVR), and an output voltage regulator (OVR).

The OVR loop is simply a voltage-feedback loop, closed around the load port, and duty cycle d_1 is used as its control input. The SVR loop is used to regulate the PV panel voltage to its reference value, which is provided by an MPPT controller. And the reference value represents an estimate of the optimal operating PV voltage; duty cycle d_2 is used as its control input.

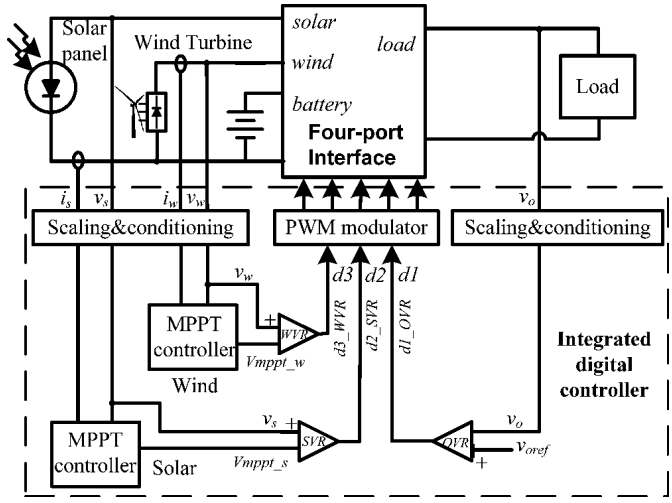

Fig. 5. Possible control structure to achieve MPPT for the PV panel and the wind turbine, meanwhile maintaining output voltage regulation. OVR, SVR, and WVR loops are to control d_1, d_2, and d_3, respectively.

The WVR loop is taking a very similar structure to SVR, except that its voltage reference represents the optimal operating voltage of the rectified wind turbine output voltage. The WVR loop is made to control d_3. This control strategy allows the load voltage to be tightly regulated while maximizing the PV and wind power harvesting. In this system, the battery storage plays the significant role of balancing the system energy by injecting power at heavy loads and absorbing excess power when available PV and wind power exceeds the load demand.

B. Dynamic Modeling

In order to design the SVR, WVR, and OVR controllers, a small signal model of the four-port converter is desired. The detailed modeling procedure can refer to [19], which is proposed for a three-port converter. And for this four-port converter, the general modeling procedure is very similar to [19]. Therefore, to avoid unnecessary repetition, only a brief introduction is given here. First, state-space equations for five energy storage elements during the four main circuit stages are developed. For the aforementioned mode of operation, these include the solar-side capacitor C_s, the wind-side capacitor C_w, the transformer magnetizing inductor L_M, the output inductor L_o, and the output capacitor C_o. In the next step, state-space equations in the four main circuit stages (corresponding to the turn ON of four main switches) will be averaged, and then applied with the small signal perturbation. Finally, the first-order small-signal perturbation components will be collected to form the matrices A and B, which actually represent the converter power stage model. It should be noted that the symbolic derivation of these transfer functions is fairly tedious. Alternatively, the dynamics of the plant can be calculated by computer software like MATLAB. The resultant state-space averaging model takes the following form:

$$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t), \qquad \hat{y}(t) = I\hat{x}(t) \tag{8}$$

$$A = \begin{bmatrix} -\dfrac{1}{R_s C_s} & 0 & \dfrac{-D_2}{C_s} & \dfrac{-nD_2}{C_s} & 0 \\ 0 & -\dfrac{1}{R_w C_w} & \dfrac{-D_3}{C_w} & \dfrac{-nD_3}{C_w} & 0 \\ \dfrac{D_2}{L_M} & \dfrac{D_3}{L_M} & 0 & 0 & 0 \\ \dfrac{nD_2}{L_o} & \dfrac{nD_3}{L_o} & 0 & 0 & \dfrac{-1}{L_o} \\ 0 & 0 & 0 & \dfrac{1}{C_o} & -\dfrac{1}{RC_o} \end{bmatrix},$$

$$\hat{x}(t) = \begin{bmatrix} \hat{v}_s(t) \\ \hat{v}_w(t) \\ \hat{i}_{L_m}(t) \\ \hat{i}_{L_o}(t) \\ \hat{v}_o(t) \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & \dfrac{-I_{L_m} - (nV_o/R)}{C_s} & 0 \\ 0 & 0 & \dfrac{-I_{L_m} - (nV_o/R)}{C_w} \\ -\dfrac{V_b}{L_M} & \dfrac{V_s - V_b}{L_M} & \dfrac{V_w - V_b}{L_M} \\ \dfrac{nV_b}{L_o} & \dfrac{n(V_s - V_b)}{L_o} & \dfrac{n(V_w - V_b)}{L_o} \\ 0 & 0 & 0 \end{bmatrix},$$

$$\hat{u}(t) = \begin{bmatrix} \hat{d}_1(t) \\ \hat{d}_2(t) \\ \hat{d}_3(t) \end{bmatrix} \tag{9}$$

where $\hat{x}(t)$ is a matrix containing the small signal state variables $\hat{v}_s(t)$, $\hat{v}_w(t)$, $\hat{i}_{L_m}(t)$, and $\hat{i}_{L_o}(t)$, and $\hat{v}_o(t)$, $\hat{u}(t)$ is a matrix containing the control inputs $\hat{d}_1(t)$, $\hat{d}_2(t)$, and $\hat{d}_3(t)$, $\hat{y}(t)$ is a matrix containing the system outputs, and I is the identity matrix.

With matrices A and B, transfer functions for PV, wind and output voltages to different duty-cycle values can be extracted according to (10). For example, $G(s)(5,1)$ represents the fifth state variable v_o and the first control variable d_1, thus equals to open-loop transfer function of $v_o(s)/d_1(s)$. Therefore, the row number denotes the sequence of state variable, and the column number denotes that of control input

$$G = (sI - A)^{-1} B$$
$$g_{11} = G(s)(5,1), \quad g_{21} = G(s)(1,1), \quad g_{31} = G(s)(2,1)$$
$$g_{12} = G(s)(5,2), \quad g_{22} = G(s)(1,2), \quad g_{32} = G(s)(2,2)$$
$$g_{13} = G(s)(5,3), \quad g_{23} = G(s)(1,3), \quad g_{33} = G(s)(2,3). \tag{10}$$

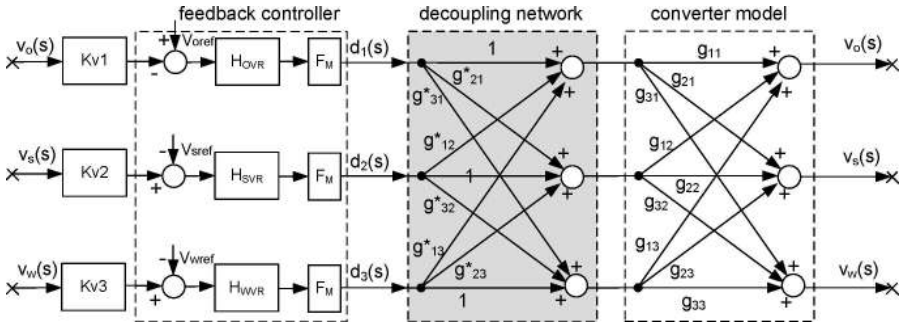

Fig. 6. Small signal model diagram, control inputs and outputs are decoupled to enable separate controller design. The far right signals are routed to the far left ones in this diagram. $V_{\rm sref}$, $V_{w\rm ref}$, and $V_{o\rm ref}$ are the references for solar, wind and output voltages, respectively. $H_{\rm SVR}$, $H_{\rm WVR}$, and $H_{\rm OVR}$ are the compensators need to be designed.

Fig. 6 illustrates the small signal model diagram when closing SVR, WVR, and OVR loops, which consists of the converter model and the feedback controllers. F_M represents the PWM modulator gain and different Kv values represent different voltage signal sensing gains, which can be treated as the fixed proportional values.

C. Decoupling Method

As can be seen from Fig. 6, the three control loops are coupled with each other, which make it difficult to design close-loop compensators for each control loop. Therefore, a decoupling network, as shadowed in Fig. 6, is introduced, so that the control loops can be designed independently with different control-loop bandwidth requirement. Since output-port voltage regulation requirement is the most stringent of the three and the PV panel and wind turbine characteristics are relatively slower, the SVR loop is designed to have a one-decade lower bandwidth than that of OVR. Moreover, WVR bandwidth can be set to be lower than that of SVR to further reduce SVR and WVR loop interactions, since the mechanical behavior of wind blades is slower than the PV behavior of PV panels.

The derivation of decoupling network G^* is described as follows. The state vector matrix X can be written as $X = G{\cdot}U^*$, where U^* is the modified input vector made up of duty cycles $U, U^* = G^*{\cdot}U$. Therefore, $X = G{\cdot}G^*{\cdot}U$. According to modern control theory, our goal is to make $G{\cdot}G^*$ a diagonal matrix to allow one control input to determine one output independently. Therefore, based on $G^* = G^{-1}{\cdot}X{\cdot}U^{-1}$, the decoupling matrix G^* can be derived and simplified as follows:

$$G^* = \begin{bmatrix} g_{11}^* & g_{12}^* & g_{13}^* \\ g_{21}^* & g_{22}^* & g_{23}^* \\ g_{31}^* & g_{32}^* & g_{33}^* \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{g_{13}g_{32}-g_{12}g_{33}}{g_{11}g_{33}-g_{13}g_{31}} & \dfrac{g_{12}g_{23}-g_{13}g_{22}}{g_{11}g_{22}-g_{12}g_{21}} \\ \dfrac{g_{23}g_{31}-g_{21}g_{33}}{g_{22}g_{33}-g_{23}g_{32}} & 1 & \dfrac{g_{13}g_{21}-g_{11}g_{23}}{g_{11}g_{22}-g_{12}g_{21}} \\ \dfrac{g_{21}g_{32}-g_{22}g_{31}}{g_{22}g_{33}-g_{23}g_{32}} & \dfrac{g_{12}g_{31}-g_{11}g_{32}}{g_{11}g_{33}-g_{13}g_{31}} & 1 \end{bmatrix}. \tag{11}$$

It should be noted that the decoupling network is only intended to calculate and derive the separate control objects, while it does not need to be implemented in the real controller design. In other word, the decoupling can be taken as one part of the control objects, but not included in the compensators. Now, the cross-coupled three-loop control system is decoupled into three independent single-loop subsystems. The system can then be controlled using independent loop controllers and each compensator can be designed separately as well. For example, the OVR controller can then be designed based on the following plant transfer function:

$$\frac{v_o(s)}{d_1(s)} = g_{11} + g_{12}\frac{g_{23}g_{31}-g_{21}g_{33}}{g_{22}g_{33}-g_{23}g_{32}} + g_{13}\frac{g_{21}g_{32}-g_{22}g_{31}}{g_{22}g_{33}-g_{23}g_{32}}. \tag{12}$$

The open-loop OVR-loop bode plot implies that it has two main poles at around L_oC_o resonance, which causes a -40 dB/decade slope for gain plot while not having enough phase margin. This double pole characteristic is because that this topology is buck-type derived in terms of the output port. Therefore, the design objective is to make the gain plot pass 0 dB line at -20 dB/decade slope while maintaining a sufficient phase margin. A tradition PID controller is recommended to boost the phase. The PID compensator of $H_{\rm OVR}$ takes the following form:

$$H_{\rm OVR} = \frac{80(s/2\pi 400+1)(s/2\pi 500+1)}{s(s/2\pi 4000+1)(s/2\pi 5000+1)}. \tag{13}$$

Similarly, SVR and WVR controllers can also be designed once their decoupled plant transfer functions are derived. The SVR and WVR bode plots before compensation have very high bandwidth. But the control bandwidth should be reduced to minimize loop interaction, SVR compensator $H_{\rm SVR}$ is then designed to enforce relatively low control-loop bandwidth with some phase boost. Therefore. a PID controller with very low gain is adopted to achieve this design goal. And WVR compensator $H_{\rm WVR}$ is set at even lower gain to have a lower bandwidth than SVR loop. $H_{\rm SVR}$ and $H_{\rm WVR}$ are designed as follows:

$$H_{\rm SVR} = \frac{0.08(s/2\pi 20+1)(s/2\pi 30+1)}{s(s/2\pi 1000+1)(s/2\pi 2000+1)} \tag{14}$$

$$H_{\rm WVR} = \frac{0.02(s/2\pi 20+1)(s/2\pi 30+1)}{s(s/2\pi 1000+1)(s/2\pi 1500+1)}. \tag{15}$$

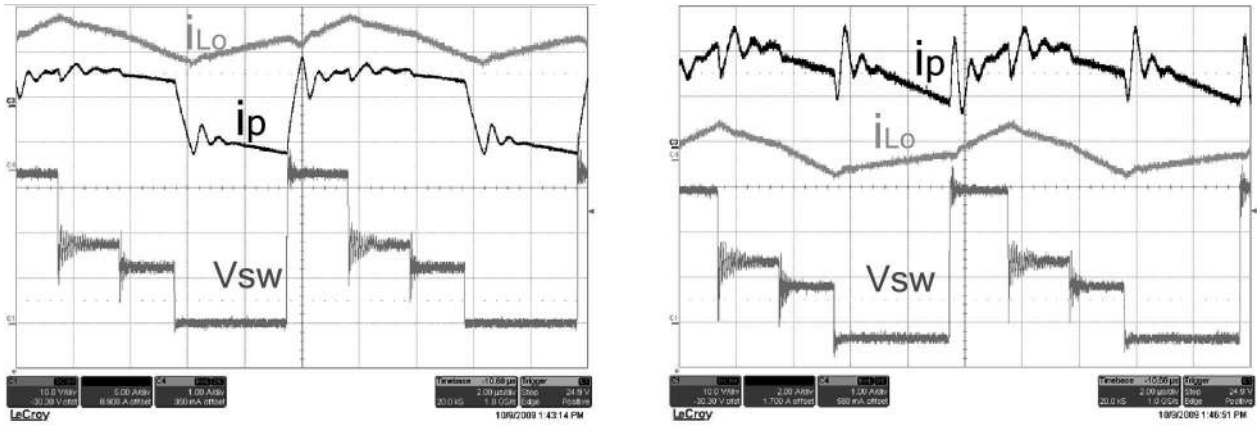

Fig. 7. Steady-state waveforms. (a) Loading the output port when the battery current is zero. (b) Loading the battery port when the output current is zero.

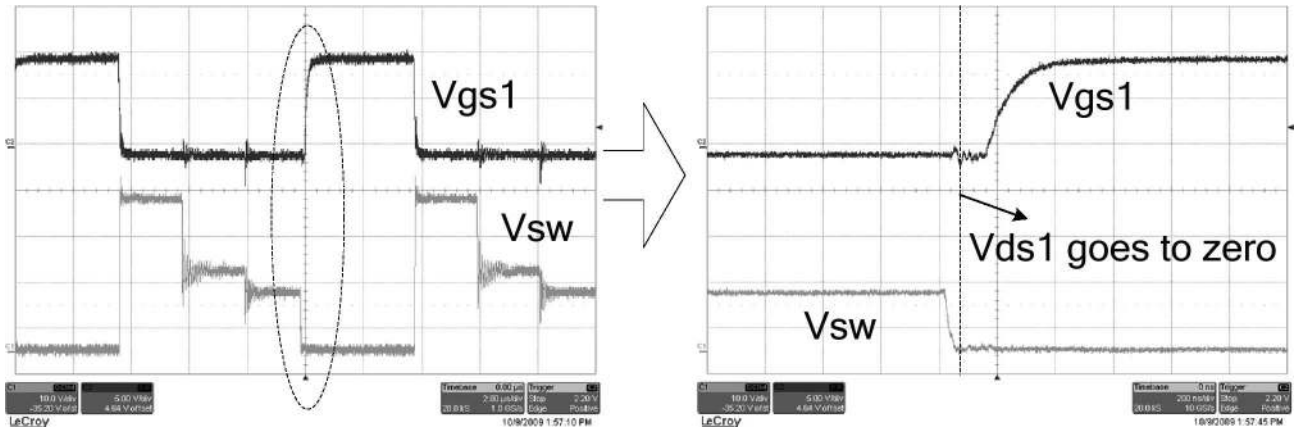

Fig. 8. $V_{\rm gs}$ and $V_{\rm sw}$ of the switch S_1.

IV. Experimental Results

A four-port dc/dc converter prototype is built to verify the circuit operation. The circuit parameters are: solar port, 30–40 V/1.5 A; wind port, 20–30 V/1.5 A; battery port, 12–18 V/3 A; and output port, 12 V/3.3 A. The switching frequency is 100 kHz, and it is implemented by the digital control to achieve the close-loop regulation.

Fig. 7 gives the steady-state waveforms when loading the output port (a) and loading the battery port (b). The switch-node voltage $V_{\rm sw}$ shows a four-stage wave shape, corresponding to the turn ON of four main switches with four different voltage levels. In addition, there is no CCM and DCM transition for the output inductor current i_{L_o}, which avoids the sharp change of plant dynamic characteristics and simplifies the output-voltage feedback-controller design. The transformer magnetizing current i_p is determined by both the reflected output current and the battery current.

Figs. 8 and 9 show the gating signal $V_{\rm gs}$ and switching node $V_{\rm sw}$ waveforms of the switches S_1 and S_2. Since S_3 and S_4 have ZVS under all conditions, as mentioned earlier, only S_1 and S_2 waveforms are presented here. The conclusion is that all four main switches can achieve ZVS, because they all turn ON after their $V_{\rm ds}$ go to zero.

Table II shows eight different load and source combinations with each one of them to be either 10% or 90% load/source condition, while the battery port provides the power balance. The test setup is realized by connecting the solar port and wind port of the converter to two independent PV array simulators instead of the solar panel and the wind turbine. Then, two different I–V curves are assigned for the solar and wind port, and the DSP code is tuned so that the SVR and WVR voltage references are at 10% or 90% rated current point. As a result, two sources will have four different combinations. A battery is connected to sink the excess power or source the deficit power, and the load is set to sink either 10% or 90% rated output current. Therefore, there are eight different conditions for one load and two sources, as described in Table II.

Fig. 10 depicts all three-port voltages under different load/source conditions. The cross regulation of V_s, V_w, and V_o are 0.5%, 0.6% and 1.1%, respectively. This confirms its capability to regulate three of the four ports tightly.

Fig. 11 shows the efficiency curve under different load/source conditions, as shown in Table II. The highest efficiency is 93.9%

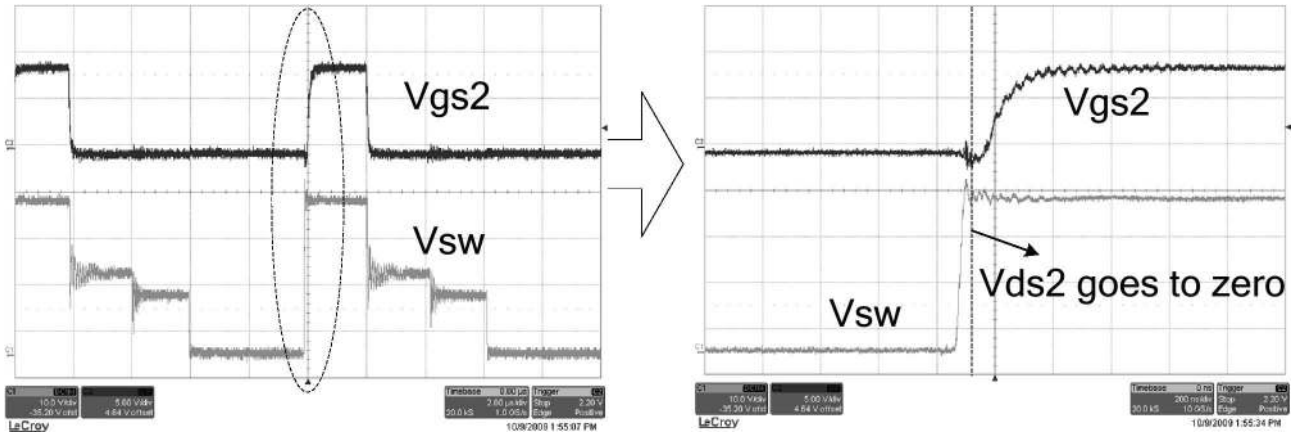

Fig. 9. $V_{\rm gs}$ and $V_{\rm sw}$ of the switch S_2.

TABLE II
DIFFERENT LOAD/SOURCE CURRENT LEVEL CONDITIONS

	Load/Source Current Level Conditions (%)		
	V_s=35.6V	V_w=28.2V	V_o=12V
Case1	10	10	90
Case2	90	10	90
Case3	10	90	90
Case4	90	90	90
Case5	90	10	10
Case6	10	90	10
Case7	90	90	10
Case8	10	10	10

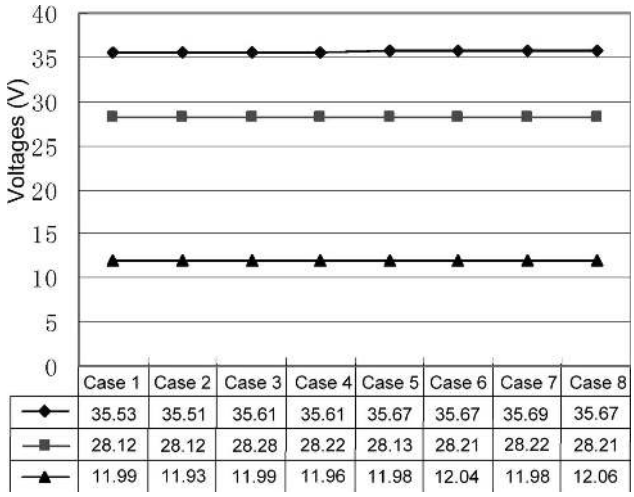

Fig. 10. Solar port, wind port, and output port voltages under different load/source conditions.

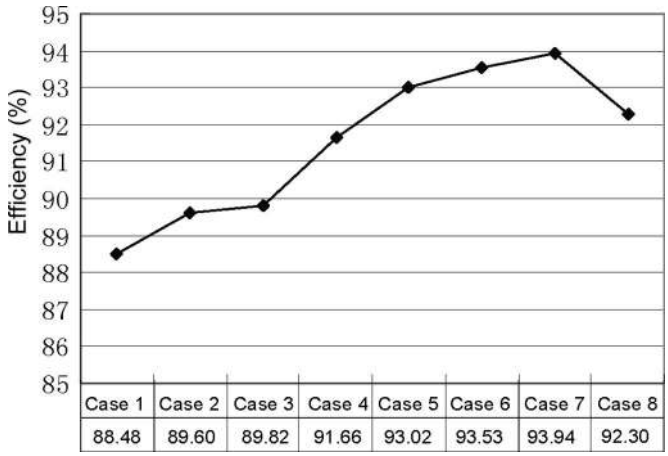

Fig. 11. Efficiency under different load/source conditions.

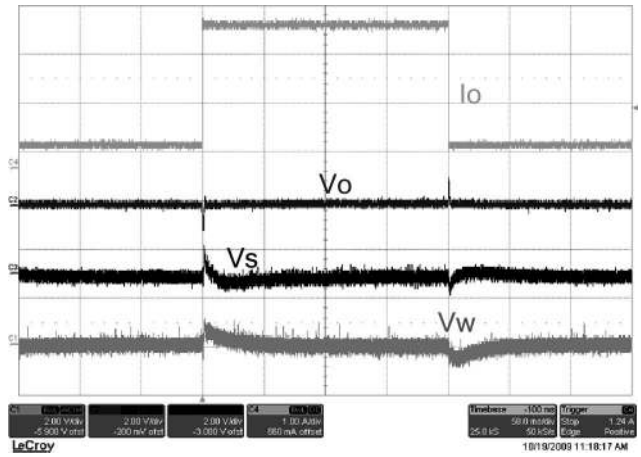

Fig. 12. Transient response of solar, wind, and output voltages when the load is perturbed by a step change between 10% and 90% rated output current.

when most of the power is exchanged within the primary side from the solar and wind port to the battery port; the reason is that this operation has minimal transformer losses.

Fig. 12 shows the transient response of the PV voltage, wind voltage, and output voltage to a load transient between 0.33 and 3 A, when SVR, WVR, and OVR loops are closed. Although the reference values of $V_{s\rm ref}$ and $V_{w\rm ref}$ are given as the fixed values rather than being constantly updated by the MPPT controllers,

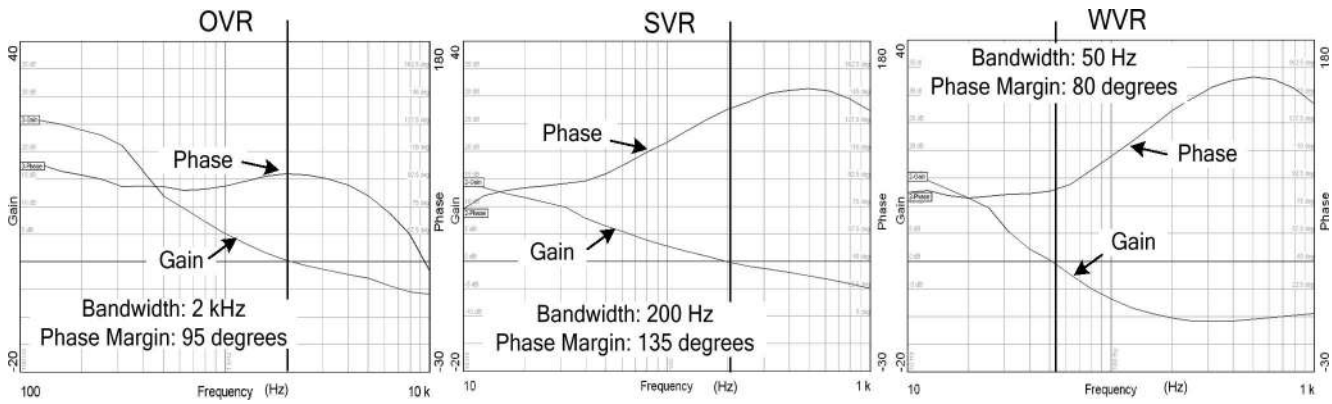

Fig. 13. Bode plots testing results for OVR, SVR, and WVR, respectively. OVR bandwidth is set to be ten times of that of SVR, and SVR bandwidth is four times of that of WVR.

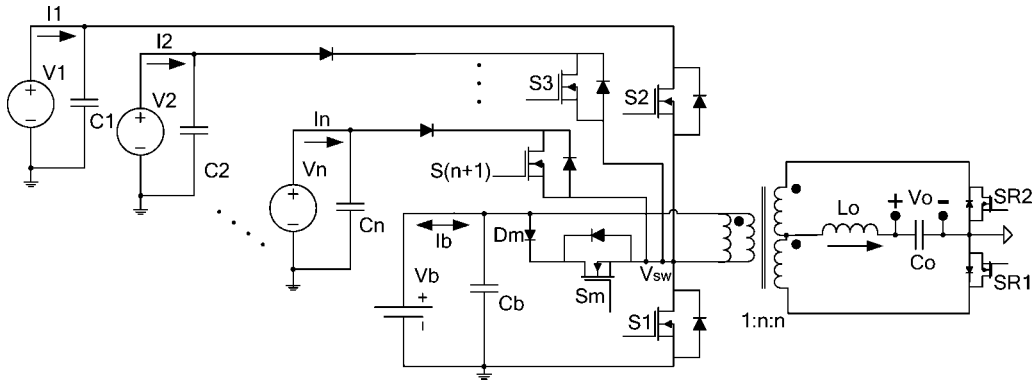

Fig. 14. Extension of the proposed multiport dc/dc converter.

these experiments provide a quick approximation that MPPT of the PV panel and the wind turbine SVR can be achieved at the same time while maintaining a regulated output voltage. In terms of the settling time, the output-voltage transient response is much faster than that of the solar or the wind port, while the transient of the solar port is slightly faster than that of the wind port. Because OVR bandwidth is ten times larger than that of SVR and SVR bandwidth is four times larger than that of WVR. Fig. 13 gives the measured bode plots for these control loops, the loop bandwidth for OVR, SVR, and WVR are 2 kHz, 200 Hz, and 50 Hz, respectively. The controllers take the PID format to ensure sufficient phase margin and guarantee the stable operation of this multiport converter under all load/source conditions. The large phase boost in SVR- and WVR-loop measurement is because the placement of poles is far away from the zeros. The reason for the bandwidth limitation is that the output dynamics is the most stringent of the three, while PV panel and wind turbine dynamics are relatively slower. The aforementioned control-loop bandwidth limitation is helpful to reduce the loop interactions.

V. Extension of the Topology

In the proposed four-port dc/dc converter, there are two input switch branches, which enable two sources. However, the number of the unidirectional switch branches is not limited. Addition of a half-bridge upper switch plus a diode will provide one more input port to interface another renewable energy source. Fig. 14 is a generalized multiport dc/dc converter with n input ports, one bidirectional port, and one isolated output port.

VI. Conclusion

This paper has presented a novel dc/dc converter topology capable of interfacing four dc power ports: two input source ports, a bidirectional storage port, and a galvanically isolated loading port. The converter features low component count and ZVS operation for all primary switches. Modification based on the traditional half-bridge topology makes it convenient for the practicing engineers to follow the power stage design. Three degrees of freedom necessary to control power flow in the system are provided by a four-stage constant-frequency switching sequence.

This four-port converter is suitable for renewable energy systems, where the energy storage is required while allowing tight load regulation. It is suitable for low-power applications since based on the half-bridge topology, while the multiport converter based on the full-bridge topology maybe suitable for high-power applications. For the hybrid PV wind system, the proposed control structure is able to achieve maximum power harvesting for PV and/or wind power sources, meanwhile maintaining a regulated output voltage. The close-loop controller design is investigated based on the dynamic modeling of the converter power stage. Proper decoupling method is introduced to help

design close-loop compensators for such a cross-coupled control system. The circuit operation of this converter and its control system is experimentally verified. Although the proposed four-port converter only has two input ports, it can be extended to have n input ports.

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Zhijun Qian (S'09) was born in Jiangsu, China. He received the B.S. and M.S. degrees in electrical engineering both from Zhejiang University, Hangzhou, China, in 2005 and 2007, respectively, and the Ph.D. degree in the area of power electronics from the University of Central Florida, Orlando, FL, in 2010.

He did internship with Advanced Power Electronics Corporation, Orlando, FL, from 2007 to 2010. He is currently working for Linear Technology Corporation, Milpitas, CA. His research interests include renewable energy conversion such as photovoltaic and wind power harvesting, DC/DC conversion, DC/AC inversion, AC/DC rectification and related digital control.

Osama Abdel-Rahman (S'07–M'08) received the B.S. degree in electronics engineering from Princess Sumaya University for Technology, Amman, Jordan, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the University of Central Florida, Orlando, 2005 and 2007, respectively.

He is a currently a Vice President of engineering in the Advance Power Electronics Corporation, Orlando, FL, where he is involved in conducting leading edge research and development in the areas of power electronics and control for a variety of applications, including renewable energy and solar power, battery charging, space power management, and other applications. He has a vast academic and practical knowledge of electronics, power management, power conversion topologies, magnetic design, and control theory.

Issa Batarseh (S'84–M'85–SM'91–F'06) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Illinois, Chicago, in 1983, 1985, and 1990, respectively.

From 1989 to 1990, he was a Visiting Assistant Professor at Purdue University. In 1991, he joined Electrical and Computer Engineering Department, University of Central Florida, Orlando, where he is currently the Director of the School of Electrical Engineering and Computer Science and Florida Power Electronics Center. He is also a Professor of electrical engineering. He is the author of *Power Electronic Circuits* (New York: Wiley, 2003). He has authored or coauthored nearly 50 refereed journals and 150 conference papers. He holds 13 U.S. patents. His research interests include power electronics, primarily developing high-frequency dc–dc soft-switching semiconductor power converters to improve power density, efficiency, and performance.

Dr. Batarseh is a Registered Professional Engineer in Florida.