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An Integrated Passive Phase-Shift Keying Modulator for Biomedical Implants With Power Telemetry Over a Single Inductive Link

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***Abstract*—This paper presents a passive phase-shift keying (PPSK) modulator for uplink data transmission for biomedical implants with simultaneous power and data transmission over a single 13.56 MHz inductive link. The PPSK modulator provides a data rate up to 1.35 Mbps with a modulation index between 3% and 38% for a variation of the coupling coefficient between 0.05 and 0.26. This modulation scheme is particularly suited for biomedical implants that have high power demand and low coupling coefficients. The PPSK modulator operates in conjunction with on-off-keying downlink communication. The same inductive link is used to provide up to 100 mW of power to a multi-channel stimulator. The majority of the system on the implant side was implemented as an application specific integrated circuit (ASIC), fabricated in 0.6-μm high voltage CMOS technology. The theory of PPSK modulation, simulated and measured performance evaluation, and comparison with other state-of-the-art impedance modulation techniques is presented. The measured bit error rate around critical coupling at 1.35 Mbps is below 6×10^{-8}.**

***Index Terms*—Application specific integrated circuit (ASIC), implantable device, inductive link, passive phase-shift keying (PPSK), power and data telemetry.**

I. Introduction

INDUCTIVELY powered implantable neural stimulators, such as cochlear implants [1], visual prostheses [2]–[5], spinal cord stimulators [6], [7], deep brain stimulators [8] and vestibular prostheses [9]–[12], are often equipped with back telemetry, over which the device operational parameters, such as electrode voltage, power supply level, humidity and temperature, are reported to external controllers for optimising power transfer and monitoring implant safety. In some applications, back telemetry is also used to record neural activities and transmit the digitised readings to an external processor, where the data can be analysed and integrated into neural modulation algorithms for closed-loop stimulation control [1], [12]–[14].

Transmission of multi-channel neural recording data from an inductively powered implant is technically challenging. On one hand, a wide bandwidth is preferable to allow high resolution real-time recording; on the other hand, the implementation must take account of the tight restriction on the physical size and power consumption. Active transmitters provide wide bandwidth at the cost of extra components such as RF antenna and power consumption [15]–[17]. The alternative of passive impedance modulation has been widely used because of its circuit simplicity and power efficiency [18]–[31]. However, a trade-off exists in impedance modulation between the modulation index, data rate and power transfer efficiency. The coil size constraints for biomedical implants result in small coupling coefficients over the inductive link. In addition, some implantable devices such as neurostimulators demand high power resulting in small load impedance. Small coupling coefficients and load impedance limit the modulation index that can be achieved. As a consequence, the working range of the coil separation and data rate are also limited. Changing the load impedance for a longer period of time allows more time for the voltage on the receiver side to settle and hence increases the modulation index. However, this would slow down the data transmission and inevitably disturb the power transfer hence reduce the power transfer efficiency. One approach to address this trade-off is to use separate power and data links. Data rates in the region of megabit per second (Mbps) have been achieved [24]–[27] at the expense of larger device size and circuit complexity. Other approaches include using a series secondary ohmic configuration for a larger dynamic range of impedance modulation to increase the modulation index [21], or carefully choosing the timing of modulation to achieve a high data rate [23], [28]–[30].

In the presented design a passive phase-shift keying (PPSK) modulation scheme, reported in [29], has been developed. PPSK modulation uses superficially similar circuits to the conventional load impedance modulation, but imposes precise control on the timing of modulation to generate a fast transient response over the inductive link with a relatively high amplitude change. This modulation scheme is particularly suitable for biomedical implants that require a high uplink bandwidth but

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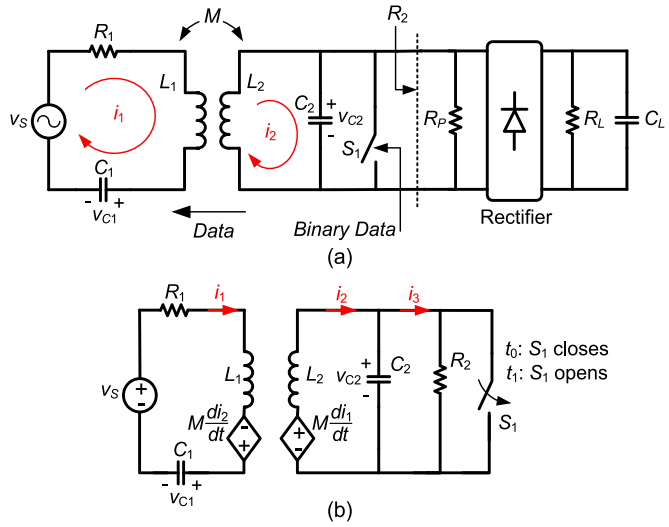

Fig. 1. Modeling PPSK modulation. (a) Simplified circuit model of an inductive link with PPSK modulation. (b) Equivalent circuit model of the inductive link.

have small coupling coefficients and low load impedances. A high modulation index can be achieved without sacrificing the data rate. By reducing the duration of the impedance change the disturbance on power transfer is also minimized. The PPSK modulator was designed for use in an integrated stimulator for a vestibular prosthesis [12] (which describes the multi-channel stimulators and the recording unit). It specifies a minimum data rate of 600 kbps and up to 100 mW of power for device operation.

The focus of this paper is the telemetry design. A preliminary presentation of the PPSK modulator was reported in [28]. This paper presents in detail the theoretical principles of PPSK modulation, performance evaluation and comparison with other state-of-the-art impedance modulation techniques. Included are further circuit details of the application specific integrated circuit (ASIC), comprehensive measured results including modulation index, bit error rate, an improved data rate (up to 1.35 Mbps over a 13.56 MHz inductive link), gain factor and efficiency of the power transfer.

The rest of the paper is organized as follows. Section II presents the theory of PPSK and evaluates its performance in simulation. Section III describes the implementation of the integrated PPSK modulator and the corresponding demodulator in the external transmitter. Section IV presents the implementation of the inductive link and the external transmitter. In Section V the operation of the inductive link is demonstrated with measured results. Concluding remarks are drawn in Section VI.

II. Theory of PPSK

A. Principle of Modulation

The principle of PPSK modulation [30] can be explained with reference to Fig. 1. Fig. 1(a) shows a simplified circuit model of an inductive link for PPSK modulation. In this model, L_1 and L_2 are the inductively coupled primary and secondary coils, respectively, with a mutual inductance M, where $M = k\sqrt{L_1 L_2}$ and k is the coupling coefficient between the two coils. During inductive powering, L_1 is tuned with C_1 and L_2 with C_2 at the carrier frequency. R_1 is the total serial loss resistance on the primary side, including the serial loss resistance of the primary coil and the loss resistance from the driver, v_S. R_P is the parallel loss resistance of the secondary coil and R_L is the total equivalent load resistance from the circuits driven by the secondary coil. The total load resistance seen by L_2 can be represented as R_2, where $R_2 = R_P \| (R_L/2)$. A switch, S_1, connects both ends of L_2 for PPSK modulation. For every binary bit "1," S_1 closes to short L_2 before it opens after a short time interval. This action creates a transient current surge in the primary loop, which can be detected by sensing the voltage peak on C_1.

An equivalent circuit model of Fig. 1(a) is shown in Fig. 1(b). Assume during operation, both $L_1 - C_1$ and $L_2 - C_2$ resonate at the carrier frequency ω_o, generated by the driver v_S, a sinusoidal signal with unity peak amplitude. v_S, and the current in the primary and secondary loops, i_1 and i_2, are

$$\begin{cases} v_S = \sin \omega_o t \\ i_1 = I_{1,\text{peak}} \sin \omega_o t \\ i_2 = I_{2,\text{peak}} \sin\left(\omega_o t + \frac{\pi}{2}\right). \end{cases} \tag{1}$$

At resonance, i_1 is in phase with v_S and lags i_2 by $\pi/2$, and also i_1 leads v_{C1} by $\pi/2$ and i_2 leads v_{C2} by $\pi/2$. Therefore, at a specific time instant t_0, where $\omega_o t_0 = 0$, signals v_S, i_1, and v_{C2} are crossing zero towards the positive phase, while i_2 is at its positive peak, $I_{2,\text{peak}}$, with a phase of $\pi/2$ and v_{C1} is at its negative peak with a phase of $-\pi/2$. Similarly, at a specific time instant t_1, where $\omega_o t_1 = \pi$, signals v_S, i_1, and v_{C2} are crossing zero again but towards the negative values, while i_2 is at its negative peak, $-I_{2,\text{peak}}$, with a phase of $-\pi/2$ and v_{C1} is at its positive peak.

If the switch S_1 closes at t_0 to short L_2 for half a carrier cycle, i_2 is held at $I_{2,\text{peak}}$ during this period (given the on resistance of S_1 is small). S_1 is then opened after half a carrier cycle, i.e., at time instant t_1. At this instant, both v_S and i_1 are still crossing zero towards the negative phase and v_{C1} is still at its positive peak, but i_2 is now forced to be at the positive peak instead of the negative peak in the steady-state. Denoting $i_{2,\text{steady}}(t_1) = -I_{2,\text{peak}}$ as the steady-state i_2, then $i_2(t_1) = i_{2,\text{steady}}(t_1) + 2I_{2,\text{peak}}$. It can be regarded as injecting a transient current of $i_{2,\text{transient}}(t_1) = 2I_{2,\text{peak}}$ into the secondary loop that has been running in the steady-state. The energy of the injected current contributes to a transient current surge in the primary loop. The loop response to the transient current superimposes itself onto the steady-state response, resulting in a transient voltage increase on top of the peak value of v_{C1}. Using the circuit model in Fig. 1(b), the Kirchhoff equations of the transient response at t_1 are

$$\begin{cases} R_1 i_1 + L_1 \frac{di_1}{dt} + \frac{1}{C_1}\int i_1 dt - M\frac{di_2}{dt} = 0 \\ L_2 \frac{di_2}{dt} + \frac{1}{C_2}\int (i_2 - i_3) dt - M\frac{di_1}{dt} = 0 \\ \frac{1}{C_2}\int (i_3 - i_2) dt + R_2 i_3 = 0 \end{cases} \tag{2}$$

where i_1, i_2, and i_3 are all transient currents as a result of injecting $i_{2,\text{transient}}(t_1) = 2I_{2,\text{peak}}$, but "transient" has been removed in the subscripts for simplicity. These transient currents are superimposed on the steady-state currents. Applying

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TABLE I
PARAMETERS OF THE INDUCTIVE LINK

Carrier frequency	13.56 MHz
Primary coil	0.5 mm diameter copper wire, 2 turn solenoid, 25 mm diameter
L_1	0.21 µH
C_1	656 pF
R_S	0.15 Ω
Secondary coil	0.315 mm diameter copper wire, 8 turn solenoid, 16 mm diameter
L_2	1.55 µH
C_2	88.9 pF
R_P	15.340 kΩ

Laplace transform to (2) with the initial condition of $i_2(t_1) = 2I_{2,\text{peak}}$ at t_1, yields

$$\begin{cases} \left(R_1+sL_1+\frac{1}{sC_1}\right) I_1(s)-sMI_2(s)+2I_{2,\text{peak}}=0 \\ sL_2I_2(s)-2I_{2,\text{peak}}+\frac{1}{sC_2}\left(I_2(s)-I_3(s)\right)-sMI_1(s)=0 \\ \frac{1}{sC_2}\left(I_3(s)-I_2(s)\right)+R_2I_3(s)=0 \end{cases} \quad (3)$$

where s is the Laplace operator. From (3), rearranging $I_1(s)$ as a function of $I_{1,\text{peak}}$ results in a Laplace transform with a quartic denominator

$$I_1(s) = \frac{-s\frac{2k^2\omega_o^2\sqrt{1+Q_2^2}}{1-k^2}I_{1,\text{peak}}}{s^4+s^3\frac{\omega_o\left(\frac{1}{Q_1}+\frac{1}{Q_2}-\frac{k^2}{Q_2}\right)}{1-k^2}+s^2\frac{\omega_o^2\left(2+\frac{1}{Q_1Q_2}\right)}{1-k^2}+s\frac{\omega_o^3\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)}{1-k^2}+\frac{\omega_o^4}{1-k^2}} \quad (4)$$

where $Q_1 = \omega_o L_1/R_1$, $Q_2 = R_2C_2\omega_o$, and $I_{1,\text{peak}} = I_{2,\text{peak}}/(k\sqrt{C_1/C_2}\sqrt{1+Q_2^2})$. Applying inverse Laplace transform, the i_1 natural transient can be expressed as

$$i_1(t) = 2|r'|e^{-\alpha' t}\cos(\omega' t+\theta')+2|r''|e^{-\alpha'' t}\cos(\omega'' t+\theta''). \quad (5)$$

$i_1(t)$ is a pair of damped cosine waves. When $k^2 \ll 1$, the interaction between the primary and secondary sides are minor, α' and α'' are the damping factors of the primary and secondary circuits, respectively, where $\alpha' \approx R_1/2L_1$ and $\alpha'' \approx 1/2R_2C_2$; ω' and ω'' are the damped frequencies on the primary and secondary respectively, where $\omega' \approx \sqrt{\omega_o^2-(\alpha')^2}$ and $\omega'' \approx \sqrt{\omega_o^2-(\alpha'')^2}$. For $k^2 \ll 1$, $\omega' \approx \omega'' \approx \omega_o$. As k increases, the interaction between the primary and secondary circuits varies the values of α', α'', ω', ω'', r' and r'', resulting in changes of the peak value and the rate of increase and decay of the envelope of $i_1(t)$.

By way of example the link parameters in Table I are specified for a vestibular prosthesis [12]. They were derived following the design procedure in Section IV.A. To evaluate $i_1(t)$ in (5) numerical analysis was conducted in Matlab with the parameters in Table I. Fig. 2 shows the variation of the parameters α, ω, r, and θ of (5) with k. There is a distinct change in parameter variation as k approaches $k_{\text{crit}}(= 0.107)$. There is always a 180° phase difference between θ' and θ''. As a result, the composite waveform of $i_1(t)$ always has an envelope increasing to a peak and then decaying. Fig. 3 shows the resultant transient waveforms for different values of k. For large values of k, $\alpha' \approx \alpha''$ and $|r'| \approx |r''|$, and an additional low frequency $(\omega' - \omega'')$ sinewave multiplying factor develops and causes ringing.

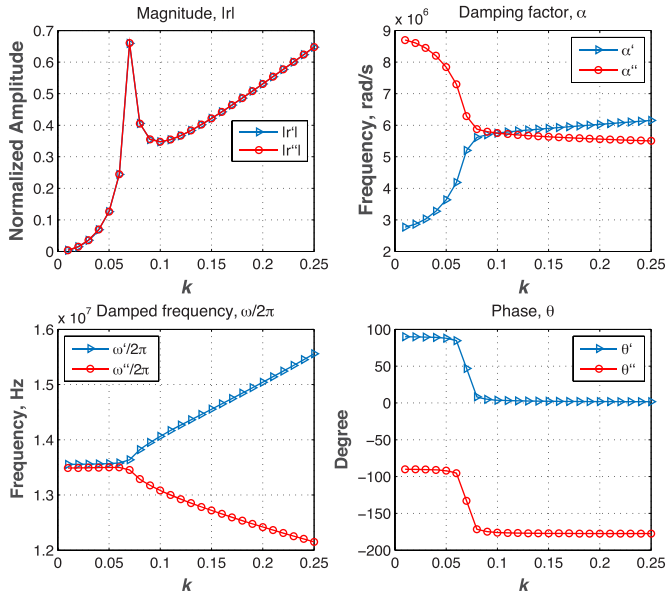

Fig. 2. Variation of the parameters of the i_1 natural transient in (5) versus coupling coefficient k using the parameters in Table I.

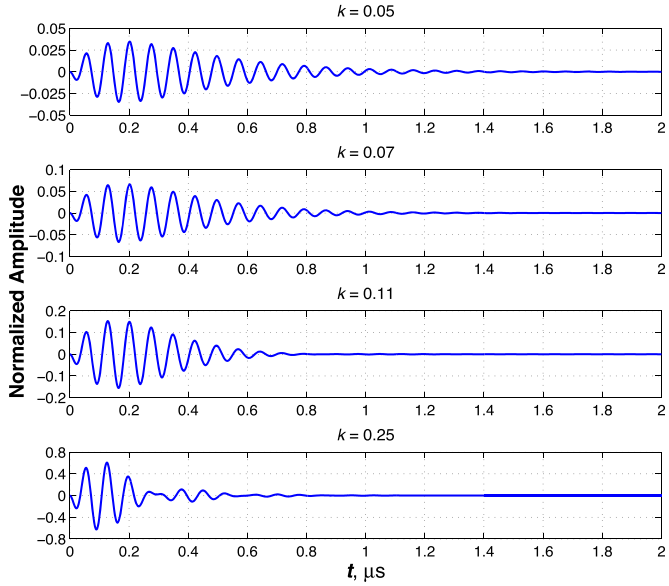

Fig. 3. Transient waveforms of the i_1 natural transient for different values of the coupling coefficient k with reference to the results in Fig. 2.

B. Evaluation With ADS Simulation Model

To evaluate the performance of PPSK modulation, a simulation model based on the circuit model in Fig. 1(a) was created in Keysight Advanced Design System (ADS) v2015.01. The coupling coefficient was calculated from the coil geometry [32] using the parameters in Table I. PPSK modulation is implemented by switching on S_1, to short the secondary coil L_2. The variables in the simulations are the coupling coefficient k, the equivalent load resistance R_2 on the secondary coil, and the time instants at which S_1 is closed and released. For the vestibular prosthesis application, the required working range of coil separation is 5–15 mm, corresponding to calculated coupling coefficients between 0.169 and 0.048.

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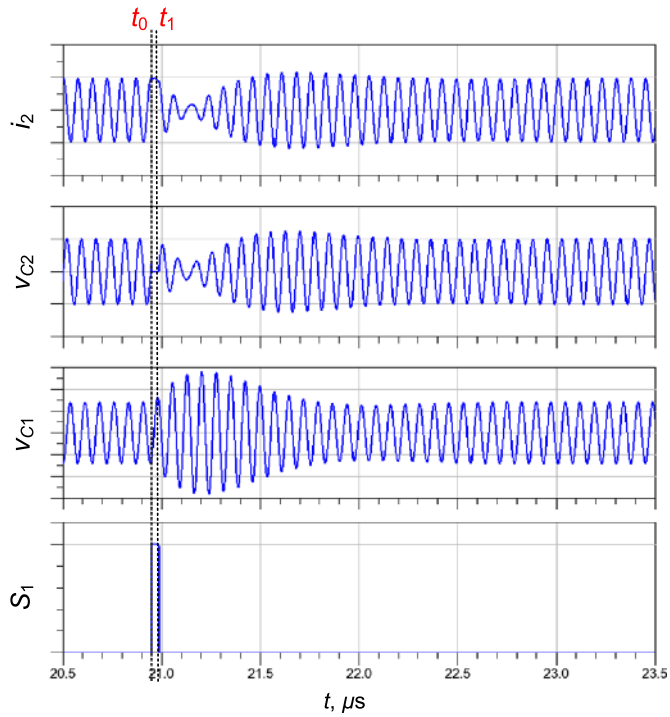

Fig. 4. Transient responses of the voltages and current in the operation of PPSK modulation. The dotted lines indicate the time instants when the secondary coil is shorted and released.

1) Transient Response: Fig. 4 shows the transient change on i_2, v_{C1}, and v_{C2} when S_1 is closed at the instant i_2 is at its positive peak and is then released after half a carrier cycle. k is set to 0.08 corresponding to 10.5 mm coil separation (this distance is in the middle of the expected working range of coil separation for a vestibular implant design). As shown in Fig. 4, a clear transient voltage surge can be seen on v_{C1}. The rise and fall of the voltage surge shows a pattern of summation of two damped cosine waves. v_{C1} returns to its steady-state level approximately 10 carrier cycles after S_1 is closed. This gives a data rate of 1.35 Mbps over a carrier frequency of 13.56 MHz.

2) Comparison With Other Load Modulation Schemes: The analysis in Section II.A shows that S_1 should ideally close at t_0 and open at t_1. Any timing offset from these two critical time instants will result in a lower i_1 transient and hence, lower modulation index. This is because the equivalent extra current injected into the secondary coil is at its maximum, $2I_{2,\text{peak}}$, when S_1 is on for half a carrier cycle, i.e., $\omega_o t_1 = \pi$. When S_1 remains closed for longer, $\omega_o t_2 > \pi$, where t_2 is the new time instant when S_1 opens, the new phase of the original i_2 is not opposite to the stored i_2 at $\pi/2$, and thus the equivalent extra injected current is lowered. The performance of PPSK was compared with two other load modulation schemes: the ISO/IEC 14443-Type B phase-shift keying (BPSK) load modulation scheme [33] (termed as BPSK-LSK below), and the cyclic on-off keying (COOK) scheme described in [23]. For all three schemes, the carrier frequency was set to 13.56 MHz and the data rate to 847.5 kbps. The onset of load modulation was set to the positive zero-crossing point of v_{C2}, at which point S_1 was turned on to short the secondary coil, for all the three schemes. S_1 remained on for half a carrier cycle for PPSK, one carrier cycle for COOK and eight carrier cycles for BPSK-LSK. The modulation repeated every sixteen carrier cycles. The equivalent load resistance, R_2, was set to 644 Ω for all the three schemes. This value was derived from the measured R_L (1344 Ω) in parallel with the measured R_P (15.34 kΩ) of the secondary coil.

Fig. 5(a) compares the modulation index of different modulation schemes. The modulation index on the primary coil is compared over the targeted working range of coil separation. The modulation index is defined as $m = (A - B)/(A + B)$, where A and B are the peak voltage and steady-state voltage of v_{C1}, respectively. The results show that the BPSK-LSK scheme provides the highest modulation index among the three schemes, while COOK gives the lowest. PPSK produces a modulation index close to that of BPSK-LSK when $k < 0.08$. Fig. 5(b) shows the influence of these three schemes on power transfer with reference to the power transfer link efficiency when no modulation is applied to the link. In contrast to the relative performance of the modulation index, COOK has the minimum disturbance on the power transfer, while BPSK-LSK reduces the link efficiency significantly. PPSK has a link efficiency slightly lower than that of COOK. Comparing the modulation index performance in Fig. 3(a), BPSK-LSK achieves the highest modulation index by having the longest duration of modulation. As a result it causes the most reduction in the power transfer. PPSK shorts the secondary coil for only half a carrier cycle. It achieves a modulation index higher than COOK by momentarily reversing the phase of LC resonance on the secondary side, and subsequently injecting extra current into the primary side. However, this phase reversal of LC resonance causes more energy loss than COOK, despite the fact that its modulation duration is shorter. Fig. 5(c) shows the minimum time required for the carrier to recover after single bit modulation with PPSK and COOK. The recovery time for both schemes increases as the coupling coefficients decreases. At strong coupling, a high data rate can be achieved as shown in [23].

The modulation strategy for specific applications can be chosen from the simulated performance. BPSK-LSK would be favourable for its highest modulation index in applications that only require occasional uplink communication with a low volume of data to transmit, such as RFID. The reduction in link efficiency from occasional disturbance on power transfer will not be significant. On the other hand, at strong coupling, COOK has the advantage of providing a high data rate with high link efficiency and acceptable modulation index. For biomedical implants with low coupling and a demand for constant uplink communication at high speed, as well as high power demand (e.g., vestibular prosthesis), PPSK is the optimal choice. At low coupling, it provides a modulation index much higher than COOK and comparable to BPSK-LSK, while it is much more power efficient than BPSK-LSK and close to COOK.

Fig. 5(d) plots the simulated modulation index against the timing error of the onset and length of the switch closure duration for PPSK modulation. The timing error is presented as the percentage of a carrier period. The modulation index is simulated with a k of 0.08 and R_2 of 2 kΩ. The highest modulation index of 0.32 occurs when both the onset and length error are zero. The results suggest a tolerance of -15% to 10% for the length error, and -10% to 5% for the onset error within which the modulation index remains above 90% of the peak value.

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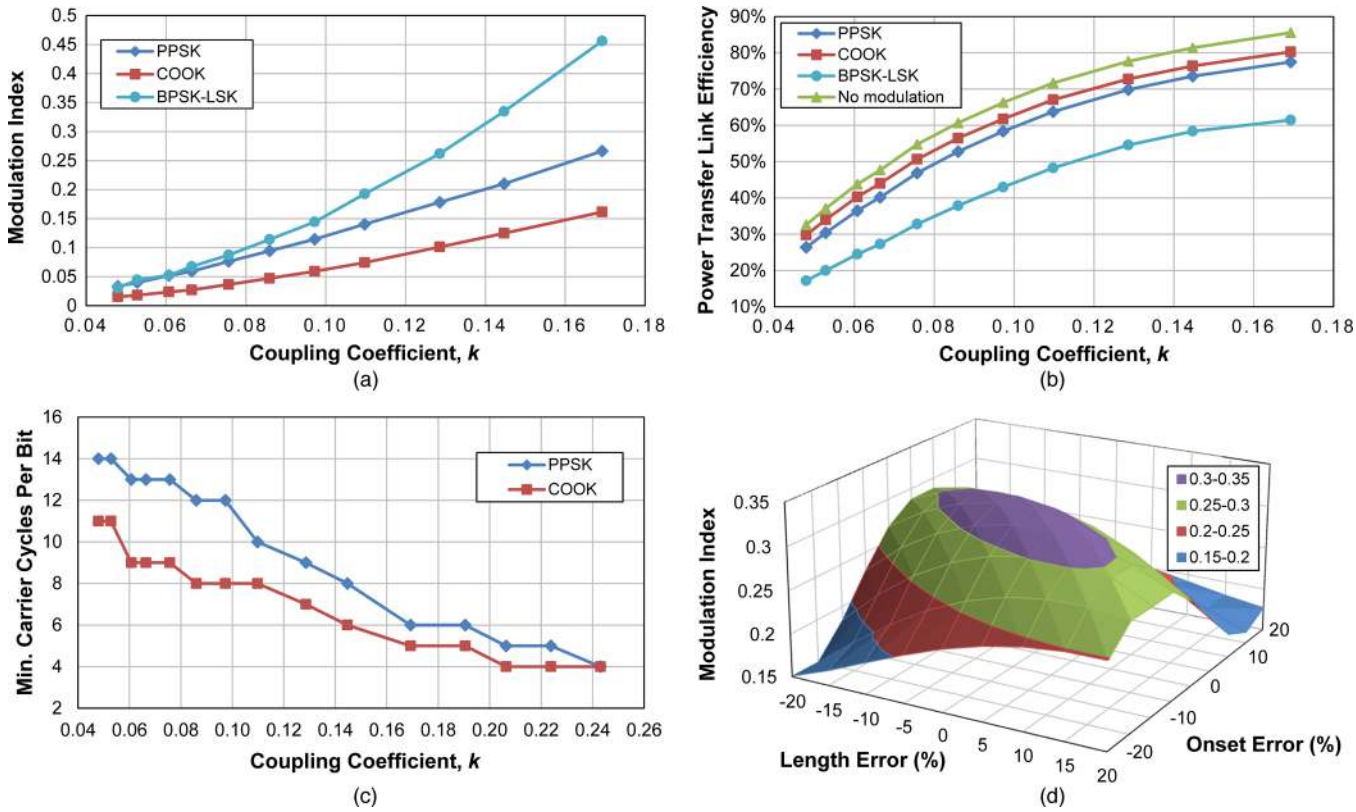

Fig. 5. Simulated performance of PPSK with comparison to COOK and BPSK-LSK, with a R_2 of 644 Ω, data rate of 847.5 kbps and carrier frequency of 13.56 MHz. (a) Simulated modulation index at different coupling coefficients. (b) Simulated power transfer link efficiency at different coupling coefficients. (c) Simulated minimum number of carrier cycles per bit of PPSK and COOK for different coupling coefficients. (d) Simulated modulation index of PPSK with regard to timing offset of both the start and duration of the switch closure.

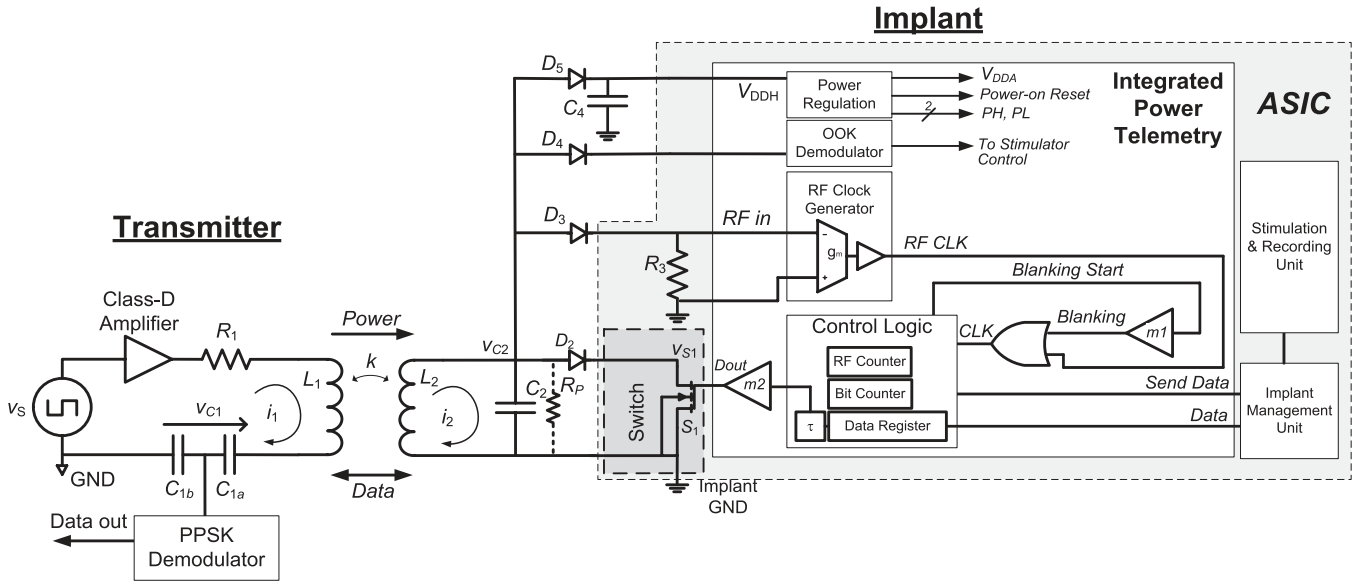

Fig. 6. System architecture of the power telemetry with PPSK modulation. The integrated components are in the area labeled ASIC.

III. Implementation of the Telemetry

A. System Overview

A power telemetry with an integrated PPSK modulator was implemented as part of an implantable stimulator for vestibular prosthesis (requiring up to 100 mW power delivery and 600 kbps uplink data communication [12]). The system architecture is shown in Fig. 6 with emphasis on the power and data telemetry. Power transfer is via the inductive link with its tuning network, including L_1, C_{1a}, C_{1b} on the primary side and L_2, C_2 on the secondary side. The tuning network is adjusted to the carrier frequency of 13.56 MHz. Downlink data transmission uses on-off keying (OOK) while uplink employs PPSK. The implant subsystem was integrated in an ASIC as highlighted

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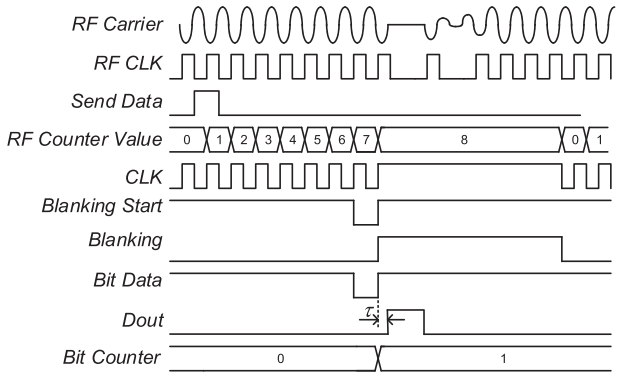

Fig. 7. Timing sequence of the control logic.

in Fig. 6. Diodes $D_2 - D_5$ are glass case Schottky diodes and C_4 is a 10 μF tantalum capacitor. The ASIC includes a power regulator providing a stable high voltage, $V_{\rm DDH}$, of 12 V for the stimulator output stage and a stable low voltage, $V_{\rm DDA}$, of 5 V for the rest of system, comprising a PPSK modulator, an OOK demodulator, an implant management unit and a stimulation and recording unit. Details of the management unit and stimulation and recording circuits were presented in [11], [12]. The carrier is generated by a class-D power amplifier in the external transmitter. The voltage developed in the resonant tank $L_2 - C_2$ is rectified by a half-wave rectifier, $D_5 - C_4$, for the power regulator. The signal on the secondary coil is connected to the OOK demodulator and the PPSK modulator.

B. PPSK Operation

The PPSK modulation is managed by a control logic that operates on a clock extracted from the carrier by the RF clock generator. The control logic contains a shift register for the data, two counters and a delay block. The shift register streams out data received from the implant management unit at a speed defined by the RF counter. The timing sequence of the modulation control is shown in Fig. 7. A *Send Data* signal from the implant management unit triggers the modulation procedure in which the RF counter starts counting the *RF CLK* pulses generated from the *RF Carrier*. At the overflow value of the counter (7 in Fig. 7 for a bit rate of 847.5 kbps), if the current bit is logic "1," a *Bit Data* pulse is generated to trigger the monostable $m2$ to generate a pulse on *Dout*. This pulse turns on switch S_1 for PPSK modulation. S_1 was implemented by a high voltage NMOS transistor with dimensions $W/L = 1995$ μm/1.3 μm, yielding an on resistance of 17 Ω.

Since the received carrier disappears for a few cycles when modulation occurs due to shorting the secondary coil, *RF CLK* becomes momentarily irregular during modulation, as shown in Fig. 7. To maintain regularity and constant timing between bits, a blanking mechanism was implemented. After the *RF Counter Value* reaches its overflow value, a *Blanking Start* pulse is generated to trigger the monostable $m1$, which generates a blanking pulse of about 570–590 ns, sufficiently longer than the required time for the carrier to recover. This pulse blanks the clock to the control logic from *RF CLK*, keeping *CLK* static until *RF CLK* returns to regular action. The data rate is programmable by setting the overflow value of the RF counter. This value is set by the external transmitter during system initialisation. Once the counter exceeds this value, it resets and starts the next modulation period, where the shift register streams out the next bit and the bit counter increments by 1. The overall period for each bit is the sum of the length of the blanking pulse and the number of carrier cycles set by the overflow value.

As discussed in Section II, the timing of switching on and off S_1 is critical for achieving the maximum modulation index. A delay cell, τ, was inserted at the input of S_1 to align the switch onset. The length of the delay is a sum of the delay from the monostable $m2$, the control logic and the RF clock generator. Its value was derived from Monte-Carlo simulation to ensure the onset error is within 10% of one period of the carrier. In addition, $m2$ is made programmable so that the length of the S_1 pulse can be fine-tuned to reduce the length error.

C. Monostable

The circuit implementation and operation of the two monostable units ($m1$ and $m2$, Fig. 6) are shown in Fig. 8. Fig. 8(a) shows the overall architecture of the monostable. In operation, a rising edge at the input *IN* switches the output *OUT* to "1" and turns on the current source I_C to charge the capacitor C. When the voltage on C reaches a high threshold value, $V_{\rm hi}$, the D-flip flop is reset. As a result, its output Q becomes "0" and I_C is turned off and the current sink, I_D is switched on to discharge C. Once the voltage on C drops to $V_{\rm low}$, *OUT* is switched back to "0." The circuit stays in this state until the next pulse on *IN* arrives. The width of the output pulse on *OUT* is decided by the charging and discharging current value, the capacitance of C and the threshold values of $V_{\rm hi}$ and $V_{\rm low}$. $V_{\rm hi}$ and $V_{\rm low}$ are the threshold voltages of inverter "*hi*" and "*low*" in Fig. 8(a), respectively. The charging time, t_c, and the discharging time, t_d, are

$$t_c = \frac{CV_{\rm hi}}{I_C} \tag{6}$$

$$t_d = \frac{C(V_{\rm hi} - V_{\rm low})}{I_D}. \tag{7}$$

The threshold voltage of a simple CMOS inverter is [34]

$$V_{\rm th} = \frac{V_{{\rm th}N}\sqrt{\frac{\beta_N}{\beta_P}} + V_{\rm DDA} - V_{{\rm th}P}}{1 + \sqrt{\frac{\beta_N}{\beta_P}}} \tag{8}$$

where β_N/β_P is the transconductance ratio of the NMOS and PMOS transistors; $V_{{\rm th}N}$ and $V_{{\rm th}P}$ are the threshold voltages.

The current source and sink of $m2$ are programmable as shown in Fig. 8(c). I_C is mirrored with transistors M15, M25, M27, M28, M36, and M37 to generate a fixed current of 136 μA. I_D consists of two parts: a fixed current $I_{\rm base}$ of 80 μA mirrored with M15, M19, M22, and M24, and a tuning current $I_{\rm control}$. $I_{\rm control}$ is eight times the programmable current $I_{\rm program}$ generated from $M_1 - M_{14}$. The variation range of $I_{\rm control}$ is between 0 μA and 60 μA with a step size of 4 μA. $I_{\rm control}$ is programmed by the digital values of $A0$, $A1$, $A2$, and $A3$ that are set by the external transmitter. Charging and discharging are controlled by signal Qn that turns on or off of the transistor switches M21, M23, M33, and M38.

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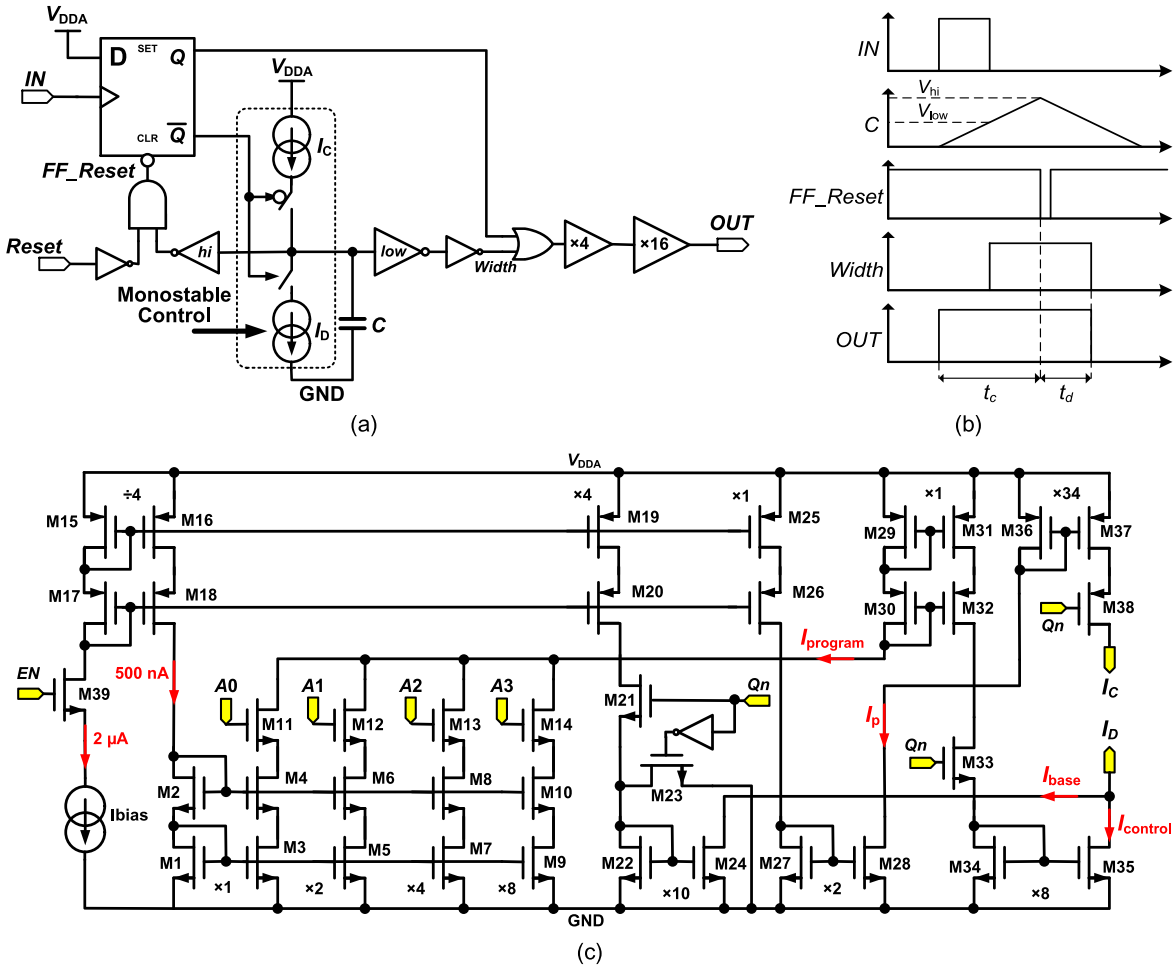

Fig. 8. Programmable monostable implementation. (a) Monostable schematic. (b) Operation of the monostable. (c) Programmable current source.

The value of the capacitor C in $m2$ is 1.68 pF (included in the ASIC). The transistor dimensions of the inverters are: for "*high*," PMOS $W/L = 4\ \mu$m$/10\ \mu$m and NMOS $W/L = 1\ \mu$m$/10\ \mu$m; for "*low*," PMOS $W/L = 3\ \mu$m$/10\ \mu$m and NMOS $W/L = 5\ \mu$m$/10\ \mu$m. The duration of the $m2$ output pulse (OUT) is between 107 ns and 116.3 ns with a step size of 0.62 ns. This is suitable for matching 1.5 cycles of the 13.56 MHz carrier. The choice of 1.5 cycles instead of 0.5 cycle is to allow a larger C so that the effect of the process variation is reduced. A switch closure of 1.5 carrier cycles generates the same PPSK modulation performance because the switch release time is still at the opposite phase of the switch closure onset, while the current loss in the secondary loop during switch closure is low given the high parallel loss resistance of the coil and the low on resistance of the switch.

The implementation of the monostable $m1$ is the same architecture as that in Fig. 8(a) but with $I_C = 40\ \mu$A, $I_D = 48\ \mu$A and $C = 5.73$ pF (included in the ASIC).

D. RF Clock Generator

To extract the carrier frequency from the RF signal in the digital domain a level shifting circuit was implemented as shown in Fig. 9. The differential amplifier generates a pulse when the carrier amplitude is above 0 V. This results in a square wave at the output of the differential amplifier. The following inverters generate a square wave compatible digital signal to serve as the clock for the PPSK control logic.

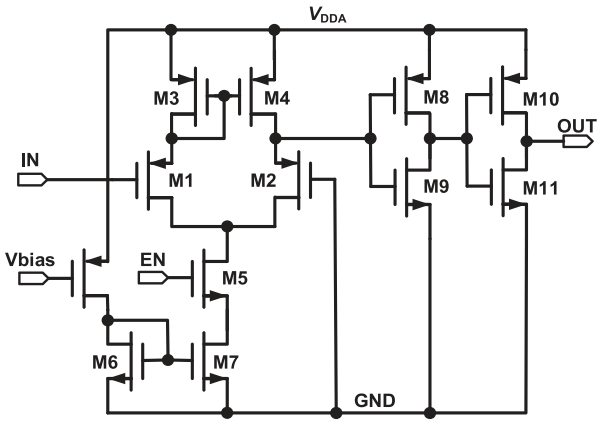

Fig. 9. RF clock generator.

E. OOK Demodulator

The implant receives control settings from the external transmitter via the inductive link using OOK modulation with a data rate of 400 kbps. The circuit of the OOK envelope detector to extract the signal from the modulated carrier is shown in Fig. 10. As the recovery time of the carrier varies with the load and coupling coefficient, the time constant of the RC_d peak

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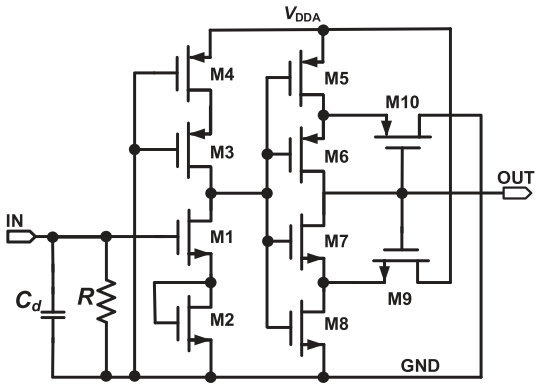

Fig. 10. Implementation of the OOK demodulator.

detector should be set to a larger value than the worst case rise time of the carrier. The implemented R is 44.9 kΩ and C_d is 2.8 pF. Transistors M5–M10 form a Schmitt trigger to generate a digital output from the peak detector.

F. Power Regulator

The power regulator module includes a voltage monitoring unit, a voltage regulator and a power-on reset. The voltage monitoring unit reports to the external transmitter when the received voltage is too high or too low (by respectively setting *PH* and *PL*; see Fig. 6) and the driving voltage V_{driver} on the class-D amplifier (see Fig. 11) is adjusted accordingly. The voltage regulator generates a stable 5 V supply for the implant electronics. The voltage regulator and the power-on reset are implemented in standard circuit architecture as described in [34].

IV. External Transmitter and Communication Protocol

A. Link Design

The diameter of the secondary coil and the coil separation are mainly defined by the surgical constraints. In the example of the vestibular application, the layout of the implant is similar to commercial cochlear implants [35], where the secondary coil locates alongside a hermetically sealed hybrid. Both the coil and hybrid are encapsulated with medical grade silicone rubber. The diameter of the secondary coil L_2 was set to 16 mm. The working range of the coil separation takes into account the thickness of the skin behind the ear where the device will be implanted, and the thickness of the secondary coil after encapsulation. It is set between 5 mm and 15 mm, while the gain factor of the power transfer peaks around 7–10 mm. To accommodate misalignment due to relative movement between the coils on implantation, the diameter of the primary coil L_1 was set to 25 mm to ensure 100% overlap.

The gain factor of the power transfer (refer to Fig. 1) can be expressed as [36]

$$A_G = \frac{|v_{C2}|}{|v_S|} = \frac{\sqrt{\frac{R_2}{R_1}}}{\left(\frac{k_c}{k} + \frac{k}{k_c}\right)} \tag{9}$$

where k_c is the critical coupling coefficient

$$k_c = \sqrt{\frac{C_1 R_1}{C_2 R_2}}. \tag{10}$$

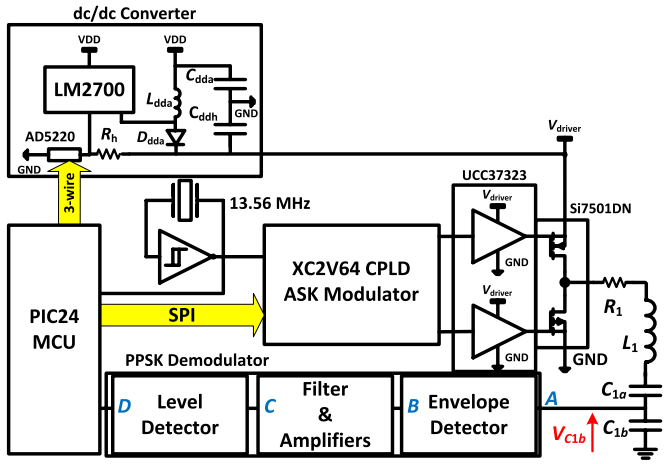

Fig. 11. Architecture of the external transmitter.

Equation (9) indicates that A_G peaks when $k_c = k$. Therefore, the values for C_1, C_2, R_1, and R_2 are bounded by (9) so that $k_c = k$ at 8 mm coil separation. Among the variables, R_1 is a combination of the primary coil serial loss resistance and the loss resistance of the power amplifier and $R_2 = R_P \| (R_L/2)$. For this design, R_1 is 1.15 Ω, while the load resistance of the implant, R_L, is about 1344 Ω from measurements. The carrier frequency is 13.56 MHz. Based on the values of R_1, R_2, the geometry of the coils and the carrier frequency, L_1 and L_2 were chosen to satisfy $k_c = k$ at 8 mm coil separation, where the value of k was derived using the procedure in [30]. The link parameters are listed in Table I. According to these parameters, k is between 0.048 and 0.169, and k_c is 0.107 at 8 mm coil separation.

B. External Transmitter

The architecture of the external transmitter is shown in Fig. 11. A class-D power amplifier was constructed with the primary LC tank driven by a pair of power switches built with two complementary power MOSFETs, Si7501DN, and a dual MOSFET driver UCC37323. A XC2V64 CPLD (complex programmable logic device) operates the power switches at a switching frequency of 13.56 MHz. A microcontroller (MCU) controls the power transfer level by adjusting the supply voltage of the class-D amplifier. According to the feedback voltage measurement from the implant, the MCU programs a digital potentiometer, AD5220, in the dc/dc converter that supplies the class-D amplifier. The MCU also generates control settings for the implant. These settings are sent via SPI (serial peripheral interface) to the CPLD, where they are packed into frames with cyclic redundancy check (CRC) code generated and attached. The CPLD also shifts the frames into a bit-stream and performs OOK modulation on each bit. The modulation is implemented by switching on or off the driving signal to the power switches at 400 kbps. Logic "1" switches off the carrier while logic "0" keeps the carrier unchanged.

The uplink data stream is demodulated in the PPSK demodulator. A simple capacitive voltage divider, C_{1a} and C_{1b}, scales down the modulated carrier in the primary LC tank to the dynamic input range of the amplifiers in the filtering and

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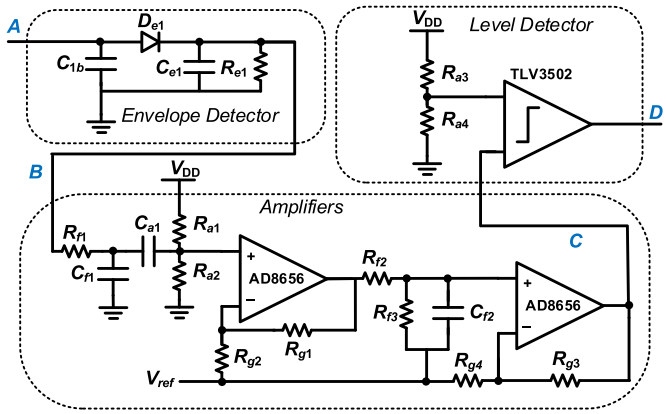

Fig. 12. Schematic of the PPSK demodulator.

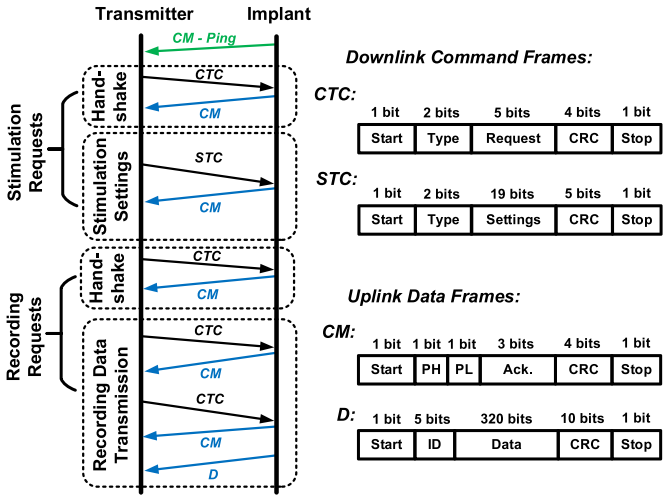

Fig. 13. Communication protocol and the frame structures.

amplifying stage. The ratio between capacitors C_{1a} and C_{1b} is 1 : 8.57. The voltage on C_{1b} is applied to the PPSK demodulator, which comprises an envelope detector, a filter and amplifier stage and a level detector. The circuit details of the three stages are shown in Fig. 12. The envelope detector extracts the voltage transient on C_{1b} from the input. The time constant of the $R_{e1} - C_{e1}$ network was set to be higher than the carrier period (73.7 ns) but lower than a single bit width ($>$ 740 ns). A RC low pass filter $(R_{f1} - C_{f1})$ with a cut-off frequency of 2 MHz attenuates the carrier frequency components from the output of the envelope detector. The ac components in the filtered signal are applied to a two-stage amplifier with a dc bias at the mid-supply range. The two-stage amplifier consists of two AD8656 op-amps and a low-pass filter between the two amplifiers. The amplified signal is translated into a digital bit-stream by a level detector implemented with a comparator TLV3502.

C. Communication Protocol

The external transmitter and the implant communicate over the inductive link following a half-duplex protocol shown in Fig. 13. There are two types of downlink frame, *CTC* and *STC*, and two types of uplink frame, *CM* and D. All frames begin with a logic "1" as *Start* and end with a logic "0" as *Stop*, so that the RF carrier remains intact when there is no communication.

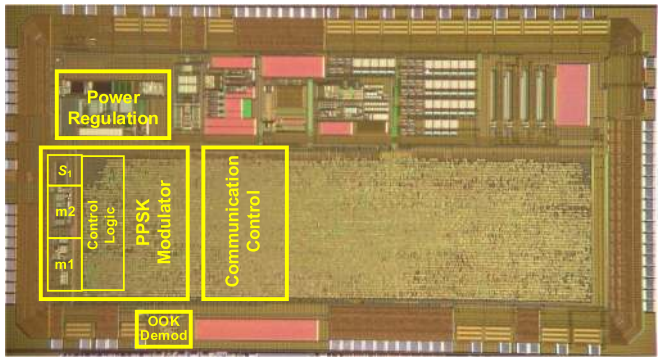

Fig. 14. ASIC microphotograph with the building blocks of the telemetry highlighted.

When the implant is powered up, it sends *CM* frames to the transmitter repetitively every 250 μs as *Ping* signals until the transmitter responds. The procedure for stimulation, recording and housekeeping requests consists of two stages. The transmitter firstly sends a *CTC* frame for handshake. The *Request* section in the frame defines the request. The implant completes the handshake with a *CM* frame as acknowledgement. The transmitter then sends a *STC* frame with the settings for the request, such as the pulse profile and channel for stimulation or recording window length and channel selection. Details of the stimulation and recording settings are described in [12]. The housekeeping request includes settings for the PPSK data rate control and programmable monostable. The settings can be sent over multiple *STC* frames. The implant acknowledges each *STC* frame with a *CM* frame. The *Ack.* section in the *CM* frame informs the transmitter whether the *STC* frame was correctly received or not. For a recording request, the transmitter repeatedly sends *CTC* frames to check if the 320-bit buffer in the implant, corresponding to a 1.6 ms neural recording window length, has been filled up with recorded data. The implant reports the buffer status in the *Ack.* section of the *CM* frames. Once the buffer is full, the implant starts transmitting data in a D frame. All the frames contain CRC for error detection at the receiving end. The length of CRC depends on the length of a frame. Each *CM* frame also contains two power bits, *PH* and *PL*, for reporting whether or not the received voltage is too high or too low, so that the transmitter can adjust the power transfer accordingly.

V. Measured Results

The ASIC was implemented in 0.6-μm high voltage CMOS technology. Fig. 14 shows the die microphotograph with the building blocks of the telemetry highlighted. Table II lists features and measured performance. For the measurements, the external transmitter and the implant electronics were mounted on two separate printed circuit boards (PCBs). The implant electronics includes the ASIC shown in Fig. 14, the auxiliary discrete components for the telemetry ($D_2 - D_5$, C_2, and C_4 shown in Fig. 6), and resistors used as equivalent electrode load impedances [12]. The primary and secondary coils as specified in Table I were connected closely to the two PCBs. The two coils were mounted onto two parallel panels in a coaxial position. The distance between the two coils was adjusted by moving one panel along the axis.

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TABLE II
SUMMARY OF FEATURES AND PERORMANCE

Technology	X-FAB 0.6-µm HV CMOS
Die size	ASIC: 21.42 mm^2 (including the telemetry, implant management, stimulation and recording circuits)
Supply voltage	5 V (digital circuits, PPSK modulator, OOK demodulator, recording unit) 12 V (stimulator output stage)
Telemetry	
Carrier frequency	13.56 MHz
Working distance	5 – 15 mm
Uplink modulation	PPSK
Uplink data rate	Up to 1.35 Mbps
Uplink BER	$< 1.01 \times 10^{-6}$ at 847.5 kbps $< 1 \times 10^{-5}$ at 1.35 Mbps
Downlink modulation	OOK
Downlink data rate	400 kbps
Power transfer	Up to 100 mW
Power transfer link efficiency	66.4% without PPSK, 60.64% with PPSK**

**With continuous PPSK at 1.35 Mbps for coil separation of 8 mm.

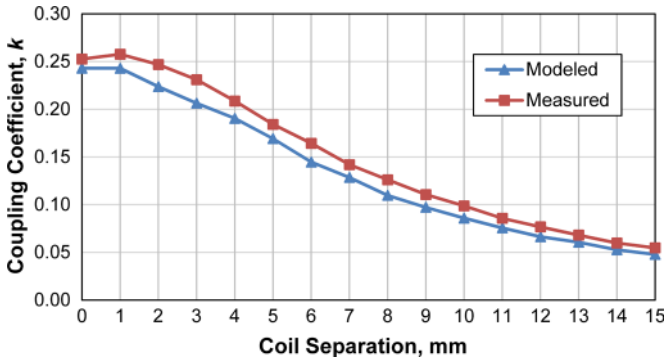

Fig. 15. Modeled and measured coupling coefficient for different coil separations.

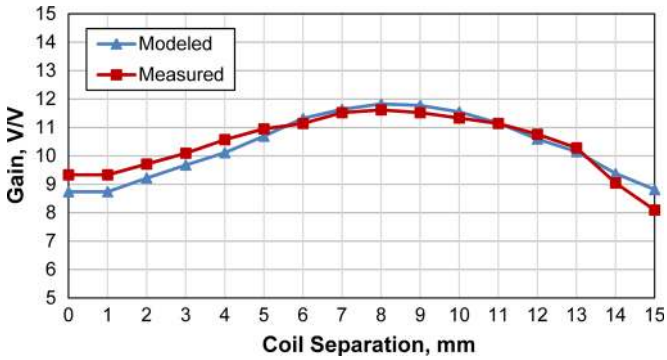

Fig. 16. Modeled and measured gain factor for different coil separations.

A. Power Transfer

The coupling coefficients at different coil separations were calculated from measured mutual inductance and compared to those modeled shown in Fig. 15. The modeled coupling coefficients in the figure were derived from the coil geometry using the procedure in [32]. Fig. 16 shows the gain factor against coil separation of the inductive link driving the vestibular prosthesis with $R_L = 1344\ \Omega$. The measured gain factor matches the result derived from (9) using the modeled coupling coefficients. The gain factor peaks around 8 mm coil separation, agreeing with the calculated critical coupling position.

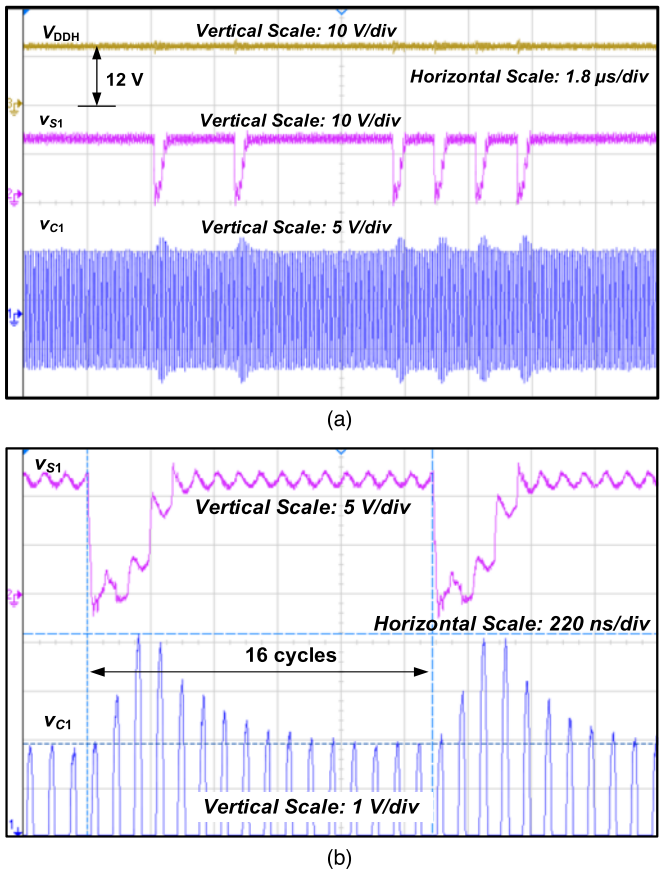

Fig. 17. (a) Oscilloscope screenshot of the transmission of a CM packet with PPSK modulation at a coil separation of 7 mm. (b) Zoomed in view of two consecutive bits of "1."

B. PPSK Modulation and Demodulation

Fig. 17 shows the performance of the PPSK modulator with the vestibular implant sending a *CM* frame over the inductive link. The coil separation was 7 mm, corresponding to a measured k of around 0.14. A *CM* frame with an 11-bit sequence (10100011110) was transferred over the inductive link. In Fig. 17(a), the top trace is the power regulator output V_{DDH} that supplies the implant. V_{DDH} is a stable dc voltage of 12 V. The middle trace is the voltage v_{S1} recorded at the drain of the switch S_1, as shown in Fig. 6. S_1 is shorted at every logic "1" bit for 1.5 carrier cycles. As a result, a transient voltage surge on v_{C1} can clearly be seen in the bottom trace in Fig. 17(a). Fig. 17(b) shows a zoom-in view of v_{S1} and v_{C1} when two consecutive logic "1" bits are transmitted. Switching of S_1 causes a transient voltage surge on v_{C1} that lasts for nine carrier cycles before it returns to the steady-state. In order to allow sufficient settling time over the entire working range of 5–15 mm for the coil separation, each bit of the uplink data lasts for sixteen carrier cycles before transmitting the next bit. This corresponds to data rates up to 847.5 kbps.

The measurement was repeated with different coil separations, and the recorded modulation index is shown in Fig. 18 alongside the simulated modulation index from ADS with $R_2 = 644\ \Omega$. As shown, the measured values approximately agree with the simulation, decreasing with the increase of the coil separation.

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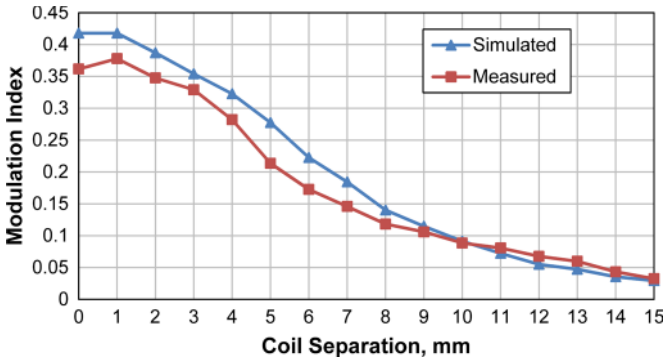

Fig. 18. Simulated and measured variation in modulation index for different coil separations.

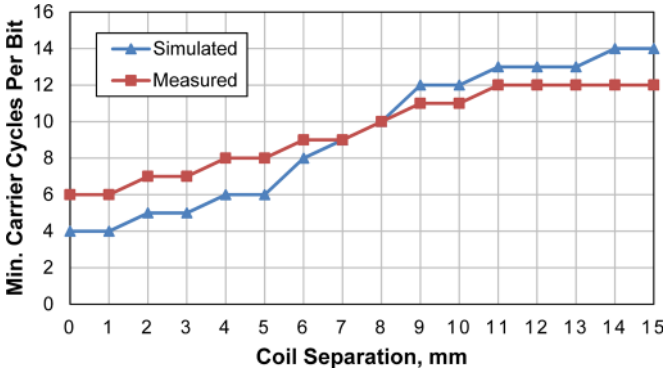

Fig. 19. Simulated and measured minimum number of carrier cycles needed to transmit one bit, for different coil separations.

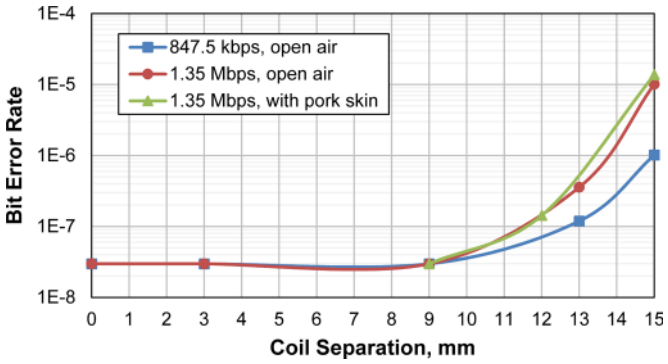

Fig. 20. Measured BER for data rates of 847.5 kbps and 1.35 Mbps.

The minimum numbers of carrier cycles per bit were also recorded in these measurements and are plotted in Fig. 19 alongside the simulated values. It is shown that the chosen data rate of 16 carrier cycles per bit is enough for the specified working range of coil separation, but there is potential for a higher data rate, especially for small coil separations.

Bit error rate (BER) was measured with the PPSK modulator configured to continuously transmit a pseudorandom bit-stream generated from a 24-bit linear feedback shift register. For each measurement, 16.78 Mbits were collected from the PPSK demodulator and erroneous bits were counted to obtain the BER. The BER was measured with $R_L = 1344\ \Omega$, similar to the simulations. The measured BERs over a coil separation range between 0 mm and 15 mm at data rates of 847.5 kbps and 1.35 Mbps in open air, are shown in Fig. 20. Over the working

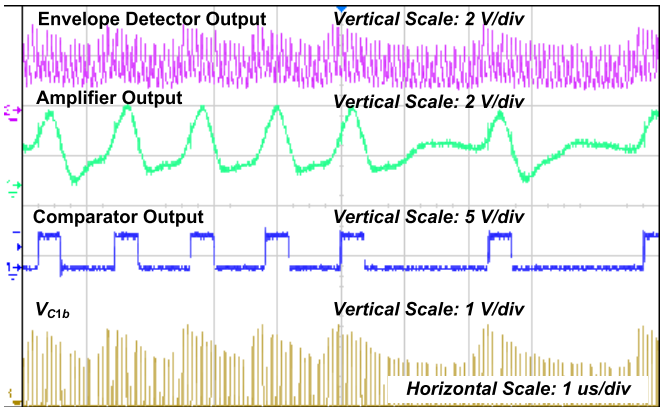

Fig. 21. Oscilloscope screenshot of signals in the PPSK demodulation stages.

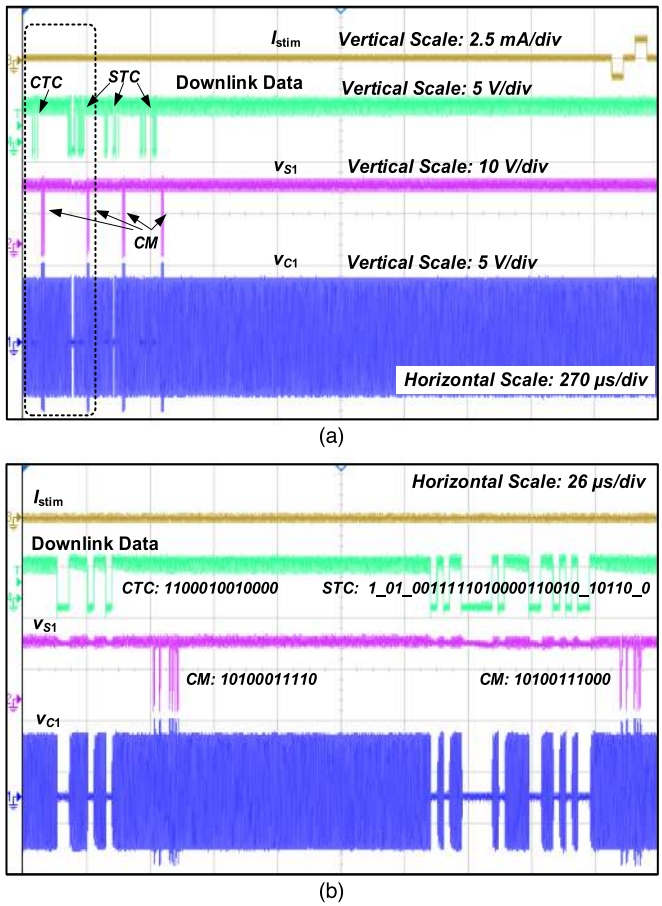

Fig. 22. Oscilloscope screenshot of telemetry operation for a handshake between the transmitter and the receiver.

range of 5 mm to 15 mm coil separation, the BER at 847.5 kbps is below 1.01×10^{-6} and the BER at 1.35 Mbps is below 1×10^{-5}. To examine the effect of skin/tissue on the PPSK modulation the BER at 1.35 Mbps was measured with a pork skin sample (of thickness 3–4 mm) attached to the secondary coil. The measured BER with the pork skin is also plotted in Fig. 20. The results show that the BER is only very slightly downgraded at long coil separations.

Fig. 21 shows the waveforms in the PPSK demodulation stages for extracting a 9-bit sequence (111110101). The captured waveforms are: the input to the envelope detector (V_{C1b}), the

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TABLE III
COMPARISON WITH OTHER SINGLE-INDUCTIVE-LINK DESIGNS

Reference	Carrier frequency (MHz)	Downlink		Uplink			Coupling coefficient in the specified coil separation	Power delivered to the load (mW)
		Modulation	Data rate (kbps)	Modulation	Data rate (Mbps)	BER		
[19]	10	BPSK	1120	LSK	n./a.	n./a.	0.07	≥ 0.61
[20]	1	-	-	LSK	0.003	$<1.6\times10^{-6}$ (PER)	$0.08-0.17$	≤ 250
[21]	13.56	-	-	LSK	0.5	n./a.	0.03*	20
[22]	13.56	BPSK	1690	LSK	0.1	n./a.	$0.04-0.12$*	22.5
[23]	13.56	-	-	COOK	6.78	$<6\times10^{-7}$	≥ 0.34*	≤ 6.3
This work	13.56	OOK	400	PPSK	1.35	5.98×10^{-8}**	$0.055-0.184$	≤ 100

*Estimated using equations (1)-(7) in [32] from the coil parameters given in the references. The coupling coefficients of [22] and [23] were estimated for both coaxial solenoid single-layer coil and planar spiral coil scenarios. In the latter the maximum spacing between two adjacent turns in the coil was set to D_{MAX}/N, where D_{MAX} is the radius of the outermost turn, and N is the total number of turns.
**BER at the critical coupling where the coil separation is 8 mm. The BER over the full working range of coil separation is shown in Fig. 20.

output from the envelope detector, the output from the second amplifier, and the output digital bit-stream from the comparator. The probe positions capturing these waveforms are labeled in Fig. 11 as A, B, C, and D, respectively.

C. Bi-Directional Communication

Fig. 22 shows the recorded procedure of initiating biphasic stimulating pulses with the bi-directional communication over the inductive link as illustrated in Fig. 13. Fig. 22(a) shows four downlink data packets were sent to the implant using OOK, among which are one *CTC* packet for selecting the semi-circular canal and three *STC* packets for setting the stimulation. The implant responds to each packet with a *CM* packet using PPSK modulation. After the communication the stimulator starts generating biphasic current pulses (I_{stim}), as shown in the top trace in Fig. 22(a). Fig. 22(b) shows a zoom-in view of the enclosed area in Fig. 22(a), which includes the *CTC* packet, the first *STC* packet and their corresponding *CM* packets. The OOK and PPSK modulations are clearly visible in the trace of v_{C1}.

D. Comparison With State-of-the-Art

A comparison of performance of the implemented power and data telemetry with other work is shown in Table III. This comparison is specific to designs that use a single inductive link for both power transfer and data communication, where the performance of the data link is limited by the implementation of the power link. PPSK modulation provides high load power and has a high data rate at low coupling with a good BER.

VI. CONCLUSION

This paper has presented a telemetry system with simultaneous power delivery and bi-directional data transmission over a single pair of inductively coupled coils. The telemetry has been used to operate efficiently a vestibular prosthesis which requires both a high data rate and high power. An integrated PPSK modulator has been implemented in 0.6-μm high voltage CMOS technology. A fast data rate of 1.35 Mbps has been achieved for the uplink over the same pair of coils at a carrier frequency of 13.56 MHz to transmit out neural recording data. The performance of the PPSK modulator and its dependence on the inductive link parameters have been investigated and verified.

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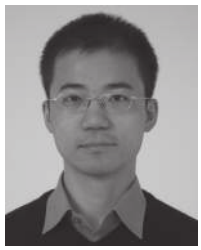

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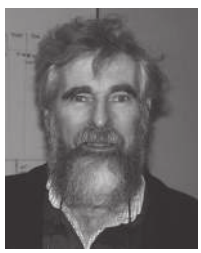

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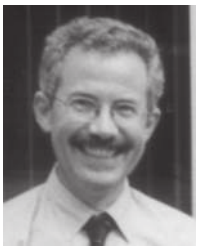

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