An Interconnect-Aware Methodology for Analog and Mixed Signal Design, Based on High Bandwidth (Over 40 GHz) On-chip Transmission Line Approach

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Abstract

This paper presents an on-chip, interconnect-aware methodology for high-speed analog and mixed signal (AMS) design which enables early incorporation of on-chip transmission line (T-line) components into AMS design flow. The proposed solution is based on a set of parameterized T-line structures, which include single and two coupled microstrip lines with optional side shielding, accompanied by compact true transient models. The models account for frequency dependent skin and proximity effects, while maintaining passivity requirements due to their pure RLC nature. The signal bandwidth supported by the models covers a range from DC to 100 GHz. The models are currently verified in terms of S-parameter data against hardware (up to 40 GHz) and against EM solver (up to 100 GHz). This methodology has already been used for several designs implemented in SiGe (Silicon-Germanium) BiCMOS technology.

1 Introduction

The recently introduced SiGe BiCMOS technology ($f_T \approx 100GHz$) ([18], [6]) enables a tremendous increase in on-chip signal bandwidth in the areas of analog and mixed signal (AMS) design. Consequently, new design challenges have risen. In multi-GHz design regimes, on-chip interconnect has a major impact on an integrated circuit (IC) performance and has to be adequately factored in the frame of the design process. A traditional post-layout treatment of on-chip interconnects may lead to either numerous design iterations and consequently to longer time-to-market, or to a significant amount of over-design. This is particularly true in SiGe designs where the frequencies are in the order of tens of gigahertz, and post-layout only consideration of interconnect would probably lead to a re-design. IC design in the high speed AMS domain is featured by a frequent need for true-transient time-domain simulations, high importance of signal integrity, and characteristic bandwidths in the microwave region. In addition to that, the typical layout is relatively sparse, there is no well-defined 50Ω environment and the design flow is basically serial (layout after schematic). Due to these characteristics, there is a need for on-chip interconnect-aware AMS design flow, which incorporates interconnect influence into the standard design procedure and accounts for transmission line phenomena, which abound at such high bandwidths. For the best of our knowledge there is no well-established AMS design flow, which addresses the issues described above in time domain. In this paper we present such an on-chip interconnect-aware design flow which is tuned for high-speed AMS applications. Section 2 of this paper describes the proposed methodology, which is the main focus of the paper. In section 3 we discuss the general approach used for time domain on-chip T-line modeling, Section 4 presents the existing results of the verification of the models, and Section 5 concludes the paper.

2 An Interconnect-Aware Design Methodology

2.1 Design Flow

The interconnect-aware design methodology presented below adheres to the main paradigm of combining the mer-

its of automated design with the designer's wisdom. Good examples of this emerging paradigm are constraint-based approaches, half-automated design reuse and module generators (see, e.g., [3]). The basic idea of the proposed methodology is to *design* the critical interconnect lines from the very beginning rather than just *extract* them at the very end. Critical interconnect lines are therefore identified, modeled and incorporated in the netlist from the early phases of the design flow, and their parameters are updated as the design evolves towards maturity. The primary goal of the proposed methodology is to enable higher predictability of an IC performance by means of incorporating on-chip transmission lines into the simulation using dedicated models, co-designed with the methodology. Based on our design experience and work by others (e.g. [7],[13]), it is assumed that within the AMS domain a designer has to account for transmission line effects for a limited set of signal lines only, further referred as the critical lines set. This approach is similar to the approach of critical parasitics selection [3]. A critical line is designed using a predefined set of allowed interconnect structures. The basic feature of such a structure is that most of the electric field lines and the current return path are contained within the structure boundary. This set is integrated within a design kit for the specific technology used and contains all the relevant technology data, in a consistent manner with the implementation of other library elements. The currently used set of allowed geometries makes use of two metal layers, where the top metal layer carries the signal and the bottom layer serves as a current return path. Future sets can include other geometries as well, where the selection criterion is the cost effectiveness of a structure in terms of performance versus its cost from the layout point of view. The methodology described is therefore not limited to any specific on-chip T-line structure, as long as they comply with the criteria defined in the next sub-section. Figure 1 depicts the proposed interconnect-aware design flow.

As is common in AMS design practice, a designer starts with an architecture and floorplan definitions. During this stage, the critical interconnect lines to be modeled with on-chip T-lines are identified and defined, based on the estimated length and metal level assignment, using the above mentioned set of allowed structures. After a user defines the geometry of a T-line structure, the embedded algorithm calculates the electrical parameters of the line: capacitance, low- and high-frequency inductance, series resistance, and TEM impedance (odd and even impedances for coupled lines) at high frequency limit. These critical lines are usually the longer high-speed lines, which connect the leaf cells of the design. The number of critical lines is therefore usually much lower than the total number of wires in a given design. The choice of critical lines also depends on the signal integrity and timing requirements from a given line, which is highly dependent on the specific application . More specific guidelines for the choice of critical lines can be derived from previous works ([7],[13]) in which the considerations for RC or RLC modeling are presented. It should be mentioned that due to the much higher bandwidth compared with conventional VLSI designs, the lines that have to be modeled using T-line models are much shorter in our case, and may be in the order of few hundred microns. The rest of the wires are extracted and modeled only at the post-layout stage, using standard extraction techniques, which usually do not consider interconnect inductance at all, or consider it very roughly [14]. During the schematic design phase the same T-Line models are used, with possible refinement in their geometry parameters. It may also be possible that additional lines are identified as critical at a later stage of the design, and their corresponding T-line models are added into the simulation model. However, experience shows that in most practical design examples, most of the critical lines can be identified at an early design stage. All the on-chip T-Lines are automatically netlisted and simulated together with other circuit elements (like transistors, resistors etc.) and treated equally throughout the design process. At the physical design phase, all the on-chip T-Lines are passed into the layout view as parameterized cells (p-cells) correct by construction both from DRC and LVS points of view. During the layout phase, the actual lengths of the T-lines may slightly differ from their schematic level designed values and some stretching and bending may be required. Dur-

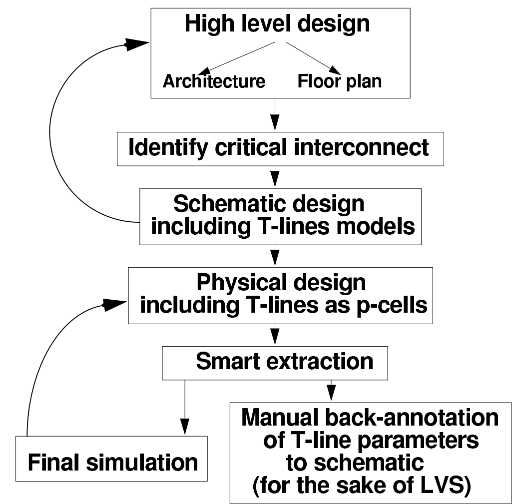

Figure 1. The proposed interconnect-aware design flow

ing the post-layout phase, wires modeled as T-Lines are recognized and treated as other library elements, namely their extracted geometrical parameters are passed into the same model equations for post-layout simulation. The rest of the wires go through a standard extraction procedure, which is faster but less accurate than the special treatment we described above. The complete netlist, combining both the T-line models and the layout-extracted components, is then simulated to complete a bottom-up verification of the design process. A correct choice of critical lines in the schematic phase will make a one-iteration success highly probable.

2.2 Allowed on-chip straight T-Line structures

The methodology introduced above makes use of a predefined parameterized set of T-line geometries with variable dimensions. As mentioned before, the basic requirement from any qualified interconnect geometry is the *closed environment* condition, which means that the majority of electric field lines are closed within the structure cross section and that the T-Line structure contains its own return path, namely the sum of the currents in its cross section is zero. This closed environment condition depends not only on the geometry but also on the proper connectivity of the return path of the T-line in the circuit. This condition implies that both the electric and the magnetic coupling to nearby parallel lines is kept small. The bottom shielding also eliminates the coupling to the conductive silicon substrate. Consequently the cross talk is kept low and the line impedance is well controlled. Currently two types of shielded structures are supported: single wire T-line and two coupled wire T-line, the latter being more suitable for differential designs. All possible metal layer combinations that are supported by the given technology can be used for signal and shielding. Figure 2 presents the generic geometries of the supported types of T-lines.

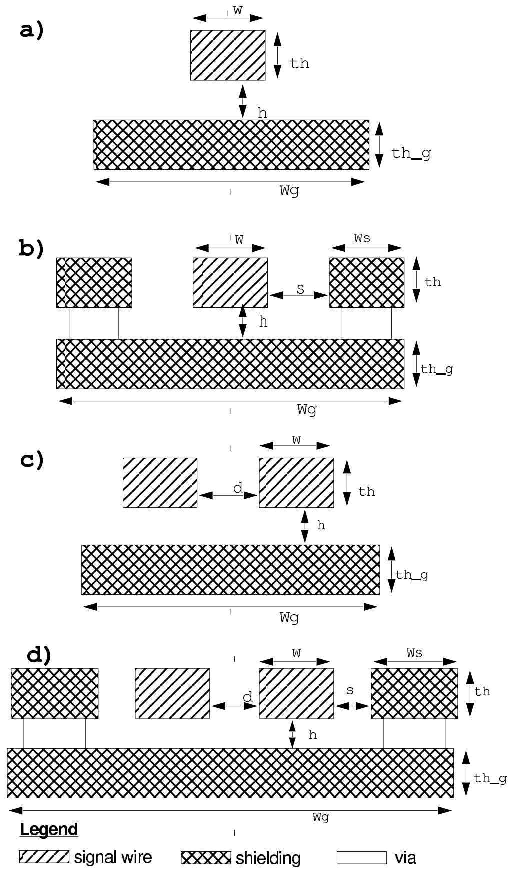

Figure 2. Cross-sections of supported geometries for on-chip T-line implementation: Single (a,b) and two coupled lines (c,d) in a microstrip geometry.

In Figure 2 (a) and (c), the width of the bottom return path layer is larger than the width of the top signal wire(s) structure in order to insure the closed environment condition. This shielding methodology reduces the inductance of the T-line structure, thereby reducing many inductance related signal integrity problems in high-speed IC designs, such as overshoots, ringing noise, and even damped resonances in longer wires. Both types of T-line structures allow side shielding of the signal line, as shown in Figures 2 (b) and (d). In this last case vias are connected between the side shielding and the bottom shielding, ensuring equal potential on the bottom and side shield, since the via-to-via separation is much smaller than the shortest possible on-chip wavelength. As an example, the on-chip wavelength which corresponds to 100 GHz signal is 1500μ, taking the approximation of a homogeneous silicon-oxide dielectric environment, and assuming a relative dielectric constant of 4.1 for

the oxide layer. At the present stage the methodology forbids any metal shape collinear with the on-chip signal wire to be placed in higher metal layers right above it.

3 High Bandwidth Transmission Line Model

Simulation of signal integrity in AMS and digital designs may include both time domain simulations and frequency domain simulations. Modeling of T-Lines is more readily achieved in the frequency domain. In order to allow for time domain analysis, it is therefore common to use frequency domain simulations and translate them to the time domain using either the inverse fast Fourier transform [24] or the inverse Laplace transform [12]. This method requires a periodic time domain excitation and does not allow for true transient simulation, namely having the system in one state and moving in time to another state without repetition. Another problem with this approach is that direct time domain simulations inherently enable large signal simulation with nonlinear components, while frequency domain simulations usually assume small or medium signal models (such as harmonic balance) for the transistors. Large signal simulations are essential in AMS designs which include switching circuits and power stages. Another way to enable time domain simulations of circuits including on-chip T-Lines is to solve Maxwell's equations directly in time domain [19],[21]. This approach requires an electromagnetic field solver to be a built-in part of the design flow, implying various problems of convergence, stability, and time consuming process, even for medium size (several tenths of T-lines) designs.

The approach used in this paper is based on incorporation of on-chip T-line models, based on RLC ladder networks. Unlike many analytical time domain approximations, this approach is inherently passive by construction, and is built to restore the frequency dependence of both the inductance and the resistance over the full bandwidth from DC to the transistor cut-off frequency (100 GHz for SiGe technology). The use of pure RLC networks enables further network reduction using standard techniques, such as AWE [15], CFH [5], or Krylov Subspace [10] on the SPICE generated matrix. The accuracy of the RLC models should be within the expected process variation of line impedance in silicon based metalization, which is usually about 10%. The use of quasi-TEM approach for high bandwidth on-chip T-Line models is justified by the fact that the cross sectional dimensions of the on chip T-Line structures, shown in Figure 2, are few microns at the most, and are very small compared with the shortest on-chip wavelength. In addition to that, the dielectric relaxation time constant in metal is much smaller than the inverse of this required bandwidth. Hence, the T-Line capacitance per unit length is practically frequency independent. On the other hand, the frequency

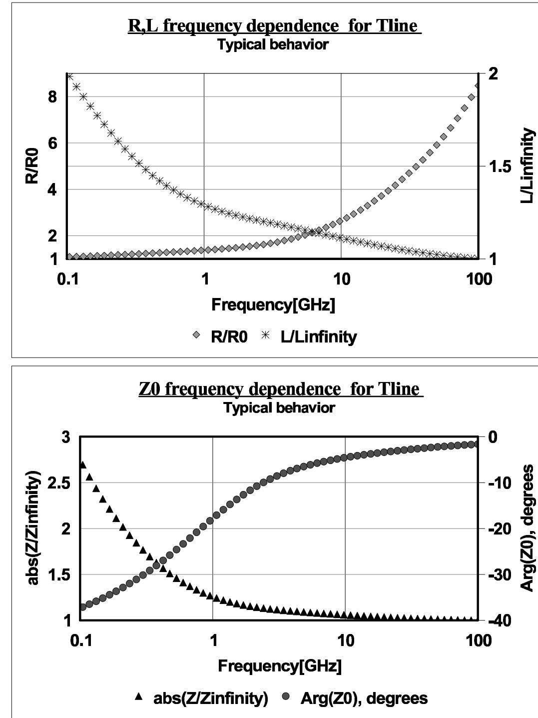

Figure 3. Resistance (*R*), inductance (*L*) and characteristic impedance (Z_0) vs. frequency, based on EM solver

dependence of both inductance and resistance due to the skin effect is very strong as is clearly demonstrated in Figure 3, which shows the frequency dependency of R, L and Z_0 for the measured structure of Figure 4. The strong frequency dependence of the T-line inductance and resistance is consistent with the skin depth values, which can be well below 1μ in the frequency range of interest. A T-line is implemented by a network consisting of several cascaded RLC segments, the number of which is calculated so that there are at least 20 segments per one on-chip wavelength corresponding to the high edge of the required bandwidth.

The large frequency dependent variation of the inductance results from the use of signal metal layers with relatively high thickness (few microns) in order to reduce the losses, and from the fact that in all structures of Figure 2 the separation (h) is of the same order of the thickness (t_h), unlike standard microwave structures on GaAs substrate where the separation is usually determined by the substrate thickness that is much larger than the line thickness. This smaller separation in our cases means that a bigger portion of the inductance is due to the skin-effect dependent internal inductance, compared with the mutual inductance part. The large frequency dependence of the resistance also follows from the relatively large thickness of the signal metal

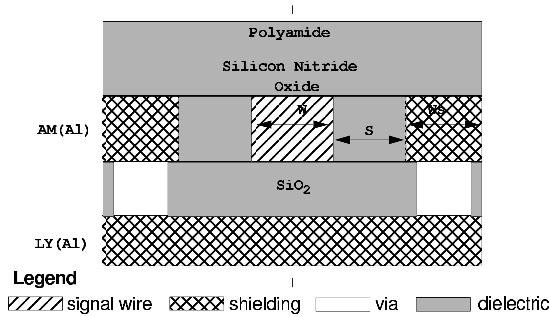

Figure 4. A single line structure used for measurements

layer, compared with the small skin depth at these high frequencies.

Several possible RLC networks which depict this RLC frequency behavior have been proposed in the literature (e.g. [25] [10] [17] [16] [23] [26] [27]) which can be generalized for the case of coupled lines by adding the required cross inductance and cross capacitance components. The method we use for calculating the components of such RLC network is as follows. Each model of a transmission line consists of several RLC segments built from fixed elements, arranged in such a way that the total inductance and resistance are frequency dependent. The calculation of the values of the RLC network components includes several steps, which are given below.

(1) In the first step, the static (low frequency) values of the RLC parameters of the T-Line per unit length are calculated. The static resistance calculation is obvious in rectangular cross sections, unless cheesing holes appear in the copper lines, which requires the development of approximate resistance expressions. Several approaches are reported in the literature for modeling of low frequency line capacitance and inductance in rectangular geometries by expressions (e.g. [2] [4] [8] [11] [22] [28] [29]). As part of this study, closed form, semi-analytical expressions were developed for the specific case of the structures of Figure 2. The models comply with basic electrostatic and magneto-static principles and have correct asymptotic behavior with about 10% error (with respect to EM solver) in the entire geometry parameter range. This level of precision complies with the T-Line impedance variations in a typical silicon process. In addition, a 10% variation in RLC data usually causes insignificant deviations in the time domain simulated waveform shapes.

(2) In the second step of the calculation, the high frequency limit TEM inductance matrix is calculated from the capacitance data (e.g. [11] pp. 115-120), making use of quasi-TEM approximation.

(3) In the third step, these boundary RLC values are used to calculate the actual values in a reduced RLC network, in a way that correctly describes the T-line behavior across the whole frequency range of interest.

The algorithm embedded in each on-chip T-Line component receives the geometry parameters (w, s, d and layer selection as shown in Figure 2) and constructs the equivalent RLC network described above, which is then used by a circuit-level simulator.

The above general approach to interconnect modeling has been applied to numerous design projects in IBM and other companies. The specific details of the T-line models that are currently being used will be published elsewhere.

4 Experimental Verification

A common way for characterization of transmission lines is S-parameter measurement using a Vector Network Analyzer (VNA). Thus, in order to verify our model against measured hardware, the results of the EM solver (Ansoft) simulation and Spectre (Cadence) simulation of on-chip T-line models were expressed in S-parameter formalism. Measurements of single T-line structures were performed using the *8510C* Agilent 40 GHz VNA, standard 40 GHz coaxial cables and 40 GHz *Cascade* Ground-Signal-Ground (GSG) type coplanar probes. An LRRM type calibration was used, followed by on-chip de-embedding (additional on-chip ”open” calibration and Y parameter subtraction). The estimated calibration errors are small: contact resistance lower than 0.1Ω, residual tip inductance lower than $10pH$, residual pad capacitance lower than $5fF$. These numbers are at least an order of magnitude smaller than any measured data. The two coupled line structures require four port S-parameter measurements, which can be directly transformed to even mode and odd mode S-parameter data. These measurements are currently in preparation and will be reported elsewhere.

Electromagnetic simulation of on-chip T-Line structures can be obtained by standard full wave S-parameter solver. 2D calculation is sufficient in our case, since the on-chip T-Line is modeled per unit length, and the end-effects due to the loading are treated by the source and load models in the circuit simulation level. For the reasons presented previously (Section 3) a quasi static EM solver was used for verification. The absolute numerical convergence accuracy was verified by comparing the results of two independent EM

solvers based on two different numerical methods, namely finite element (Ansoft *EM2D*) and boundary element (Ansoft *SI2D*) , to less than 1%. The resulting RLC data was then mathematically converted to 50Ω-based S-parameter data. The models of T-lines under discussion were simulated by means of a standard circuit-level simulator (*Spectre* by *Cadence*) in S-parameter simulation mode.

Figure 5 compares measured results, EM solver and model simulation data for a representative single on-chip T-Line structure with the geometry cross section given in Figure 4 with dimensions of $w = 5.72\mu$, $th = 4\mu$, $s = 147\mu$, $h = 4\mu$ and $th_g = 1.4\mu$, and two lengths: 1020μ and 4010μ, using aluminum-copper metalization. In this structure we get a DC resistance per unit length of $1.25\Omega/mm$, compared with an AC resistance of $8.3\Omega/mm$ at 60 GHz . In this same structure we get a DC (static) inductance per unit length of $0.8nH/mm$ compared with an AC inductance of $0.3nH/mm$ at 60 GHz . The high frequency limit quasi TEM inductance in this geometry is $0.28nH/mm$. The strong frequency dependence of the RLC data of these structures is explained in the previous section. The characteristic impedance of these structures varies from $51 - 16.3j\ \Omega$ at 1 GHz to $45.1 - 3.6j\ \Omega$ at 10 GHz and about 43 Ω at 60 GHz. The results of EM solver based model verification for the two wires T-line structure of figure 2 (c) are presented in Figure 6. As can be seen from Figures 5 and 6, the S-parameters data obtained by the above-described three methods, are in a reasonable agreement. The deviations, however, are mostly due to the errors in the static RLC values, obtained by the semi-analytical expressions used in the model. Hence, a better approximation can be achieved by using more sophisticated expressions for the static RLC values.

Judging by the experience gained so far by several users of the presented interconnect-aware design methodology, it seems that the currently obtained model accuracy is sufficient for most typical AMS designs.

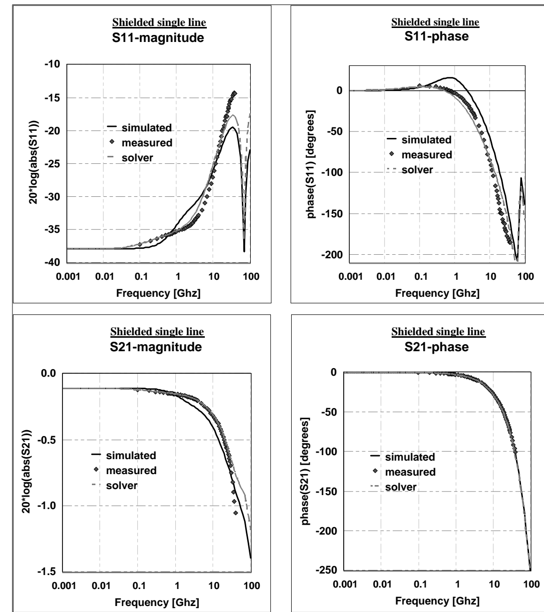

Figure 5. Comparing the model to field-solver and measured hardware for a single line.

5 Conclusions

A novel methodology is suggested that introduces on-chip T-Lines into the standard AMS design flow. This methodology has proved to be a cost effective way to account for interconnect effects during the design process by providing a means for controlling the signal integrity on critical wires in high-speed AMS designs. This suggested methodology is a careful combination of the merits of design automation with designer's wisdom, as well as the merits of microwave and VLSI design methodologies. On-chip T-line models have already been applied to several SiGe design projects inside and outside IBM. Among these projects are: data conversion circuits (ADC and DAC), Pin Electronic Drivers, post-amplifier circuit for WCDMA transceiver system and high-speed multiplexers/demultiplexers. It is currently being used successfully in 40[Gb/s] OC768 SiGe designs. Experience has shown that it is important to let the designer have the informed choice to select the critical lines in the early design stages, that it is essential to properly shield the critical lines by their own return paths, and that true transient RLC network based models are highly cost effective in small to medium size designs up to very high frequencies.

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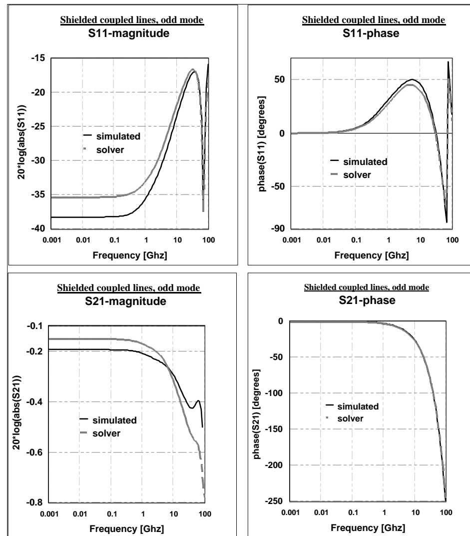

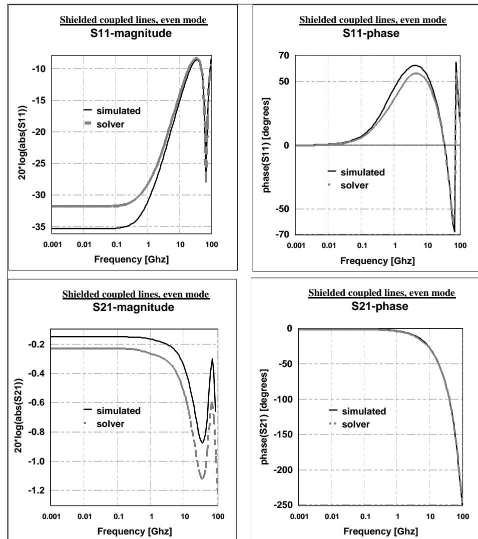

Figure 6. Comparing the model to field-solver for a dual wire T-line, showing odd-mode (top) and even mode (bottom) S-parameters.

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