An Interface Circuit for High-Accuracy Signal Processing of Differential-Capacitance Transducers

Kouji Mochizuki, *Member, IEEE,* Takashi Masuda, and Kenzo Watanabe, *Fellow, IEEE*

***Abstract*—An interface circuitry for high-accuracy signal processing of differential-capacitance transducers is developed. The architecture is based on the idea that the ratio of one of the transducer capacitances to its total capacitance represents the offset binary equivalent of the physical quantity under measurement. An opamp-based capacitance-to-voltage converter is commonly used for capacitance detection, and an analog-to-digital (A/D) converter is used for the ratiometric operation. Analyses show that the interface can detect the capacitance change as small as 0.01% of the total capacitance. Experimental results are also given to confirm the analyses.**

***Index Terms*—Analog circuit, capacitance transducers, intelligent sensors, pressure measurement, signal processing.**

I. Introduction

DIFFERENTIAL-CAPACITANCE transducers are widely used for detecting such physical quantities as pressure difference, linear displacement, and rotational angles. Their configurations depend on what quantity is to be measured [1], [2], but they can be represented by two capacitors whose capacitances change complementarily with the measurand. The complementary capacitance change may be linear or nonlinear. In either case, the accurate and linear detection of the measurand can be made by ratiometric signal processing which divides the capacitance difference between two capacitors by their sum. Beside such a ratiometric processing, a differential-capacitance transducer requires a special interface configuration because the two capacitors share one electrode in structure.

To meet these requirements, several techniques have so far been proposed, including switched-capacitor (SC), analog-to-digital (A/D) [3], [4], capacitance-to-frequency (C/F) [5], [6], and capacitance-to-phase conversion [7]. The SC technique is best suited for integrated circuit realization using CMOS process, but suffers seriously from clock feedthrough. Because of this error source, the resolution attainable with the SC method is estimated to be 1 fF [8]. A higher resolution is possible with the C/F conversion techniques [6], but their applications to high-speed real-time measurements seem difficult because they require a microprocessor for the calibration and the ratiometric operation.

Manuscript received July 12, 1996; revised December 10, 1998.

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Publisher Item Identifier S 0018-9456(98)09902-1.

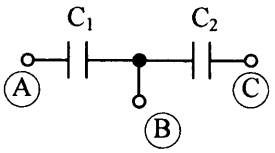

Fig. 1. An equivalent circuit of a differential-capacitance transducer.

The above-mentioned methods detect the capacitances of the transducer by sensing the charge stored in it. Sensing the current flowing through the transducer is another approach. Recent advances in high-speed opamps have made this approach quite attractive because they allow high-sensitivity and high-speed capacitance detection by means of the high-frequency probe signal. This paper describes an interface circuitry of a differential-pressure transducer based on this approach and demonstrates its performances.

II. Transducer Model

A differential-capacitance transducer can be represented by two capacitors with a common electrode, as shown in Fig. 1. In a linear displacement encoder, the areas of the electrodes change linearly with the displacement x. In a rotational angle encoder, the apparent permittivities of the capacitors change linearly with the angle x. In these encoders, therefore, the capacitances C_1 and C_2 change linearly with the measurand x and can be expressed as follows:

$$C_1 = \frac{C_0}{2}(1+x) \tag{1}$$

$$C_2 = \frac{C_0}{2}(1-x) \tag{2}$$

where C_0 is the total capacitance of the transducer. In a differential-pressure transducer, on the other hand, the spacings between the electrodes change linearly with the pressure difference x. Therefore, C_1 and C_2 are expressed as

$$C_1 = \frac{C_0}{2}\frac{1}{1-x} \tag{3}$$

$$C_2 = \frac{C_0}{2}\frac{1}{1+x}. \tag{4}$$

Whether the capacitance change is linear or hyperbolic, the measurand x can be detected independently of the total capacitance C_0 by the following ratiometric operation:

$$\frac{C_1 - C_2}{C_1 + C_2} = x. \tag{5}$$

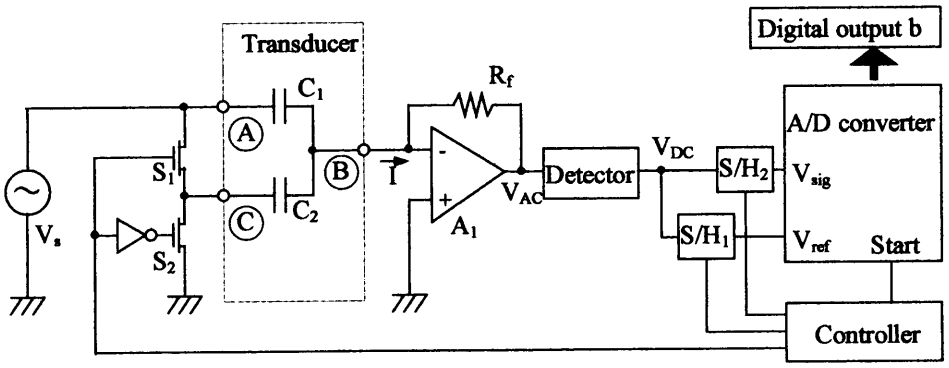

Fig. 2. A block diagram of the interface.

III. Interface Circuitry

A block diagram of the interface circuit to perform the ratiometric operation (5) is shown in Fig. 2. The circuit is designed based on the idea that component errors do not affect the ratiometric operation if a common stage is used for detecting $C_1 - C_2$ and $C_1 + C_2$.

The first stage is the capacitance-to-voltage converter. Sensing the current flowing through the transducer, it produces the output voltage proportional to the transducer capacitance. Assume for the moment that opamp A_1 and switches S_1 and S_2 are ideal. When S_1 is on and S_2 is off, the C/F converter senses the currents flowing through C_1 and C_2 to produce the output voltage V_{o1}

$$V_{o1} = -s(C_1 + C_2)R_f V_s \tag{6}$$

where V_s is the probe signal applied to the transducer. After conversion to a dc signal by the detector, this voltage is applied to the A/D converter as the reference voltage. When S_1 is off and S_2 is on, on the other hand, the C/F converter senses only the current flowing through C_1 to produce the output voltage V_{o2}

$$V_{o2} = -sC_1 R_f V_s. \tag{7}$$

After being converted to a dc signal by the detector, V_{o2} is applied to the signal input terminal of the A/D converter. The n-bit A/D converter then generates the binary number b given by

$$b = \frac{V_{o2}}{V_{o1}} = \frac{C_1}{C_1 + C_2} = b_1 2^{-1} + b_2 2^{-2} + \quad \cdots \quad + b_n 2^{-n}. \tag{8}$$

Modifying (5) as

$$x = \frac{C_1 - C_2}{C_1 + C_2} = \frac{2C_1}{C_1 + C_2} - 1 \tag{9}$$

and substituting (8) into (9), one finds that b is itself the n-bit offset binary representation of x.

The circuit diagram of the detector is shown in Fig. 3. It consists of a full-wave rectifier followed by a low-pass filter [9]. The low-pass output contains the ripple component. This component should be made small enough so that the ripple factor, defined as the ratio of the ripple component to the average dc output, is smaller than the relative measurement

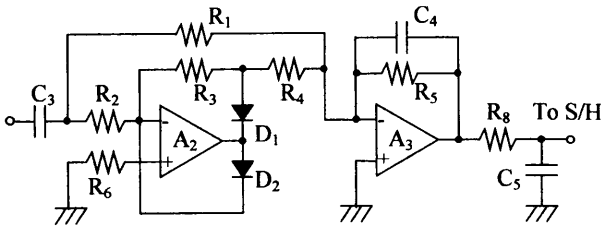

Fig. 3. The circuit diagram of the detector.

error ε specified for x. This requirement specifies the time constant, $\tau_C = C_4 R_5$, of the low-pass filter

$$\tau_C \geq \frac{1}{2f \ln(1 - \varepsilon)} \tag{10}$$

where f is the frequency of the sinusoidal source V_s applied to the transducer. The $\varepsilon\%$ settling time of the low-pass filter is then given by

$$\tau_S = -\tau_C \ln \varepsilon. \tag{11}$$

The settling time τ_S specifies the sampling speed of the S/H circuit, thereby limiting the conversion rate of the A/D converter to $f \ln(1-\varepsilon)/\ln \varepsilon$. Specifically, when $f = 1$ MHz and $\varepsilon = 0.1\%$, the conversion rate is 150 samples per second (sps).

The above estimate of the sampling speed assuming the first-order low-pass filter is pessimistic. The output of the detector settles much faster because V_{o1} and V_{o2} change slowly. In addition, the time constant τ_C can be made much smaller by adopting a second-order low-pass filter. Therefore, much higher speed can be expected without degrading the accuracy.

IV. Accuracy

Error sources involved in the interface circuit are parasitic capacitances, the input impedance and finite gain of opamp A, and the nonlinearity of the detector. Their effects on the accuracy are evaluated in this section.

The C/V converter involving the error sources is shown in Fig. 4. Exact analyses give the following expressions for the output voltages:

$$V'_{o(1,2)} = -\frac{Y_{s(1,2)}}{Y_f} \cdot \frac{k_{(1,2)}}{1 + \frac{1}{A}\left(1 + \frac{Y_i + Y_{s(1,2)}}{Y_f}\right)} V_s \tag{12}$$

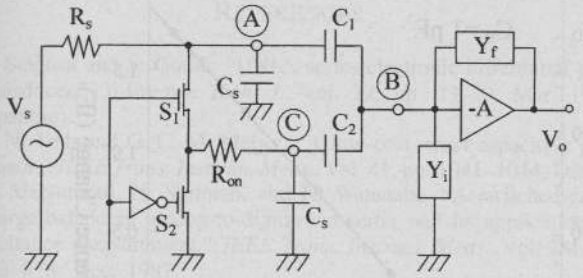

Fig. 4. The C/V converter including error sources.

TABLE I
ERRORS DUE TO PARASITICS

f [MHz]	R_{on} [W]	C_s [pF]	C_0 [pF]	Error ε ($\times 10^4$) x=-0.5	x=0	x=0.5
1	300	10	6	4.26	2.25	1.12
0.5	300	10	6	1.07	0.56	0.28
1	125	10	6	0.74	0.39	0.19
1	300	5	1	0.60	0.40	0.22

where V'_{o1} and V'_{o2} are the output voltages of opamp A_1 in the state 1 when S_1 is on and S_2 is off and in the state 2 when S_1 is off and S_2 is on, respectively. A and Y_i are the open-loop gain and input admittance of the opamp, respectively. Y_{s1} and Y_{s2} are the admittances of the transducer network in the state 1 and 2, respectively, seen from the inverting input terminal of opamp, and are given by

$$Y_{s1} = \left(sC_1 + \frac{1}{R_{\text{on}} + 1/sC_2} \right) \Bigg\| \frac{1}{R_s} \tag{13}$$

$$Y_{s2} = \frac{1}{R_s + 1/sC_1} + \frac{1}{R_{\text{on}} + 1/sC_2}. \tag{14}$$

Y_f is the admittance of the feedback network and $k(1, 2)$ are given by

$$k_1 = \frac{1 + s\,\dfrac{C_1(C_s + C_2)}{C_1 + C_2} R_{\text{on}}}{1 + s\left(C_s + \dfrac{C_1 C_2}{C_1 + C_2} \right) R_{\text{on}}} \tag{15}$$

$$k_2 = \frac{C_1}{C_1 + C_2} \frac{1 + s(C_s + C_2) R_{\text{on}}}{1 + s\left(C_s + \dfrac{C_1 C_2}{C_1 + C_2} \right) R_{\text{on}}}. \tag{16}$$

When $\omega C_1 R_s \ll 1$, which is a reasonable condition in practice, $Y_{s1} = Y_{s2}$ holds. Then, A and Y_i have no effect on the ratiometric operation and the A/D converter outputs the digital equivalent of $|k_2|/|k_1|$

$$\frac{|k_2|}{|k_1|} = \frac{C_1}{C_1 + C_2} \frac{|1 + s(C_s + C_2) R_{\text{on}}|}{\left| 1 + s\dfrac{C_1(C_s + C_2)}{C_1 + C_2} R_{\text{on}} \right|}$$

$$= \frac{C_1}{C_1 + C_2} (1 + \varepsilon) \tag{17}$$

where ε is the relative error given, to first order, by

$$\varepsilon = \frac{1}{2} \omega^2 (C_s + C_2)^2 \frac{(2C_1 + C_2) \cdot C_2}{C_0^2} R_{\text{on}}^2. \tag{18}$$

Table I lists the error ε evaluated for several cases. R_{on} and C_s quoted in this table assume standard analog switches and wiring, respectively. It indicates, therefore, that an accuracy better than 13 b is easily achievable without any special techniques and components.

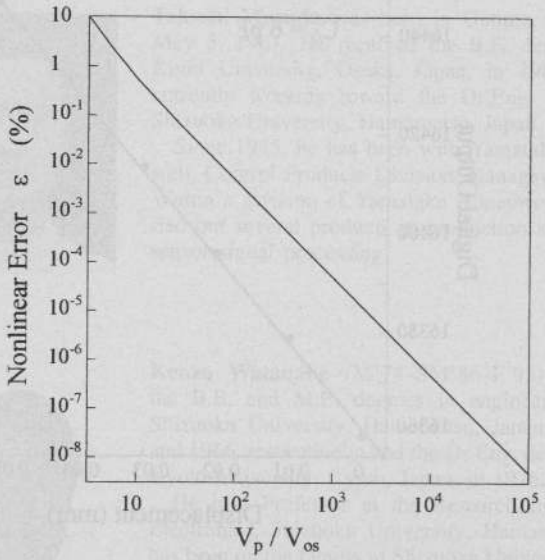

Fig. 5. Nonlinear error due to the offset voltage of opamps.

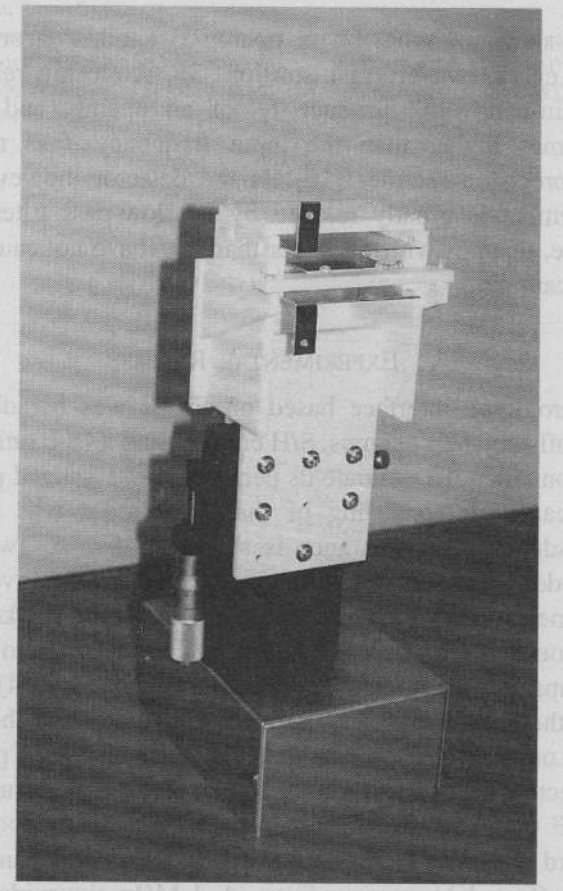

Fig. 6. A ganged parallel-plate capacitor used for experiments.

A main error source in the detector is the offset voltage V_{os} of opamp which modulates the conduction period of diode D_1 in Fig. 3. Its effect on the linear detection can be evaluated by integrating the input sinusoidal signal over the conduction period. The results are shown in Fig. 5. Decreasing with the peak amplitude V_p of the input signal, the nonlinear error becomes negligibly small if V_p is 100 times larger than V_{os}.

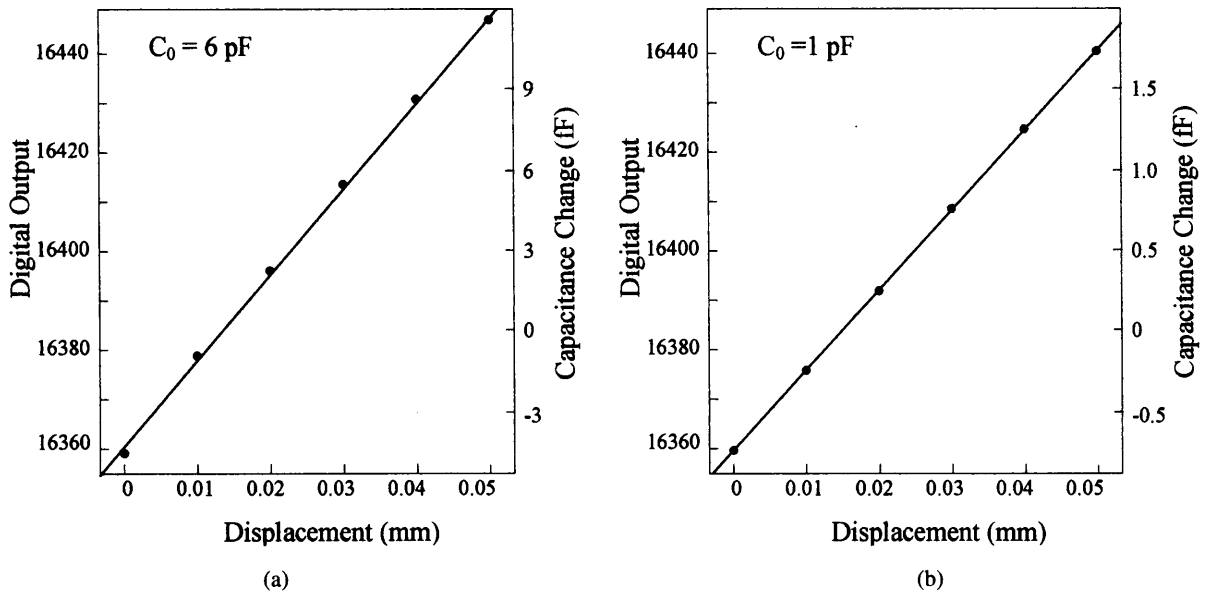

Fig. 7. Experimentally measured capacitance changes and the digital readings of the displacement when C_0 is (a) 6 and (b) 1 pF.

The slew rate (SR) of an opamp is another error source which causes waveform distortion. SR is closely related to the gain-bandwidth product f_T of an opamp, and an f_T 100 times higher than the input frequency f is required for a precision rectifier [10]. In the detector, however, this requirement is greatly relaxed by the low-pass filtering. In practice, opamps with f_T larger than $30f$ have not caused any significant error.

V. Experimental Results

A prototype interface based on Fig. 2 was breadboarded using off-the-shelf opamps, S/H circuits, and a 16-b ratiometric A/D converter. To evaluate its performance, a ganged parallel-plate capacitor consisting of three electrodes was used as a transducer. Its appearance is shown in Fig. 6. Two outer electrodes are fixed while the inner electrode is driven by a micrometer screw to move back and forth. The stroke of the micrometer is 22 mm, and its readings are accurate to 10 μm. The capacitances C_1 and C_2 are given by (3) and (4) with x being the displacement of the inner electrode from the center of two outer electrodes. The total capacitance C_0 is 6 pF when the electrodes measuring 47.5 mm × 47.5 mm are used and is 1 pF when the electrode dimensions are 10 mm × 5 mm. A guard electrode is installed to prevent the capacitance from being affected by surroundings. A 1-MHz sinusoidal signal with 1 $V_{p\text{-}p}$ amplitude is applied to the capacitor. Component values of the detector and the S/H circuits are selected such that V_{o1} applied to the A/D converter as the reference voltage is close to the recommended value of 3 V, and the full-scale digital output is 32 768. The nonlinear error of the detector is less than 0.02%.

Fig. 7 shows typical measurement results. Capacitance changes $\Delta C = C_1 - C_2$, and the digital readings $\Delta C/C_0$ for displacement x are indicated. Dots shown in the figures are average values of ten measurements. The standard deviation σ was 0.21 fF when $C_0 = 6$ pF and was 0.044 fF when $C_0 = 1$ pF. The maximum nonlinear error evaluated from the digital readings was 0.19 fF when $C_0 = 6$ pF and was 0.036 fF when $C_0 = 1$ pF. These data indicate that the measurement uncertainties decrease in proportion to C_0. As can be seen from Fig. 7, the capacitance change is 3 fF/10 μm when $C_0 = 6$ pF and is 0.5 fF/10 μm when $C_0 = 1$ pF. The minimum scale of the micrometer is 10 μm. Therefore, it may be reasonably concluded that the measurement accuracy is wholly dominated by reading errors and backlash of the micrometer screw and that the signal processing accuracy of the interface is far beyond these limits.

Similar measurements were also repeated for a wide variety of opamps. No remarkable difference could be found for high-speed opamps with f_T larger than 30 MHz. Excellent linearity was also found over a wide range of displacement. These preliminary measurements confirm the principles of operation and the accuracy estimate of the interface and prove its validity for high-accuracy signal processing of differential-capacitive transducers.

VI. Conclusions

An interface circuitry of differential-capacitance transducer which performed the ratiometric operation of dividing one of the transducer capacitances by its total capacitance was described. The front end consisting of a C/V converter and a detector was commonly used for the capacitance detection. This time-multiplexing capacitance detection using the common stage followed by the ratiometric operation using an A/D converter is quite useful for high-accuracy signal processing. Analyses have shown that capacitance change as small as a few tenths of fF can be detected by this architecture. Performance evaluation of a prototype interface using a ganged parallel-plate capacitor has confirmed the accuracy estimate.

The interface described herein allows high-accuracy signal processing with standard components. The sampling speed higher than 5 ksps can also be expected if a second-order low-pass filter is incorporated in the detector. These distinct features encourage its integrated circuit (IC) realization. Applications to practical transducers are another future work.

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