An Isolated Resonant Mode Modular Converter with Flexible Modulation and Variety of Configurations for MVDC Application

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***Abstract*—The dc tap or dc transformer will play an important role in interfacing different voltages of dc links in dc grids. This paper presents an isolated resonant mode modular converter (RMMC) with flexible modulation and assorted configurations to satisfy a wide variety of interface requirements for medium voltage dc (MVDC) networks. The transformer-less RMMC, as introduced in the literature, implemented a restricted modulation scheme leading to a very limited range of step-ratio and the diode rectifier resulted in unidirectional power flow. Both of these limitations are removed in this proposal and galvanic isolation has also been added. Moreover, this new RMMC approach can serve as a building block for variety of configurations. Two such derived topologies are given, which inherently balance the voltage and current between different constituent circuits and realize the high power rating conversion for very low or very high step-ratio application. The theoretical analysis is validated by a set of full-scale simulations and a down-scaled experimental prototype. The results illustrate that this isolated RMMC and its derivatives have promising features for dc taps or dc transformers in MVDC applications.**

***Index Terms*—modular multilevel converter, resonant dc-dc conversion, dc tap, dc transformer, MVDC.**

I. INTRODUCTION

THE RAPID development of renewable energy in the last decade has led to increased interest in medium voltage dc (MVDC) research [1]–[3]. One of the most significant challenges in MVDC networks is the dc voltage transformation devices for various conversion specifications. The low power throughput but high step-ratio converter, often termed as ‘dc tap’, has roles in collecting the power from distributed generation and feeding low voltage dc or ac loads [4]–[6]. On the other hand, the high-power dc-dc converter, or ‘dc transformer’, will play a key role in interfacing dc grids at different voltage levels, including the low step-ratio connection between two MVDC distribution grids of slightly different voltages, and the high step-ratio linking from the MVDC grid to the low voltage dc (LVDC) microgrid [7], [8].

Dc-dc conversion at a low voltage has attracted great attention for many years to achieve various step-ratios and high efficiencies [9]–[11]. Most of topologies are of a single switch configuration with high switching frequency and are therefore not readily extended to the medium voltage ranges. Multiple module designs can overcome this problem by utilizing series and parallel arrangements. The widespread solution for medium voltage dc-dc conversion is the dual-active-bridge (DAB) topology and its wider family of circuits that offer soft-switching operation, bidirectional operation capability and high power density [12], [13]. The modular DAB has been considered as the key circuit for the ac solid state transformers (SST) and has raised great interest for dc transformer research [14]–[16]. However, modular converters in DAB family need a large number of module transformers to achieve high power and high step-ratio conversion, which raises isolation challenges and decreases the system reliability. Moreover, the complex balancing control that is required between different modules would be another drawback in the practical operation although some relevant solutions have been presented [17], [18]. These difficulties can be avoided in modular multilevel converter (MMC) technology which has been extensively developed in recent years for several kinds of high voltage power conversion [19], [20] following its success in voltage-source-converter high voltage dc transmission (VSC-HVDC). The front-to-front configuration of MMC is one of the most promising choices to interconnect two different HVDC links because of the good modularity, symmetry and flexibility [21]–[23]. Different modulation methods were presented to improve power density and efficiency [24]–[26]. However, it is not a low-cost option for MVDC applications since the power devices utilization is usually lower than competing approaches [14], [27], and the complicated rotation algorithm and hard switching operation may further undermine its advantages for MVDC conversion. The concept of the dc auto-transformer with modular multilevel design was proposed in [28]–[31]. Part of sub-modules in the stack were utilized on both high-voltage side and low-voltage side. High power-device utilization was achieved leading to a reduced cost but the large inductance required [28], [29] and difficulties with dc fault management [30], [31] would weaken this benefit.

Apart from the above-mentioned well-known topologies, the resonant dc transformer opens a new road for medium voltage dc-dc conversion after the basic resonant topology was proposed in [32]. Soft-switching operation was achieved for all the switches in the circuit facilitating high efficiency conversion. Extension of the topologies presented can interface to either a current source converter (CSC) link or VSC link. A transformer-

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less resonant mode modular converter (RMMC) was proposed in [33] and moved one step forward for medium voltage and high voltage tap applications through the combination of the principles of the MMC with the classic dc-dc converter topologies. The sub-module (SM) switches in RMMC were operated in a soft-switching mode and the SM capacitor voltages were inherently balanced without any extra rotation scheme. However, all such resonant converters have to suffer one common problem which is that some of the switches and capacitors in the circuit are required to withstand either high voltage or high current stress due to the resonant operation. Additionally, the lack of galvanic isolation is another disadvantage for these resonant converters presented so far, which limits the application areas and constrains their potential for further configurations.

To satisfy a wide variety of interface requirements for future MVDC networks and resolve the difficulties in transformer-less resonant circuits, an isolated RMMC with flexible modulation and assorted configuration is presented in this paper. Firstly, this new RMMC approach inherits the benefits of inherent SM voltage-balancing capability and soft-switching operation from the transformer-less RMMC, and expands the application areas with the addition of galvanic isolation and bidirectional power flow. Further, the proposed flexible modulation substantially extends the step-ratio of this isolated RMMC from a narrow area around a nominal conversion ratio to a much wider range. It should be noted that the current stress on the power switches would be an obstacle of this isolated RMMC to expand the power rating and application scope. Two specific topologies derived from this converter are illustrated as examples of the assortment configurations, which inherently balance the voltage and current between different constituent parts and realize the high power rating conversion for very low or very high step-ratio application.

II. Operating Principles and Modulation Schemes

The topology of the isolated RMMC is shown in Fig. 1. The high-voltage side contains a stack of N_t half-bridge SMs connected to the primary winding N_1 of the transformer T. The leakage inductance of the transformer can be served as the resonant inductance L_r, and the magnetizing inductor L_M appears in paralleled and provides the return path for the dc current component. An active full-bridge rectifier/inverter with fully controllable IGBT devices is chosen to connect the secondary winding N_2 to the low-voltage link capacitor C_L, enabling the bidirectional power flow between the high-voltage side and low-voltage side. The arrows in Fig. 1 denote the reference directions of the stack voltage v_{ST}, SM voltage v_{SM}, SM capacitor voltage v_C, transformer voltage on the secondary side v_t, resonant current i_r and low-voltage side current i_s. The turns ratio of the transformer is defined as $r_T = N_1/N_2$, and the stack modulation ratio is defined as $r_S = V_H/r_T V_L$, indicating the voltage conversion achieved within the stack itself.

The original modulation scheme [33] can still be implemented in this isolated RMMC. The stack supports the high-voltage dc link with either N_t-1 or N_t SMs and generates a square-wave voltage (N_t-1 SMs for the positive stage and N_t SMs for the negative stage). All the SMs are operated with a duty-cycle value of $(2N_t-1)/2N_t$ at a switching frequency f_s and they form a sequence of voltage pulses with a phase-shift value of $2\pi/N_t$.

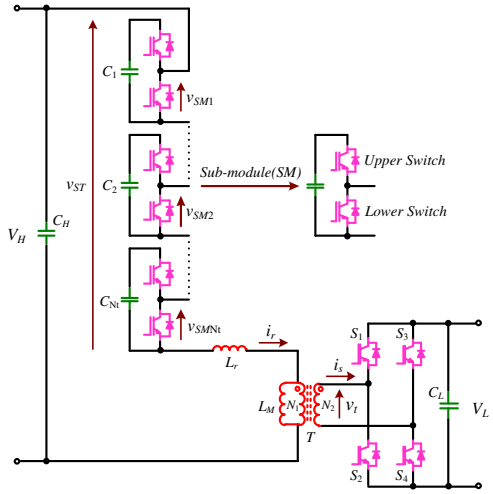

Fig. 1. Isolated resonant mode modular converter.

In this mechanism, the effective frequency of the generated square-wave voltage is increased to $N_t f_s$, and it excites an energy exchange between the SM capacitors and the resonant inductor, which forms the resonant tank of this isolated RMMC. There will be N_t-1 SMs switched into the stack for the positive stage. Their capacitors participate in the resonant operation with L_r and the single remaining SM is bypassed in this stage. The resonant frequency of this positive stage is therefore defined as f_p in (1) given the assumption that every SM capacitance is C, and the resonant frequency of the negative stage can be similarly derived as f_n, in which all the SMs capacitors are inserted into the stack and resonating with L_r. This converter has a stack of SMs similar to those in the classic dc/ac MMC, but the modulation method has been modified to achieve the high-step ratio dc/dc conversion and the resulting voltage waveforms are not the traditional staircase. The effective frequency f_e is normally controlled at an optimal value between f_p and f_n, operating in continuous current mode (CCM) in positive stage and in discontinuous current mode (DCM) in negative stage to trade-off between the conduction losses and switching losses for the best overall efficiency.

$$f_p = \frac{\sqrt{N_t - 1}}{2\pi \cdot \sqrt{L_r C}} \le f_e = N_t f_s \le f_n = \frac{\sqrt{N_t}}{2\pi \cdot \sqrt{L_r C}} \tag{1}$$

The voltage relationship derived from the positive and negative stages can be written as (2) and (3) respectively under the assumptions that all of the SM capacitor voltages are well-balanced at their average value $\overline{v_C}$ and the resonant voltage across L_r is far smaller than V_H.

$$V_H - (N_t - 1)\overline{v_C} = r_T V_L \tag{2}$$

$$V_H - N_t \overline{v_C} = -r_T V_L \tag{3}$$

So, the step-ratio R and average voltage of the SM capacitors $\overline{v_C}$ can be obtained as (4) and (5).

$$R = \frac{V_H}{V_L} = (2N_t - 1) r_T = r_S r_T \tag{4}$$

$$\overline{v_C} = \frac{2V_H}{2N_t - 1} \tag{5}$$

The difference between high-side voltage V_H and stack voltage v_{ST} is the transformer voltage on the primary side $r_T v_t$. Substituting (5) into (2) and (3), the transformer voltage can be

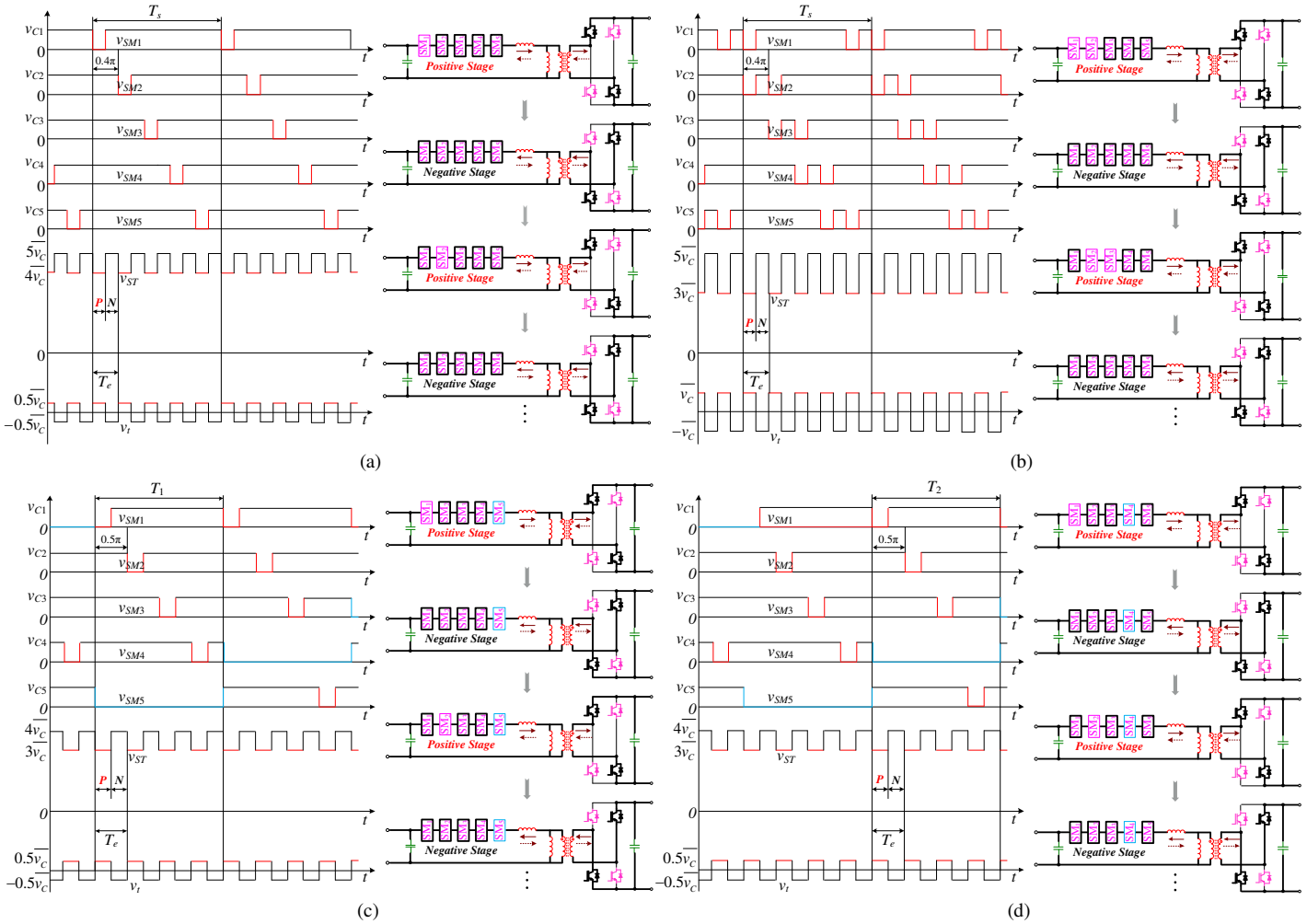

Fig. 2. Operation waveforms with SM total number N_t = 5. (a) Original/basic modulation scheme. (b) Flexible modulation scheme for j = 3 and k = 5. (c) Flexible modulation scheme for j = 3 and k = 4: first switching cycle. (d) Flexible modulation scheme for j = 3 and k = 4: second switching cycle.

described in (6).

$$r_T v_t = \pm \frac{V_H}{2N_t - 1} \tag{6}$$

To further illustrate operation, the detailed operation waveforms are illustrated in Fig. 2(a) taking $N_t = 5$ as an example. The solid arrows display the actual current flow when power direction is from the high-voltage link to the low-voltage link, and the operation of reverse power flow is denoted by the lower dash arrows. The black line of the SM voltage waveform (v_{SM1}, v_{SM2}, v_{SM3}, v_{SM4}, v_{SM5}) means the upper switch of this SM is on, while the red line means its lower switch is on. The red periods of stack voltage v_{st} and transformer voltage v_t are the positive stages whereas the black periods are the negative ones.

In Fig. 2(a), the upper switches of the SMs are deployed and the capacitors are in circuit with a duty-cycle of 90%, and for the remaining 10% SM capacitor is bypassed. The operation of the SMs is phase-shifted by 0.4π such that bypass states are interleaved as shown. The resonant frequencies and effective frequency can be derived by (1), and the step-ratio in this example is $9r_T$.

Replacing the average value in (2) and (3) with the individual SM capacitor voltages, yields (7) which describes the voltage relationship in each switching cycle T_s (in this example T_s is five times the effective cycle T_e). In the matrix, "$\mathbf{A_{5,4}}$" denotes there are five SMs switched into the stack for the negative stage and four for the positive stage. "1" means the SM upper switch is on and its capacitor is inserted in the circuit whereas "0" means the lower switch is on and the capacitor is bypassed. The first five rows show the five individual positive stages in one switching cycle with different SM bypassed in the circuit, and last row shows the common negative stage with all the SM deployed.

$$\begin{bmatrix} \mathbf{A_{5,4}} & \mathbf{1_{5\times 1}} \\ \mathbf{1_{1\times 5}} & -1 \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{v_{Ci}} \\ r_T V_L \end{bmatrix} = \begin{bmatrix} \mathbf{1_{5\times 1}} \\ 1 \end{bmatrix} \cdot V_H \tag{7}$$

with $\mathbf{A_{5,4}} = \begin{bmatrix} 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \end{bmatrix}$ and $\boldsymbol{v_{Ci}} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \end{bmatrix}$.

Solving (7), all SM capacitors adopt the voltage in (8). The SM capacitors are inherently balanced in voltage by this basic modulation scheme which rotates the set of SMs that are connected across the high-side voltage.

$$v_{C1} = v_{C2} = v_{C3} = v_{C4} = v_{C5} = \overline{v_C} = \frac{2V_H}{9} \tag{8}$$

The simple modulation scheme illustrated here switches between a positive stage with j=N_t−1 SMs on and a negative stage with k=N_t SMs on ($\mathbf{A_{k,j}}$, both j and k are at the maximum values they can have). This achieves the high step-ratio

conversion and inherent SM balancing capability. However, the flexibility and reliability of this converter are limited with this modulation scheme. The step-ratio is restricted to a narrow range dictated by the parameters N_t and r_t, and successful operation relies on all SM being healthy. In fact, the circuit can be operated by modulating the value of j and k from their minimum to maximum ($0<j<k\leq N_t$), and thus a wider range of step-ratios can be realized. The duty-cycle and phase-shift values are generalized here to $(k+j)/2k$ and $2\pi/k$. With proper combination for j and k values, this converter can still inherently balance all SM capacitor voltages. The relationships of frequencies and step-ratio are described as (9) and (10) respectively.

$$f_p = \frac{\sqrt{j}}{2\pi \cdot \sqrt{L_r C}} \leq f_e = k f_s \leq f_n = \frac{\sqrt{k}}{2\pi \cdot \sqrt{L_r C}} \tag{9}$$

$$R = \frac{V_H}{V_L} = \frac{k+j}{k-j} r_T \tag{10}$$

Compared with (4), this modulation method extends the application from only high step-ratio conversion to medium and even low step-ratio cases. The range between f_p and f_n in (9) is variable due to different combinations of j and k values for different application cases, but the switching frequency and effective frequency would maintain at specific values (or very small range for voltage regulation) in each given application for the best efficiency. The SM capacitors' average voltage and the transformer voltage are given in (11) and (12) respectively.

$$\overline{v_C} = \frac{2V_H}{k+j} \tag{11}$$

$$r_T v_t = \pm \frac{k-j}{k+j} V_H \tag{12}$$

It can be derived that the total voltage of the SM capacitors would be slightly higher than the high-side link voltage to generate an ac voltage across the transformer, which is similar to the classic ac/dc MMC and other MMC derived dc-dc converters with an intermediate ac stage for galvanic isolation [21]–[25].

To explain this flexible modulation scheme more detail, example is illustrated in Fig. 2(b) in which $j = 3$ and $k = N_t = 5$. It explains the operating principles when positive stage SM number j ranges from the minimum to maximum ($0<j\leq N_t-1$).

It is shown in Fig. 2(b) that all the SM capacitors are in the resonance path in the negative stage, as in the basic operation, but two ($k-j$) SMs are modulated out of the stack in sequence for the positive stage. The voltage relationship for each effective cycle is given in (13).

$$\begin{bmatrix} \mathbf{A_{5,3}} & \mathbf{1_{5\times 1}} \\ \mathbf{1_{1\times 5}} & -1 \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{v_{Ci}} \\ r_T V_L \end{bmatrix} = \begin{bmatrix} \mathbf{1_{5\times 1}} \\ 1 \end{bmatrix} \cdot V_H \tag{13}$$

with $\mathbf{A_{5,3}} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix}$ and $\boldsymbol{v_{Ci}} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \end{bmatrix}$.

The inherent balancing among SMs presented in the basic scheme is still achieved and the capacitors adopt the voltage in (14). The resonant frequencies are derived by (9), and the step-ratio in this mode is $4r_T$.

$$v_{C1} = v_{C2} = v_{C3} = v_{C4} = v_{C5} = \overline{v_C} = \frac{V_H}{4} \tag{14}$$

Another example is given in Fig. 2(c) and Fig. 2(d) to display the general operation law when the number of SM in the negative stage k ranges from $j+1$ to N_t. There will be k SMs inserted into the stack and participate in the resonant operation in one switching cycle, and these k SMs are defined as the active SMs. The operation scheme of these k SMs is the same as the method explained in Fig. 2(b). The value of j can still be modulated from 0 to $k-1$. The remaining N_t-k SMs are bypassed in this switching cycle and defined as the redundant SMs, which are denoted by blue in Fig. 2(c) and Fig. 2(d). It is worth noting that besides the internal phase-shift within each switching cycle for the active SMs modulation, there is another external phase-shift scheme for the redundant SMs among different switching cycles so that all the N_t SMs play the redundant role in turn.

Fig. 2(c) shows that the fifth sub-module SM_5 is bypassed throughout the first switching cycle (i.e. it is inactive and is playing the redundant role), and the other four SMs resonate with L_s as the normal operation. It needs to be noted, the duty-cycle and phase-shift angle of the active SMs are 87.5% and 0.5π as is appropriate for four active SMs. When the second switching cycle begins, SM_5 replaces the role of SM4 and participates in the resonant operation while SM4 is bypassed for the whole cycle and plays the redundant role, shown in Fig. 2(d). The voltage relationships in these two switching cycles are described in (15) and (16) respectively.

$$\begin{bmatrix} \mathbf{A_{4,3}} & \mathbf{1_{4\times 1}} \\ \mathbf{1_{1\times 4}} & -1 \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{v_{Ci1}} \\ r_T V_L \end{bmatrix} = \begin{bmatrix} \mathbf{1_{4\times 1}} \\ 1 \end{bmatrix} \cdot V_H \tag{15}$$

$$\begin{bmatrix} \mathbf{A_{4,3}} & \mathbf{1_{4\times 1}} \\ \mathbf{1_{1\times 4}} & -1 \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{v_{Ci2}} \\ r_T V_L \end{bmatrix} = \begin{bmatrix} \mathbf{1_{4\times 1}} \\ 1 \end{bmatrix} \cdot V_H \tag{16}$$

with $\mathbf{A_{4,3}} = \begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix}$, $\boldsymbol{v_{Ci1}} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \end{bmatrix}$ and $\boldsymbol{v_{Ci2}} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C5} \end{bmatrix}$.

In the next (third) switching cycle, SM_3 replaces and SM4 returns to take part in the resonance again. From (15) and (16), it can be derived all of the SM capacitor voltages are still inherently balanced at $2V_H/7$, and the step-ratio in this case is $7r_T$.

In general cases, as long as the voltage description matrix is not rank deficient, this isolated RMMC can keep the inherent balancing capability and all the SMs are balanced at $2V_H/(k+j)$. Meanwhile, all the SMs take turns to be the redundant SMs, and faulty SMs can be bypassed directly without interrupting normal operation as in the classic MMC [34].

III. Circuit Performance and Variety of Configurations

In this section, performance of the isolated RMMC is analyzed and the operational advantages and limitations discussed. Following that, two extended configurations are proposed to overcome the inherent challenges in single converter operation and accomplish the high power rating conversion for very low or very high step-ratio application.

A. Step-ratio Range

Following from (10), the minimum and maximum step-ratio of this converter are derived as (17), and plotted by blues lines and red lines respectively in Fig. 3.

$$R_{min} = \frac{N_t+1}{N_t-1} r_T, R_{max} = (2N_t-1) r_T \tag{17}$$

Since there is only one combination of positive stage number and negative stage number in the basic modulation (j=N_t−1, k=N_t), the step-ratio would be restricted to the red lines only whereas with the improved modulation scheme (j and k ranging from 0 to N_t−1 and j+1 to N_t respectively), the converter can operate between the red and blue lines. This provides another control freedom to expand the step-ratio of this converter from a narrow to a wide range which can have up to $N_t(N_t-1)/2$ choices so that various application cases can be satisfied. This makes the converter more attractive for operation as dc tap in MVDC grids.

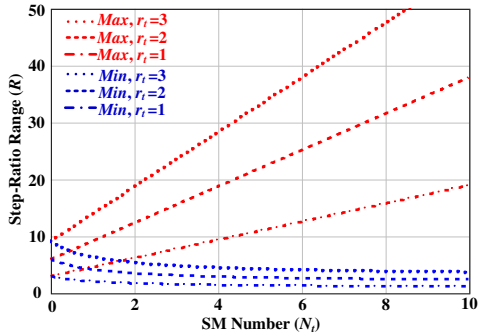

Fig. 3. Step-ratio range of the isolated RMMC.

B. SM Capacitor Sizing

Since the high-voltage side of this converter contains a stack of half-bridge SMs to support the high-voltage dc link, the SM capacitor size becomes an important metric to evaluate the volume and cost of this converter because it typically accounts for half the volume of each SM in a traditional MMC [19]. With the analysis in (2) and (3), the stack voltage can be given in (18), which is comprised of a dc offset V_H and an ac component $r_T v_t$.

$$v_{st}(t) = V_H - r_T v_t(t) \tag{18}$$

The stack current i_{ST} also consists of a dc offset I_H from the high-voltage link and an ac component i_s/r_T flowing to the transformer. Noting that the time difference between the resonant cycle and effective cycle is very short and the resonant current in this short period is very small, the stack current can be simplified as (19). The amplitude of the ac component A_t can be derived from (20) and expressed in (21) according to the power balance between the primary side and secondary side.

$$i_{ST}(t) = i_r(t) = i_{dc}(t) + i_{ac}(t) = I_H + A_t\left(sin\frac{2\pi}{T_e}t\right) \tag{19}$$

$$\int_0^{T_e} v_t(t) i_s(t) dt = 2\int_0^{\frac{T_e}{2}} V_L r_T A_t\left(sin\frac{2\pi}{T_e}t\right) dt = V_H I_H T_e \tag{20}$$

$$A_t = \frac{\pi V_H I_H}{2V_L r_T} = \frac{\pi I_L}{2r_T} \tag{21}$$

It can be derived that the dc component I_H will be much smaller than the amplitude of the ac component $\pi I_L/2r_T$ especially in the high-step ratio conversion. In the meantime, the transformer voltage is a symmetrical ac component with small magnitude of $r_T V_L$. This trivial and well-controlled dc current offset will not have a big effect on the transformer.

With (18) and (19), the energy deviation of the stack in one effective cycle T_e is obtained in (22) and plotted in Fig. 4.

$$dE_{ST}(T_e) = \int_0^{T_e} v_{ST}(t) i_{ST}(t) dt = \int_0^{T_e} [V_H - r_T v_t(t)] \cdot [I_H + \frac{\pi V_H I_H}{2V_L r_T}\left(sin\frac{2\pi}{T_e}t\right)] dt = V_H I_H T_e - \frac{\pi V_L I_L}{2}[\int_0^{\frac{T_e}{2}}\left(sin\frac{2\pi}{T_e}t\right) dt - \int_{\frac{T_e}{2}}^{T_e}\left(sin\frac{2\pi}{T_e}t\right) dt = V_H I_H T_e - V_L I_L T_e = 0 \tag{22}$$

The effective frequency f_e of this converter is several times the SM switching frequency f_s as noted in (9), and so it is realistic to illustrate the operation using an effective frequency of 2.5 kHz. Firstly, it can be seen from both (22) and Fig. 4 that the stack energy of this converter is naturally balanced. The net ac energy and dc energy deviation are zero over each effective cycle without extra balancing control. Moreover, the maximum energy deviation of this converter is around 1.5 kJ/MVA, which is much smaller than other MMC dc-dc converters with the same switching frequency range (300–500 Hz) [21], [22], [24]. This implies that the more compact and lower cost SM design could be achieved in this isolated RMMC. Lastly, noting that smaller stack ratios lead to smaller energy deviation, the split between the turn ratio and stack ratio could be optimized in the converter for the most compact overall conversion volume.

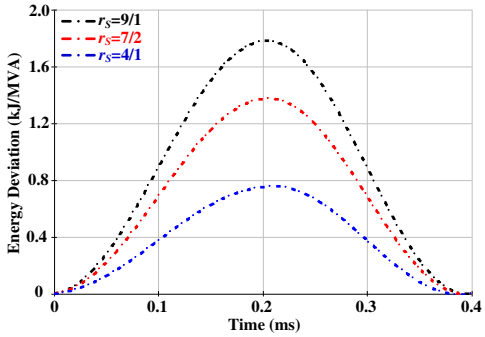

Fig. 4. Energy deviation in one effective cycle of the isolated RMMC.

C. Variety of Configurations

The flexible modulation scheme has opened up a wider range of possible step-ratios for an isolated RMMC, but its practical application will be still constrained in some areas because the conversion ratio cannot reach either very high or very low values in the actual operation due to the current or voltage limits of power devices and dc capacitors.

From (19) and (21), it can be found that the most challenging aspect for the power ratings of an isolated RMMC is likely to be the resonant current stress on the secondary side switches and the consequent ripple on the dc capacitors. This resonant current also flows through the SM switches on the primary side, but it is less significant within the longer and slower cycle C_s. However, the switches on the secondary side need to carry the amplitude of this current with the short and fast cycle C_e. Further, this current stress increases as the step-ratio extends to higher values, which will be problematic in the high-power and very high step-ratio conversion. On the other hand, the basic full-bridge circuit on the secondary side is more suitable to connect a low voltage within the capability of a single IGBT switch. The blocking voltage of a single switch would also be a barrier when the step-ratio becomes very low (close to one) and the low-side voltage is relatively high.

Fortunately, though, the isolated version of the RMMC lends itself to being the starting point for further configurations and the

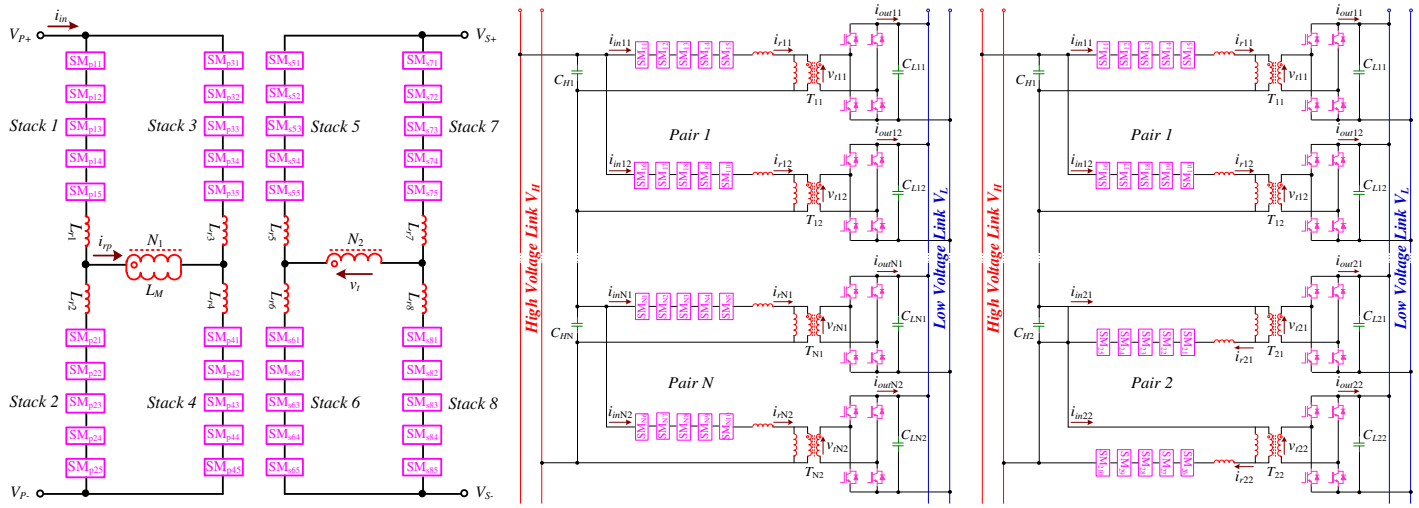

Fig. 5. The derivative topologies of the isolated RMMC. (a) Front-to-front configuration. (b) Parallel-series configuration. (c) Parallel-series configuration with the adjustment for module transformer isolation.

difficulties of working with very low step-ratio or very high step-ratio can be overcome in an assortment of derived topologies.

Turning first to very low step-ratio conversion cases, the front-to-front configuration of the isolated RMMC, shown in Fig. 5(a), can be employed. It is a DAB style converter with four individual RMMC stacks in each side. The SMs in stack 1 (stack 5) and stack 4 (stack 8) work in the same switching sequence and constitute one resonant loop, and the rest stack 2 (stack 6) and stack 3 (stack 7) resonate in another loop with the opposite current direction. Thus, these resonant currents sum at the transformer and negate at the dc-links, and the dc components of the stack currents collect from dc-links and cancel at the transformer. Compared to the single circuit operation, this front-to-front configuration increases the power four times and remove the requirement for dc-link capacitors. More importantly, since the circuit on the secondary side is symmetrical with the primary side, the resonant currents flow through all the power devices in a slower cycle C_s and the secondary side voltage is also divided equally by the secondary SMs, as for the primary side. Because of this sharing, the current and voltage limits of power devices are no longer obstacles to achieving high-power and low ratio conversion. In comparison with the traditional front-to-front dc/dc converters with modular design [21], [25], this configuration has the operational advantages of inherent SM balancing, compact SM design and soft-switching operation, which are inherited from the single isolated RMMC, but the power device utilizations would suffer drawbacks compared to the MMC-based dc auto-transformer design [29], [31].

Turning next to very high step-ratio cases, the parallel-series configuration of the isolated RMMC, shown in Fig. 5(b), can be used. The isolated RMMC serves as a circuit module. Two modules for a pair placed in parallel with the second module phase-shifted by π/k with respect to the first to offset the resonant current ripple imposed in the capacitors of the high-voltage link. The various pairs are placed in series and have a phase-shift of π/kN with respect to the previous pair in order to alleviate the filtering demand on the low-voltage side. Since all the modules are operated the same way as in the single circuit isolated RMMC, the operation benefits stated before will remain in this configuration, and it has the capability to inherently balance the voltage and current among the various modules. Compared with other dc-dc converters with the similar multiple module concept [14], [27], this parallel-series configuration could have the advantages in lower switching frequency and higher power device utilization, but the current stress would be its weakness.

D. Transformer Isolation and System Reliability

Galvanic isolation is one of the most critical issues for practical application of multiple module dc-dc converters. The parallel-series configuration in Fig. 5(b) can alleviate some isolation difficulties and has some benefits over the traditional modular DAB topologies.

Firstly, it reduces the large number of module transformers needed in modular DAB circuits, which saves system isolation space and decreases the failure rate caused by module transformers' breakdown. Further, the maximum isolation voltage between transformer primary side and secondary side in modular DAB converters has to be the difference between high-side link voltage V_H and low-side link voltage V_L. According to the analysis in (10) and (17), the SM stacks in this modular isolated RMMC will withstand a significant part of high-side voltage, so the maximum transformer isolation voltage would be smaller than the difference between V_H and V_L. Lastly, the transformer position in Fig. 5(b) can be adjusted in some specific applications to reduce the isolation requirement between module transformers. In a four-module configuration example shown in Fig. 5(c), the SM stack in the first pair is placed before its module transformer but the second pair is placed after. The operation principle remains the same as Fig. 5(b) but the transformer isolation voltage between the first pair and second pair is decreased. Overall, this parallel-series configuration could not fully resolve the transformer isolation problems, but some difficulties are alleviated and system reliability can be improved.

E. System Application and Fault Management

Prospects for dc collection and distribution are significantly strengthened by the advent of dc grids [1], [35]. Compared with

the conventional ac collection and distribution, dc connection has potential benefits in overall system size and weight [2], [16] since the bulky 50/60 Hz transformers can be avoided. Further, a dc configuration is more cost-effective for connection of distributed renewable generation and storage batteries [8], [36].

The isolated RMMC and its derivative configurations can play a key role in dc collection and distribution, and the different circuits are well suited to different applications, as shown in Fig. 6. The single circuit (SC) isolated RMMC can serve as the interface between low power dc collection (distribution) and MVDC networks, and the parallel-series configuration (PSC) would play a similar role for high power dc collection or distribution. The power flow between dc collection and distribution networks of different voltages or that require separation can be realized by the front-to-front topology (FFC).

Providing effective fault management is a significant obstacle for dc collection or distribution if the dc-dc converters lack the capability to limit or interrupt fault current. The isolated RMMC and its derivative configurations (PSC and FFC) would not suffer this disadvantage because they can make use of their intermediate medium frequency ac stage to prevent the short circuit fault propagating from one side to the other. A fault on the high voltage side will ground the primary stacks but the secondary side active rectifier can prevent flow of fault current from the low voltage side to the fault. In the case of a fault on the low voltage side, the primary stacks remain in full control of the currents as they have sufficient SM voltage to withstand the high-side link voltage. This dc-ac-dc conversion itself provides a good dc fault management without any extra protection equipment, and black start capability can be achieved inherently.

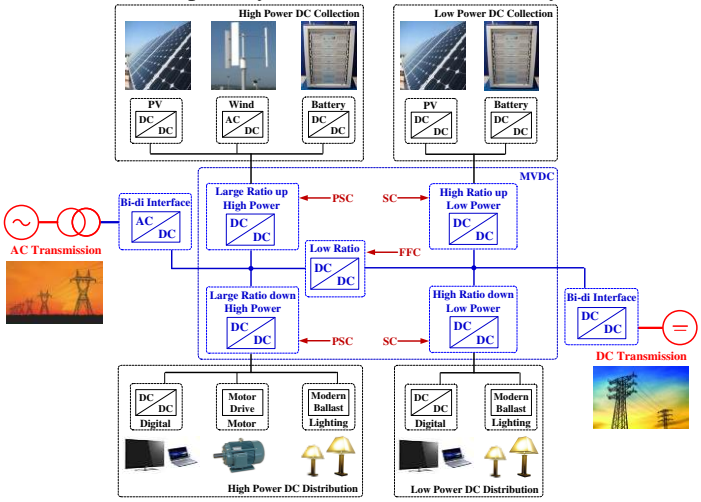

Fig. 6. Converters application in dc collection and distribution.

IV. Medium Voltage Application Examples

This section conducts a set of full-scale simulations to verify the theoretical analysis and explore application examples.

Recognizing the voltage and current limits of up-to-date power devices, the single circuit isolated RMMC is suitable to serve as a dc tap with low power throughput (P<1 MW) and reasonably medium step-ratio range ($4 \le R \le 9$) in MVDC networks. Possible roles are supplying a small DC load or transferring power from distributed generation to a MVDC link. Example converter parameters are listed in Table I.

Table I. Simulation Parameters of a Single Circuit Isolated RMMC

Symbol	Description	Value
P	*Rated Power*	0.7 MW
V_H	*High-side Link Voltage*	10 kV
V_L	*Low-side Link Voltage*	1.1 kV–2.5 kV
r_T	*Turns Ratio*	1/1
L_r	*Resonant Inductor*	15.6 μH
N_t	*SM Number*	5
f_s	*Switching Frequency*	500–600 Hz
C_1	*SM_1 Capacitor*	943 μF
C_2	*SM_2 Capacitor*	951 μF
C_3	*SM_3 Capacitor*	969 μF
C_4	*SM_4 Capacitor*	978 μF
C_5	*SM_5 Capacitor*	960 μF
E	*Energy Stored*	16.7 kJ/MVA
$C_H C_L$	*DC-link Capacitor*	300 μF
S	*Power Switches*	ABB 5SNA1500E330305

Simulation results for the modulation of j = 4 and k = 5 are demonstrated in Fig. 7. From the circuit parameters in Table I, the positive and negative resonant frequency are 2.6 kHz and 2.9 kHz respectively, so, for the best overall efficiency, the switching frequency is chosen as 550 Hz and effective frequency is 2.75 kHz. Fig. 7(a) and Fig. 7(b) shows that the capacitor of SM_1 is inserted into the stack for 90% of the switching cycle before being bypassed for the remaining 10%, which is one of the five positive stages in one switching cycle. The SM capacitors participate in the resonance with L_r and thus assist all the SM IGBTs achieve the soft-switching operation. In Fig. 7(c), all the SM capacitor voltages are inherently well-balanced without any extra control. Lastly, it can be derived from Fig. 7(d) that the transformer voltage on the secondary side is ±1.11 kV and the value of V_L is 1.11 kV in this modulation. Additionally, the dc current through the transformer (green line), shown in Fig. 7(d), is much smaller than the amplitude of ac component.

Results for reverse power flow are shown in Fig. 7(e) and Fig. 7(f). The current direction has reversed but the operating principles are the same as for the results in positive power flow. Then, the SM number in the positive and negative stage are adjusted to 4 and 3 respectively (j = 3 and k = 4) and the simulation results are shown in Fig. 8. Since there are only 4 active SMs resonating with L_r in one switching cycle, the switching frequency is set at 600 Hz to match the range of resonant frequencies. In Fig. 8(a), SM_1 is operated as the active SM in this switching cycle and participates in the resonance. It is inserted into the stack for a duty-cycle of 87.5% and removed from the stack when its upper switch voltage is high. All these five SMs take turns to be the redundancy, which is bypassed in the whole specific switching cycle and the capacitor voltage keeps a constant value. It can be observed from Fig. 8(b) that SM_4 (purple line) is operated as the redundant SM in the whole first switching cycle and SM_5 (green line) replaces it when time goes to 1.7 ms. From Fig. 8(a) and Fig. 8(b), the soft-switching and inherent balancing are still achieved, and the value of V_L is increased to 1.43 kV shown in Fig. 8 (c). The step-ratio of this converter can be further extended to 4/1 with the safety margin for the selected power devices in Table I.

To demonstrate low step-ratio ($1 < R < 2$) but high-power throughput (P>2.5 MW) conversion, the front-to-front converter, shown in Fig. 5(a), is configured for 20 kV to 15 kV conversion

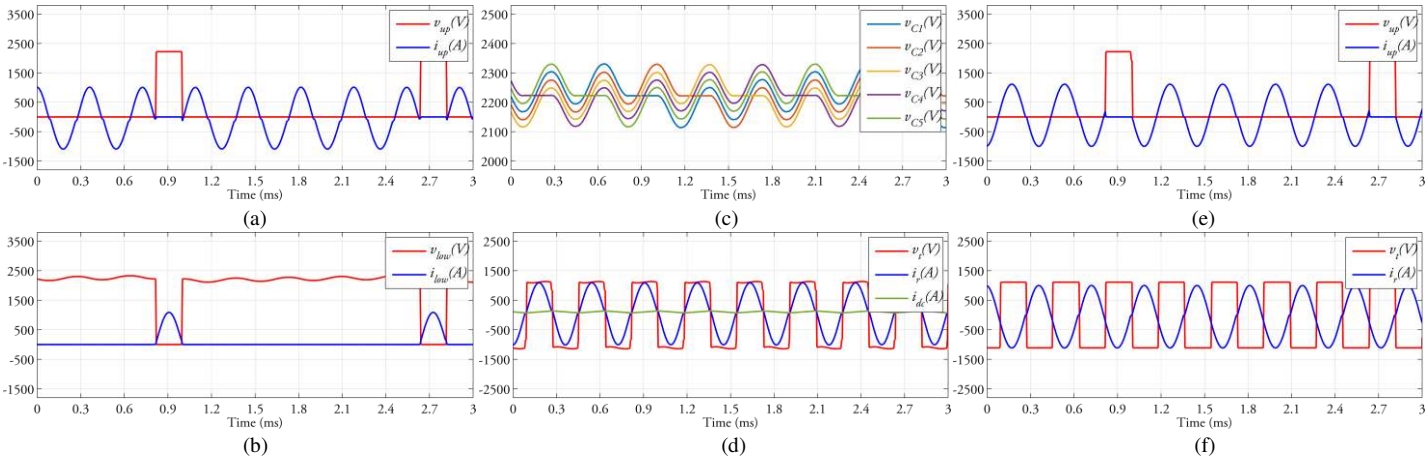

Fig. 7. Simulation results for the modulation of j = 4 and k = 5 of the isolated RMMC. (a) Voltage and current of the upper switch in SM_1. (b) Voltage and current of the lower switch in SM_1. (c) SM capacitor voltages. (d) Voltage and current across the transformer. (e) Voltage and current of the upper switch in SM_1 for reverse power flow. (f) Voltage and current across the transformer for reverse power flow.

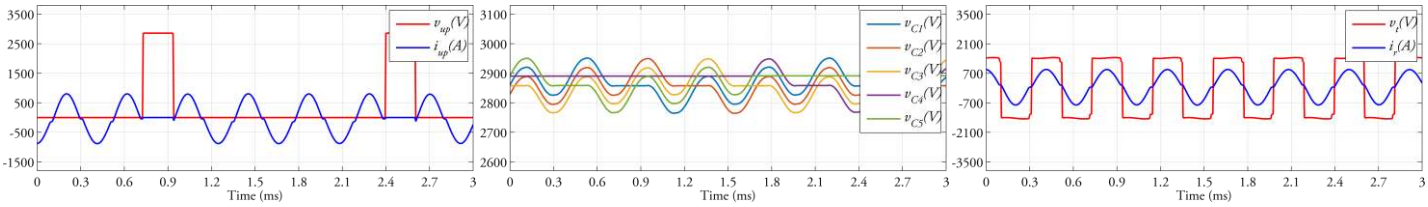

Fig. 8. Simulation results for the modulation of j = 3 and k = 4 of the isolated RMMC. (a) Voltage and current of the upper switch in SM_1. (b) SM capacitor voltages. (c) Voltage and current across the transformer.

at 3 MW. This is illustrative of a dc transformer connecting two MVDC links of similar but not identical voltage. The RMMC stacks have the same circuit parameters as Table I but with 5% variations to simulate the tolerances of the resonant inductance and SM capacitance. Each stack is operated individually as a single RMMC. The switching sequence for stack 1 (stack 5) and stack 4 (stack 8) keeps a $\pi/5$ difference with the sequence for stack 2 (stack 6) and stack 3 (stack 7). This can be observed by the waveform shift of the corresponding SM capacitor voltages in Fig. 9(a) and Fig. 9(b), and all of the SM capacitor voltages are still inherently balanced in this configuration. Fig. 9(c) shows that the power is four times greater than the single circuit operation shown in Fig. 7(d), and the input current (green line) on the primary side comprises only a steady dc component.

The parallel-series configuration, shown in Fig. 5(b), aims to achieve high-power and very high step-ratio (R>15) conversion which will be required to interface the MVDC network and LVDC network in dc grids. The simulation results with a four-module configuration are shown in Fig. 10. The first two modules are paralleled as the first pair and the last two modules are paralleled as the second pair. First, the current and voltage on each module are inherently balanced, which can be observed in Fig. 10(a)–Fig. 10(d). Further, the phase-shift within each pair is $\pi/5$ and it can be found in the individual transformer waveforms comparing Fig. 10(a) and Fig. 10(b) or Fig. 10(c) and Fig. 10(d). It contributes to the neutralization of the resonant current ripple on the high-voltage link capacitors and the comparison results are given in Fig. 10(e). The switching sequences for these two pairs have a $\pi/10$ difference, shown in Fig. 10(a) and Fig. 10(c) or Fig. 10(b) and Fig. 10(d), and this alleviates the current ripple on the low-voltage side filters, as illustrated in Fig. 10(f). This four-module example is designed for a 3 MW dc-dc conversion from 20 kV to 1.11 kV, and the module number can be flexibly configured following the analysis in Section III-C to satisfy a wide variety of connection requirements for future MVDC grids.

V. Experiment Results Analysis

To verify the theoretical analysis and simulation results, a down-scaled isolated RMMC prototype with five SMs was built with the parameters given in Table II.

Table II Experimental Parameters of the Isolated RMMC

Symbol	Description	Value
P	*Rated Power*	1.5 kW
V_H	*High-side Link Voltage*	400 V
V_L	*Low-side Link Voltage*	42 V–266 V
r_T	*Turns Ratio*	1/1
L_r	*Resonant Inductor*	208 μH
N_l	*SM Number*	5
f_s	*Switching Frequency*	500–900 Hz
C_1	*SM_1 Capacitor*	46.5 μF
C_2	*SM_2 Capacitor*	47.3 μF
C_3	*SM_3 Capacitor*	46.2 μF
C_4	*SM_4 Capacitor*	47.8 μF
C_5	*SM_5 Capacitor*	47.1 μF
C_H C_L	*DC Capacitor*	220 μF
S	*Power Modules*	Infineon FF150R12ME3G

Experimental results for the modulation of j = 4 and k = 5 are shown in Fig. 11(a) and Fig. 11(b). The circuit parameters indicate resonant frequencies in the positive stage and negative stage of 3.2 kHz and 3.6 kHz respectively. The switching frequency is set at 700 Hz giving an effective frequency of 3.5 kHz. Fig. 11(a) shows that zero-crossing of the resonant current

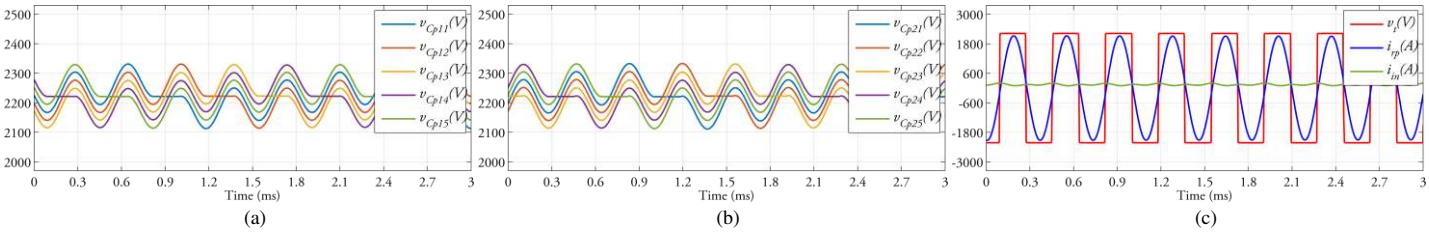

Fig. 9. Simulation results of the front-to-front configuration. (a) SM capacitor voltages of stack 1. (b) SM capacitor voltages of stack 2. (c) Voltage and current across the transformer and the input current.

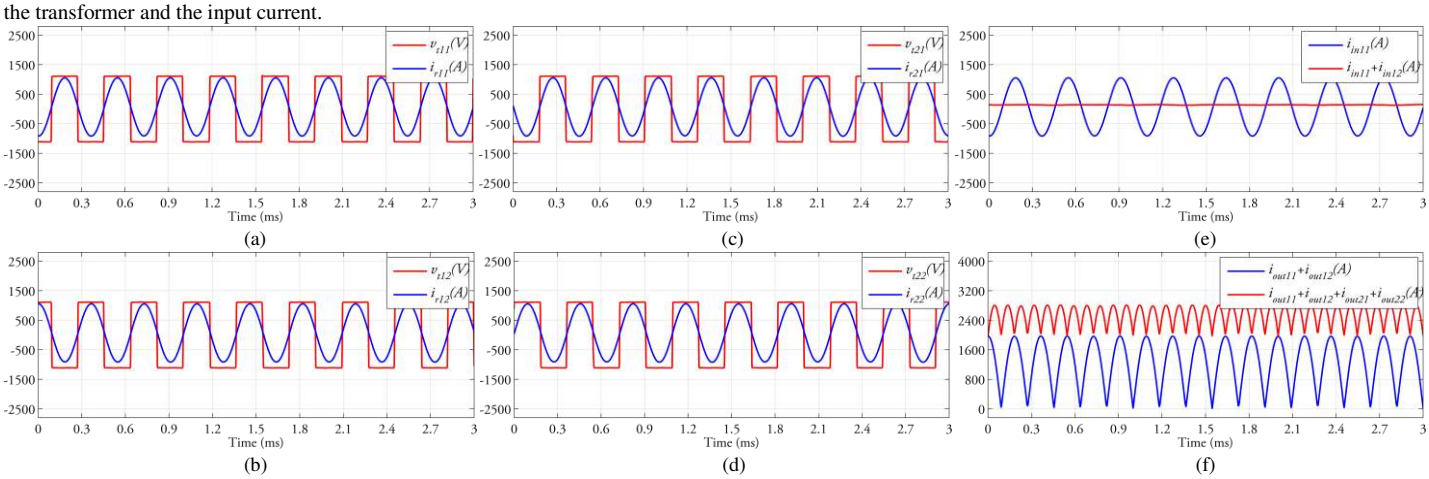

Fig. 10. Simulation results of the parallel-series configuration. (a) Voltage and current across the transformer T_{11}. (b) Voltage and current across the transformer T_{12}. (c) Voltage and current across the transformer T_{21}. (d) Voltage and current across the transformer T_{22}. (e) Comparison of the input current for one module and input current for one pair. (f) Comparison of the output current for one pair and output current for all pairs.

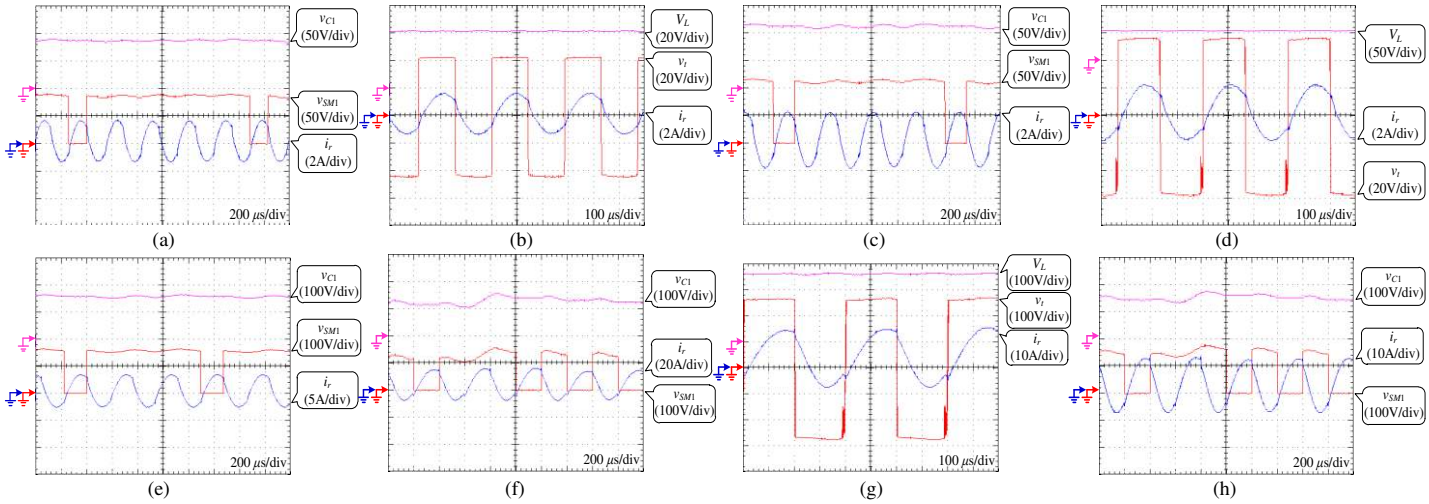

Fig. 11. Experimental results of SM_1 capacitor voltage V_{C1}, sub-module voltage V_{SM1}, resonant current i_r, transformer voltage v_t, and low-side link voltage V_L of the isolated RMMC. (a)(b) $j = 4$ and $k = 5$. (c)(d) $j = 3$ and $k = 4$. (e) $j = 2$ and $k = 3$. (f)(g) $j = 1$ and $k = 5$. (h) $j = 1$ and $k = 4$.

is always after the step-change of SM voltage, meaning that the current flows in the anti-paralleled diodes of the SM switches during each turn-on operation and soft-switching is thereby achieved. It is shown in Fig. 11(a) and Fig. 11(b) that the SM capacitor voltage is inherently balanced at about 85 V and the value of V_L is 42 V under this modulation.

To illustrate the flexible nature of the modulation scheme, results for $j = 3$, $k = 4$ and $j = 2$, $k = 3$ are shown in Fig. 11(c)(d) and Fig. 11(e) respectively. With $j = 3$ and $k = 4$, the resonant frequencies are 2.8 kHz and 3.2 kHz respectively, so the switching frequency and effective frequency are chosen at 750 Hz and 3.0 kHz. It can be observed from Fig. 11(c) and Fig. 11(d) that the SM switches still achieves soft-switching operation. The SM capacitor voltages are balanced at 110 V and the V_L is equal to 55 V. When the modulation is changed to $j = 2$ and $k = 3$, the switching frequency is designed at 930 Hz since only three SMs participate in the resonance in each switching cycle (the other two SMs are bypassed as redundancy). Fig. 11(e) shows that all the operational benefits remain and the SM capacitor voltages are balanced at 158 V. These experimental results verify the theoretical analysis and simulations in Section II and IV.

Lastly, to demonstrate the possibility for low step-ratio conversion, the experimental results with the modulation of $j = 1$, $k = 5$ and $j = 1$, $k = 4$ are given in Fig. 11(f)(g) and Fig. 11(h) respectively. The switching frequency is set at 500 Hz and 750 Hz to match the range of resonant frequencies. As the results show, the inherent balancing capability and soft-switching operation still exist in this low step-ratio conversion. The SM

voltages are balanced at 131 V and 158 V, and V_L extends to 263 V and 238 V respectively.

VI. Conclusion

An isolated resonant mode modular converter (RMMC) with flexible modulation and assorted configurations has been presented that is able to satisfy a wide variety of interface requirements for MVDC networks. The new RMMC approach inherits from the transformer-less RMMC the beneficial features of inherent SM voltage-balancing and soft-switching, and provides galvanic isolation and bidirectional power flow between the high-voltage link and low-voltage sides. Further, with the flexible modulation scheme, the step-ratio of this isolated RMMC is significantly extended from a limited range around a nominal conversion ratio to a much wider range. Moreover, to overcome the current limitation in single circuit operation and expand the power rating for wider application areas, this converter is employed as building block for variety of configurations. This has been illustrated with a front-to-front and a parallel-series configuration as examples of derived converters covering the high power rating conversion for very low or very high step-ratio application. The theoretical analysis has been verified against full-scale simulations of example converters and further verified against tests on a down-scaled experimental converter. The results demonstrate that this isolated RMMC, and its derivatives, have good potential for operation as flexible dc taps or as dc transformers in future MVDC grids.

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