A Tunable Passband Logarithmic Photodetector for IoT Smart Dusts

Jingjing Liu, Grahame Faulkner, Bhaskar Choubey, *Member IEEE*, Steve Collins, *Member IEEE* and Dominic C. O'Brien, *Member IEEE*

***Abstract*—This paper presents a tunable passband low-power logarithmic photodetector for IoT smart dusts using optical wireless communications. The photodetector can selectively receive optical signals and filter out unwanted optical noise. All the transistors work in the subthreshold region. Each transistor and circuit pole is designed based on theoretical analysis. The output of the photodetector is independent of the absolute illumination intensity and proportional to the modulation depth of the intensity. The photodetector requires a giga-ohm resistor, which is realized by a Gm circuit with an extreme low bias current. The Gm bias voltage can be used to tune the lower cut-off frequency of the passband. The upper cut-off frequency is determined by the photodetector bias and illumination intensity. The photodetector was fabricated using a standard 0.25µm CMOS process and tested under different illumination intensities of 830nm laser. Measurement results showed that the lower cut-off frequency increases as Gm bias and the minimum is approximately 100Hz when Gm bias is 0V. The photodetector output and Gm DC offset matches with theoretical analysis.**

***Index Terms*—Internet of Things, smart dusts, logarithmic photodetector, subthreshold, optical wireless communications.**

I. Introduction

The Internet of Things (IoT) draws more and more attentions due to its broad applications, such as environment monitoring, agriculture monitoring, traffic control, healthcare, and logistics management. IoTs using optical communications offer low-power advantage and enable small size of sensor nodes compared to RF communications. When a sensor node integrates self-contained sensing and communication system into a cubic-millimetre mote, it is called "Smart Dust". A key component of an optical smart dust is photodetector. There are three main types of CMOS photodetectors and they are passive photodetector, linear active photodetector and logarithmic photodetector. The passive photodetector consists of a P-N junction photodiode and a pass transistor [1-3]. The major problem of passive photodetectors is high noise because the accumulated signal charges are directly transferred through the pass transistor to the outside of the photodetector and therefore thermal noise has a big effect on the performance [4]. A photodetector with an active amplifier or buffer is referred to as an active photodetector. Linear active photodetectors can effectively reduce the noise compared to the passive photodetectors because the accumulated signal charges are converted to a gate voltage of a transistor and this voltage is transferred to the outside of the photodetector by an amplifier. The linear active photodetectors are widely used [5–9]. However, linear photodetectors have a low dynamic range. Large dynamic range can be achieved by logarithmic photodetectors [10–13], whose output signals are proportional to the logarithm of the input optical signal intensity. Oxford developed an optical smart dust system using logarithmic photodetectors [14, 15]. Logarithmic photodetectors can generate an electrical signal directly related to the contrast ratio of the light modulation. This feature is important because smart dusts can be at an unknown distance from base station and this means the beam intensity received by smart dusts varies with the distance. However, if the contrast ratio of the beam modulation is fixed, logarithmic photodetectors can generate a constant voltage output. A tunable passband photodetector is needed for optical wireless communications because it can selectively receive optical signals and filter out unwanted optical noise. This feature becomes important as visible light communications (VLC) technology will introduce many different optical signals in space. This paper presents a tunable passband low-power logarithmic photodetector based on the requirement of Oxford smart dust system and is organized as follows. Section II discusses the theoretical analysis and the design of the photodetector. Measurement results are shown in Section III and Section IV gives the conclusions of the paper.

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II. Tunable Passband Logarithmic Photodetector

A logarithmic detector circuit originally proposed by Mahowald [16] and studied further by Delbrück [17] is shown in Fig. 1. The photodiode is illuminated by an optical beam and generates such a small photocurrent that M_1 stays in the subthreshold region of operation. If the beam intensity is modulated, the generated photocurrent includes a DC component I_{ph} and an ac small signal i_{ph}. A small increase in the photocurrent tries to pull down V_1. This causes V_2 to increase significantly due to the inverting amplifier formed by M_2 and

M_3. The output change is coupled back to the gate of M_1 through capacitors and this causes V_3 to increase. This increase of V_3 pulls up V_1 and therefore the circuit is stable. The feedforward elements consist of the photodiode, M_2, M_3 and the source of M_1. The feedback elements consist of the capacitive divider, resistor R and the gate of M_1. The dominant noise in the photodetector is caused by the electron fluctuations in the photodiode and the total noise is a constant independent of illumination intensity [17].

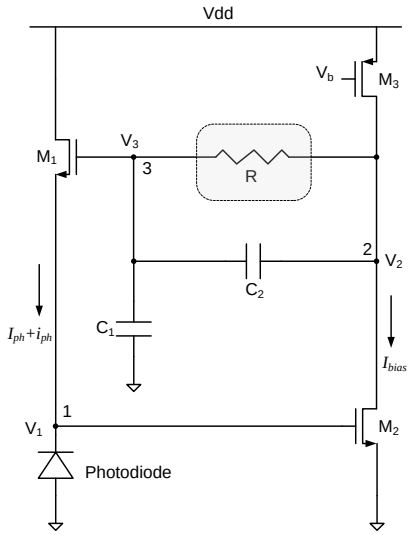


Fig. 1 Schematic diagram of a logarithmic photodetector.

A. AC analysis of the logarithmic photodetector

The photocurrent consisting of a DC component I_{ph} and an ac small signal i_{ph} flows through M_1. If $(\kappa_n v_3 - v_1) << V_T$, i_{ph} can be approximated to be

$$i_{ph} = \frac{I_{ph}}{V_T}(\kappa_n v_3 - v_1) \tag{1}$$

where v_1 and v_3 represent the small voltages caused by i_{ph} at node 1 and node 3 respectively, V_T is thermal voltage and κ_n is the capacitive coupling ratio from gate to channel of NMOS transistors. M_2 is a common-source amplifier in the feedforward path of the circuit and M_3 is the active load of M_2. The amplifier gain is

$$G_{forward} = \frac{\kappa_n}{V_T(\lambda_2 + \lambda_3)} \tag{2}$$

where λ is a function of channel length. For the RC feedback in Fig. 2, we can get

$$\frac{v_2}{v_3} = \frac{1 + sR(C_1 + C_2)}{1 + sRC_2} \approx \frac{C_1 + C_2}{C_2} \tag{3}$$

The time constants RC_2 and $R(C_1+C_2)$ should be large enough to dominate the numerator and denominator at the working frequency. In other words, the RC circuit is designed in such a way that v_3 cannot directly affect node 2 through R, but is coupled through C_1 and C_2. In this case, the large time constant and small capacitance makes the R value very large. Actually the R is regarded as open circuit to the small signal. In Fig. 1, it can be seen that v_1 is amplified by the amplifier formed by M_2 and M_3. Because the amplifier gain is much larger than the capacitance ratio, v_1 is much smaller than v_3.

$$v_1 = \frac{v_2}{G_{forward}} = \frac{v_3(C_1 + C_2)/C_2}{G_{forward}} << v_3 \tag{4}$$

So equation (1) can be simplified as,

$$\frac{v_3 / V_T}{i_{ph} / I_{ph}} = \frac{1}{\kappa_n} \tag{5}$$

Based on (3) and (5), the normalized photodetector gain is

$$G_{\text{detector}} = \frac{v_2 / V_T}{i_{ph} / I_{ph}} = \frac{1}{\kappa_n} \times \frac{C_1 + C_2}{C_2} \tag{6}$$

which is the same as the one in [17]. The denominator is the beam modulation depth that will be fixed, so the small signal output v_2 will be a constant and independent to the absolute illumination intensity. The feedback gain is approximately equal to the inverse of closed loop gain.

$$G_{feedback} = \frac{C_2 \kappa_n}{C_1 + C_2} \tag{7}$$

The loop gain of the photodetector is

$$G_{loop} = G_{forward} G_{feedback} = \frac{\kappa_n^2 C_2}{V_T(\lambda_2 + \lambda_3)(C_1 + C_2)} \tag{8}$$

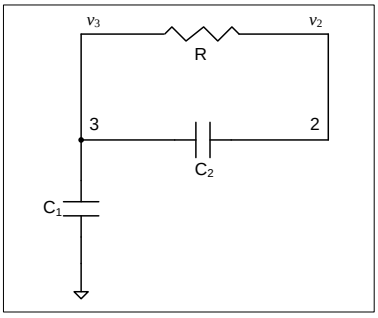


Fig. 2 The feedback part of the photodetector.

To obtain the frequency response of the photodetector transfer function, the poles and zeros need to be analyzed. Fig. 3 shows the schematic circuit diagram of the photodetector with parasitic capacitances. There are 3 nodes and each node has a pole. In addition, there is also a zero in the feedback path. The magnitude of pole 1 is

$$\omega_1 = \frac{(1 + G_{loop})(I_{ph} / V_T)}{C_{pd} + G_{forward} C_{gd2} + (G_{loop} / \kappa_n) C_{gs1}} \tag{9}$$

where C_{pd} is the photodiode capacitance, C_{gd2} is the M_2 gate-drain capacitance, C_{gs1} is the M_1 gate-source capacitance. The open loop input conductance of the photodetector is the source conductance of M_1, which is I_{ph}/V_T. So the closed loop conductance at the node 1 should be I_{ph}/V_T multiplied by the $(1+G_{loop})$ due to the shunt-shunt feedback. The first term in the denominator C_{pd} is in the order of a pico-Farad. The second and third terms are obtained by considering the Miller effect. C_{gd2} and C_{gs1} are both in the order of a femto-Farad. Although they are amplified, they are still much smaller than C_{pd}. So equation (9) is approximately reduced to

$$\omega_1 \approx \frac{(1+G_{loop})I_{ph}}{C_{pd}V_T} \tag{10}$$

The magnitude of pole 2 is

$$\omega_2 \approx \frac{(\lambda_2+\lambda_3)I_{bias}}{C_{node2}} \tag{11}$$

where C_{node2} is the total capacitance and resistance at the node 2. Equation (11) indicates that the pole 2 is dependent on the bias current, so V_b can be used to tune the upper limit of passband.

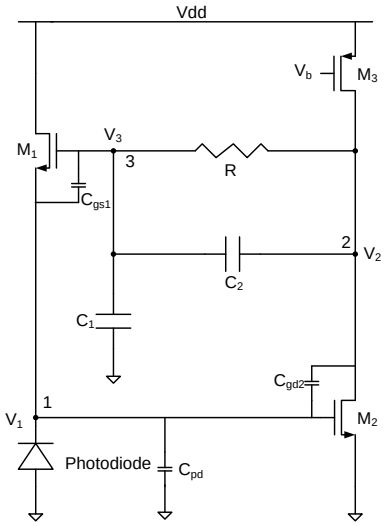


Fig. 3 Schematic of the photodetector with parasitic capacitance.

Now including the two poles, the feedforward gain becomes

$$G_{forward}'(s) = \frac{G_{forward}}{(1+s/\omega_1)(1+s/\omega_2)} \tag{12}$$

From equations (3), (6) and (7), the feedback gain is

$$G_{feedback}'(s) = \frac{\kappa_n(1+s/\omega_3)}{1+s/\omega_4} \tag{13}$$

where $\omega_3 = \frac{1}{RC_2}$, $\omega_4 = \frac{1}{R(C_1+C_2)}$.

The closed loop transfer function of the photodetector is

$$H(s) = \frac{G_{forward}'(s)}{1+G_{forward}'(s)G_{feedback}'(s)} \approx \frac{(1+s/\omega_4)/\kappa_n}{1+s/\omega_3+(1+s/\omega_1)(1+s/\omega_2)(1+s/\omega_4)/(\kappa_n G_{forward})} \tag{14}$$

It should be noted that (14) is different from the closed loop transfer function in [17]. Equation (14) shows the photodetector is a one-zero three-pole system and is more accurate to describe the working mechanism of the circuit. In (14), ω_4 is a zero and ω_3 is another pole. Since $\omega_4 < \omega_3$, the zero is at a lower frequency than the pole 3. The Bode plot of the transfer function is shown in Fig. 4. At very low frequencies, $2\pi f < \omega_4$, the gain of the photodetector is simply $1/\kappa_n$. In this case, there is no effect of the zero to the gain. This is equivalent to taking out R, C_1 and C_2 from the circuit shown in Fig. 1 and shorting V_3 to V_2. The gain in this frequency range has been shown in equation (5). At mid-band frequencies, $\omega_3 < 2\pi f < \omega_2$, the third term in the denominator is small due to the large value of $\kappa_n G_{forward}$ and can be ignored. Moreover, s/ω_3 and s/ω_4 are much larger than 1. So the transfer function is reduced to equation (6). At high frequency, $2\pi f > \omega_2$, the gain starts to drop and the pole causes the gain to drop by 20dB/dec. When $2\pi f > \omega_1$, the slope becomes -40dB/dec. In order to obtain a large bandwidth, the zero and pole 3 should be at very low frequency. The pole 1 and pole 2 determine the upper cut-off frequency of the photodetector.

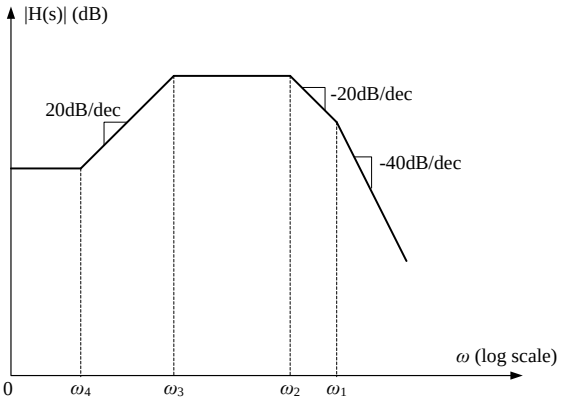


Fig. 4 Bode plot of the closed-loop transfer function.

B. Logarithmic photodetector design

The logarithmic photodetector is designed to receive 830nm optical signal using a standard 0.25μm CMOS process. The photodiode in the photodetector is a deep junction diode (N-well/P-sub) for its high quantum efficiency and its size is 7500 μm^2. In order to save power, the target of the maximum working frequency is 10kHz under 1V voltage supply. This means that pole 2 should be at least equal to 10kHz. Because the voltage gain of the one-stage amplifier has a maximal value of 40dB in a typical CMOS process [18], the unity-gain frequency of the amplifier formed by M_2 and M_3 would be 1MHz.

$$f_T = \frac{g_{m2}}{2\pi C_{node2}} = \frac{\kappa_n I_{bias}}{2\pi V_T C_{node2}} \tag{15}$$

where C_{node2} is approximately equal to the sum of C_2 and the load capacitance. The capacitance ratio (C_1/C_2) determines the photodetector gain and ideally should be large. However, a large C_1 means a large area. So the ratio was chosen as 10. C_2 is preferred to be small in order to make pole 2 frequency large. Therefore the capacitances of C_1 and C_2 are set to approximate 100fF and 10fF respectively. These two capacitors are realized by MIMCAPs. The actual C_1 is 20μm by 5μm with the capacitance of 104fF and the actual C_2 is 5μm by 2μm with the capacitance of 11fF. Assuming the photodetector output drives a 5μm^2 transistor with gate oxide capacitance 5fF/μm^2, C_{node2} would be approximately 35fF. Rearranging (15), the bias current is

$$I_{bias} = \frac{2\pi V_T C_{node2} f_T}{\kappa_n} \approx 7.7nA \tag{16}$$

where f_T = 1MHz, V_T = 25.9mV, C_{node2} = 35fF, and κ_n is 0.74.

To save power, a bias current of 5nA was set as the target. M_3 is set to 2.5μm/1μm with 0.6V bias voltage and provides 4.76nA bias current. The geometry of M_2 is 2μm/1μm to ensure that M_3 and M_2 are in the subthreshold region.

Pole 1 is proportional to the photocurrent I_{ph} and therefore moves when the photocurrent changes. This means that the minimum detectable photocurrent is determined by placing pole 1 at 10 kHz.

$$\omega_1 \approx \frac{(1+G_{loop})I_{ph}}{C_{pd}V_T} = \frac{(1+G_{loop})I_{ph0}}{C_{pd0}V_T} \quad (17)$$

where C_{pd0} is the unit area capacitance of the photodiode and I_{ph0} is photocurrent generated per unit area in the photodiode. These two parameters are fixed by the CMOS process. G_{loop} is the only parameter which can be controlled. With a capacitance ratio (C_1 /C_2) of 10 and $G_{forward}$ of 40dB, the loop gain of the photodetector is

$$G_{loop} = G_{forward}G_{feedback} = 100 \times \frac{\kappa_n C_2}{(C_1 + C_2)} \approx 10 \quad (18)$$

As a result, in order to put pole 1 at 10 kHz, the minimum detectable photocurrent I_{ph} for the photodiode can be calculated to be

$$I_{ph} = \frac{2\pi f C_{pd} V_T}{1+G_{loop}} \approx 250\text{pA} \quad (19)$$

where C_{pd} is approximately 1.6pF.

The transistor size of M_1 must be chosen to ensure that it stays in the subthreshold region over a large photocurrent range. This requires M_1 has a large W_1/L_1 ratio. Therefore L_1 is set to 0.24μm, which is the minimum length of a transistor in this CMOS process. Fig. 5 shows the simulation results of the DC output voltage (V_2) versus photocurrent for four different M_1 widths. Note that the x-axis is a logarithmic scale, so the straight line portion means M_1 is in the subthreshold region. In order to achieve a large dynamic range, the width of M_1 is set to 30μm. The point A indicates the minimum detectable photocurrent and the point B is approximately 4 decades of photocurrent.

Pole 3 determines the lower limit of the passband and should be at least 10 times smaller than pole 2, so the maximum frequency of pole 3 is 1 kHz. Then the minimum resistance of R can be estimated from (13).

$$R_{\min} = \frac{1}{2\pi f C_2} \approx 16G\Omega \quad (20)$$

The photodetector gain can be determined from these capacitor values.

$$G_{\text{detector}} = \frac{v_2/V_T}{i_{ph}/I_{ph}} = \frac{1}{\kappa_n} \times \frac{C_1+C_2}{C_2} \approx 14.0 \quad (21)$$

The i_{ph}/I_{ph} is the modulation depth and is set to 20%, and then the small signal output v_2 can be estimated by (22).

$$v_2 = V_T \times \frac{i_{ph}}{I_{ph}} \times 14.0 \approx 72.5\text{mV} \quad (22)$$

All the design parameters are summarized in Table I. It should be noted that these values are determined based on the

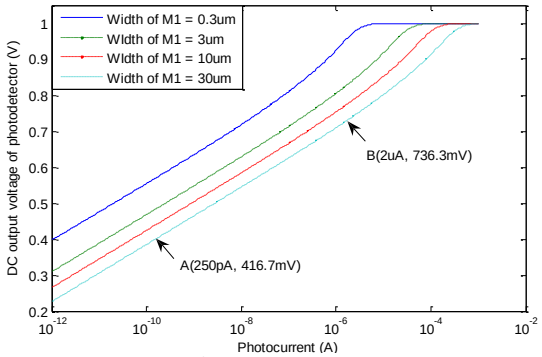


Fig. 5 Simulation results of the DC output voltage (V_2) vs. photocurrent for four different M_1 widths.

smart dust system requirement. In other applications, power may not be such stringent. The methology can be used to design each parameter based on new requirements.

It is important to ensure the stability of the photodetector. The Laplace transform of the loop gain is shown in (23).

$$G_{loop}'(s) = \frac{\kappa_n^2(1+s/\omega_3)}{V_T(\lambda_2+\lambda_3)(1+s/\omega_1)(1+s/\omega_2)(1+s/\omega_4)} \quad (23)$$

The DC gain is less than 40dB. We regard it as 40dB for

Table I Design parameters of the photodetector.

M_1 W/L (μm)	Min. I_{ph} (pA)	C_1 (fF)	R (GΩ)	I_{bias} (nA)
30/0.24	250	104	16	4.76
M_2 W/L (μm)	Max. I_{ph} (μA)	C_2 (fF)	v_2 (mV)	V_{dd} (V)
2/1	2	11	72.5	1
M_3 W/L (μm)	Diode C (pF)	V_{b1} (V)	Dyn.range	i_{ph}/I_{ph}
2.5/1	1.6	0.6	4 decades	20%

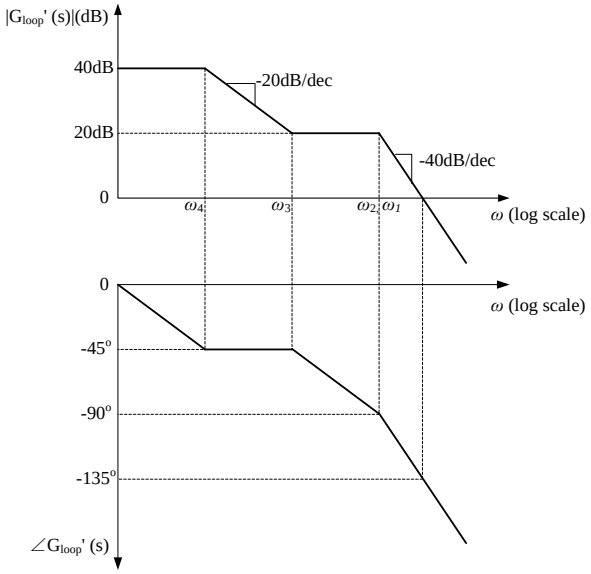


Fig. 6 The bode plot of the photodetector loop gain. The phase margin is 45° in the worst condition.

simplicity. ω_1 varies with photocurrent. In the worst case, ω_1 coincides with ω_2. The bode plot of the loop gain is shown in Fig. 6. In the photodetector design, ω_4, ω_3 and ω_2 are separated by one decade each other. The effects of pole ω_4 and zero ω_3 are cancelled. Therefore the phase shift caused by them is zero at

ω_2 and the magnitude becomes 20dB after ω_3. Since ω_1 and ω_2 coincide, the magnitude slope and phase becomes -40dB/dec and -90° respectively at ω_1 and ω_2. So the phase margin is 45° and the photodetector is stable in the worst condition.

C. High impedance element

A minimum resistance of 16GΩ is required for the R highlighted in Fig. 1. However, for analog VLSI circuits, it cannot be realized by true ohmic resistors available in a CMOS process. [17] proposed a resistor-like device which is a PMOS with its gate connected to node 3 and its body connected to node 2. This device can provide large enough resistance and make the lower limit of the passband less than 10Hz, which cannot be changed. The fixed lower limit of passband at such a low frequency causes the photodetector receive lots of optical noises, such as 50Hz optical noise generated by the lighting system. A differential transconductance amplifier, Gm, can be used to generate an equivalent resistance which can be controlled. The schematic diagram of Gm circuit is shown in Fig. 7 (a). All the transistors work in the subthreshold region. The output current is given by

$$I_{out} = I_b \tanh\left(\frac{\kappa_n}{2V_T}(V_+ - V_-)\right) \tag{24}$$

where I_b is the bias current in M_1. For small differential voltages, the output current is approximately to be,

$$I_{out} \approx \frac{I_b \kappa_n}{2V_T}(V_+ - V_-) \tag{25}$$

Rearranging (25), an equivalent resistance of the differential amplifier is obtained. If I_b is very small, a very large equivalent resistance can be realized. Equation (26) indicates that varying I_b can change the resistance, therefore tune the lower limit of the passband.

$$\frac{V_+ - V_-}{I_{out}} = \frac{2V_T}{I_b \kappa_n} = R_{equivalent} \tag{26}$$

Fig. 7 (b) shows the connection of Gm in Fig. 1. It should be noted that Gm circuit is not a resistor and the connection cannot be swapped. In the photodetector, the feedback signal flows from node 2 to node 3 and goes through a high resistance R. The Gm can generates a high equivalent resistance $R_{equivalent}$ from V_2 to V_3 in this connection. So it can replace the R. To generate 16GΩ resistance, the tail current of the Gm element should be 4.3pA. The bias voltage and W/L of M_1 are 0.1V and 1.5μm/1μm respectively. These parameters give the tail current I_b of 8.6pA. In this case, the lower limit of passband is approximately at 1.6kHz.

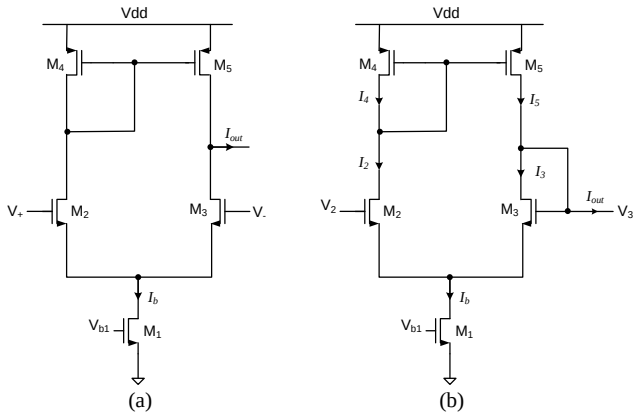


Fig. 7 (a) Differential transconductance amplifier, (b) Gm circuit as the high impedance element R in the photodetector.

The sizes of $M_2 - M_5$ can be determined by the DC offset of the Gm circuit. M_2 and M_3 are identical and preferably small to reduce parasitic capacitance loading on the photodetector. M_4 and M_5 have to be small enough not to slow down the circuit response, but big enough not to introduce large offsets. The offset is analyzed using the Vittoz CMOS model for the subthreshold mode [19, 20].

$$I_D = K\beta V_T^{\,2} \exp\left(\frac{V_G - V_{TH0} - nV_S}{nV_T}\right) \tag{27}$$

where $\beta = \mu C_{ox} W/L$, n is slope factor in subthreshold region and equal to $1/\kappa$, V_{TH0} is gate threshold voltage for source voltage $V_S = 0$. K is a factor larger than 1, which connects weak inversion (subthreshold) and strong inversion (above threshold). The slope factor n may be considered as a constant for transistors biased by similar values of V_S. The random variables in (27) are β and V_{TH0}. Assuming β and V_{TH0} have no correlations, the standard deviation in I_D can be derived explicitly as a function of the standard deviations in β and V_{TH0}.

$$\frac{\sigma_{I_D}^2}{I_D^2} = \left(\frac{\partial \ln I_D}{\partial \beta}\right)^2 \sigma_\beta^2 + \left(\frac{\partial \ln I_D}{\partial V_{TH0}}\right)^2 \sigma_{V_{TH0}}^2 \tag{28}$$

Substituting (27) into (28) leads to (29). From the CMOS process data, it is known that the first term is much smaller than the second term, so it is ignored.

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{\sigma_\beta^2}{\beta^2} + \left(\frac{\kappa}{V_T}\right)^2 \sigma_{V_{TH0}}^2 \approx \left(\frac{\kappa}{V_T}\right)^2 \sigma_{V_{TH0}}^2 \tag{29}$$

Now we can calculate the input referred offset voltage V_{OS} between V_2 and V_3. In the common mode, M_2 and M_3 ideally should have the same gate voltage and source voltage, therefore the same drain current, I_D. However, due to the variation of threshold voltages, the mismatch of I_2 and I_3 is given by

$$\frac{\sigma_{I_{D23}}^2}{I_D^2} = \left(\frac{\kappa_n}{V_T}\right)^2 \sigma_{Vtn}^2 \tag{30}$$

where σ_{Vtn} is the standard deviation of NMOS threshold voltage. The M_2 drain current I_2 is equal to M_4 drain current I_4. M_4 and M_5 form a current mirror and ideally I_4 and I_5 are both equal to I_D. However, due to the variation of threshold voltages, the mismatch of I_4 and I_5 is given by

$$\frac{\sigma_{I_{D45}}^2}{I_D^2} = \left(\frac{\kappa_p}{V_T}\right)^2 \sigma_{Vtp}^2 \tag{31}$$

where σ_{Vtp} is the standard deviation of PMOS threshold voltage. Because the M_2/M_3 pair and M_4/M_5 pair have no correlations, the mismatch between I_3 and I_5 is given by,

$$\frac{\sigma_{I_{D35}}^2}{I_D^2} = \left(\frac{\kappa_n}{V_T}\right)^2 \sigma_{Vtn}^2 + \left(\frac{\kappa_p}{V_T}\right)^2 \sigma_{Vtp}^2 \tag{32}$$

In order to balance the mismatch of I_3 and I_5, an additional voltage should be applied to the input, which is the input referred offset voltage V_{OS} of the Gm element. The standard

deviation of V_{OS} is given by

$$\sigma_{Vos} = \frac{\sigma_{I_{D35}} / I_D}{g_m / I_D} = \sqrt{\left(\sigma_{Vtn}^2 + \left(\frac{\kappa_p}{\kappa_n}\right)^2 \sigma_{Vtp}^2\right)} \quad (33)$$

where g_m is the transconductance of M_2, $g_m = \kappa_n I_D / V_T$. From simulation results, κ_n and κ_p are estimated as 0.80 and 0.79 respectively. Moreover, the CMOS process gives empirical formulae for NMOS and PMOS threshold voltage standard deviation.

$$\sigma_{Vtn} = \frac{5.2}{\sqrt{W_n L_n}}, \ \sigma_{Vtp} = \frac{4.8}{\sqrt{W_p L_p}} \quad (34)$$

where W_n /W_p and L_n /L_p are width and length of NMOS/PMOS with units of microns. σ_{Vtn} and σ_{Vtp} have the units of milli-volts. By substituting (34) into (33), the standard deviation of the input referred offset voltage as a function of the size of transistors can be derived.

$$\sigma_{Vos} = \sqrt{\left(\frac{5.2^2}{W_n L_n} + \left(\frac{0.79}{0.80}\right)^2 \frac{4.8^2}{W_p L_p}\right)} \quad (35)$$

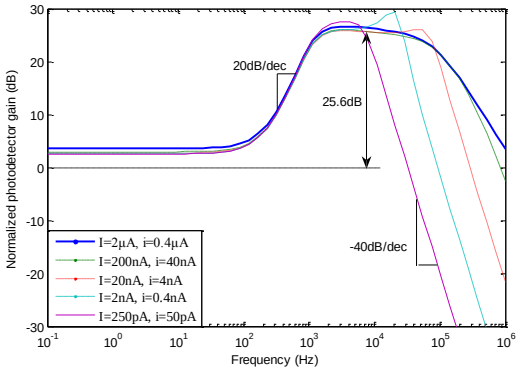
The sizes of M_2 – M_5 can be determined using (35). As mentioned previously, the size of M_2 and M_3 are preferred to be small in order to reduce parasitic capacitance effects on the photodetector, so the W/L of M_2 and M_3 are set to 1μm/1μm. If the offset is too large, V_2 will deviate from the designed dc operating point too much. This will cause either M_2 or M_3 out of subthreshold region. In order to make PMOS size not too large, the standard deviation of offset voltage is set as 5mV, which requires a reasonable size of PMOS with W_pL_p = 10μm^2. This also ensures the deviation from the designed dc operating point of the photodetector output is in the acceptable range.

Now consider the open loop gain of the Gm element in order to properly size M_4 and M_5.

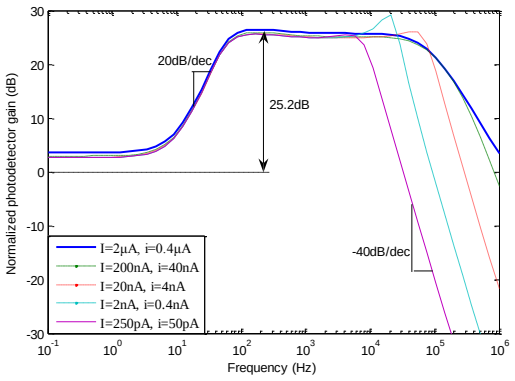
$$G_{G_m} = \frac{\kappa_n}{V_T(\lambda_3 + \lambda_5)} \quad (36)$$

where λ is inversely proportional to the channel length. Therefore the length of M_4 and M_5 should be as large as possible. Finally the W/L of M_4 and M_5 are determined to be 1μm/10μm. In this case, the standard deviation of offset V_{OS} is approximately 5.4mV.

Fig. 8 (a) shows the normalized logarithmic photodetector gain versus frequency for different photocurrents under 1V supply. In this case, the photodetector bias is 0.6V and Gm bias is 0.1V. As expected, if the photocurrent modulation depth is fixed, the gain will be the same and it is independent of the DC photocurrent. The calculated photodetector mid-band gain is 14, which corresponds to 22.9dB. Fig. 8 (a) shows the mid-band gain is 25.6dB because the parasitic capacitance introduced by the Gm increases the capacitance ratio of the photodetector. The zero, pole 3 and pole 2 are approximately at 100Hz, 1kHz and 10kHz respectively. This matches with calculation results. Pole 1 is determined by the photocurrent. As photocurrent increases, pole 1 moves towards high frequency. When pole 1 and pole 2 are close, this causes peaking in the gain. If photocurrent is 1μA, pole 1 will be larger than 10MHz. The lowest pole 3 can be achieved when the resistance R is maximized. In this case, the V_{gs} of M_1 in the Gm circuit is zero and this means the leakage current of M_1 acts as the tail current of the Gm. Fig. 8 (b) shows the detector gain when the Gm bias voltage is 0V and pole 3 is approximately at 100Hz. By adjusting the photodetector bias and Gm bias, the passband of the photodetector can be tuned.



(a)



(b)

Fig. 8 Simulation results of normalized photodetector gains for different photocurrents with 20% modulation depth and the photocurrents are 2μA, 200nA, 20nA, 2nA and 250pA, (a) Gm bias V_{b1} = 0.1V, (b) Gm bias V_{b1} = 0V.

III. Measurement Results of Photodetector

The tunable passband logarithmic photodetector was fabricated using a standard 0.25μm CMOS process and the micrograph of the chip is shown in Fig. 9. The circuit works under laser illumination, which may cause transistors to malfunction, therefore all the transistors are covered by top metal. Hence the circuit layout is also shown in the figure. The testing bench is shown in Fig. 10. A waveform generator is used to generate the modulation signal and its output is connected to a laser driver, which drives an 830nm laser diode. The maximum laser source power is 0.5mW due to the limitation of eye safety. A piece of metal with a 2.5mm diameter aperture in the centre is placed in front of the laser diode, so that a point light source is created. Two lenses are used to collimate the laser beam and focus the light. Neutral density (ND) filters are placed between the two lenses to attenuate the beam power so that the photodetector can be tested in a large range of illumination intensities. The focused

beam is directed to the IC chip by a beam splitter. There is also a microscope above the beam splitter. Through the microscope, the position of the IC chip can be adjusted so that the beam can illuminate the desired part of the chip.

The photodetector was tested under six different illumination intensities. These intensities are interesting because they correspond to certain working distance of the photodetector in the smart dust system [21]. The beam intensity was modulated by a square wave and the modulation depth was 20%. The upper cut-off frequency tuning has been shown in [17], so we focus on the lower cut-off frequency tuning. Fig. 11 shows the normalized photodetector gain vs. frequencies for two different Gm bias voltages. The upper cut-off frequencies for both cases are approximately 10kHz because we set pole 2 at 10kHz by a fixed I_{bias} in the measurement. When Gm bias is 0V, the lower cut-off frequency is approximately at 100Hz. The photodetector output is independent of the absolute illumination intensity. The gain has a peaking at 10 kHz when illumination intensity is $0.44\mu W/mm^2$. This is because pole 1 moves close to pole 2. When Gm bias is 0.1V, the lower cut-off frequency moves to approximate 1 kHz. In this case, pole 3 and pole 2 are too close and the passband is narrow. The simulation results for I=2nA/i=0.4nA are selected for comparison because the gain has a large peaking in this case. From Fig. 11, it can be seen that the bandwidth of simulation and experimental results has a good match. But the mid-band gain of the measurement is 2.6dB smaller than the simulation. The dominant reason is that

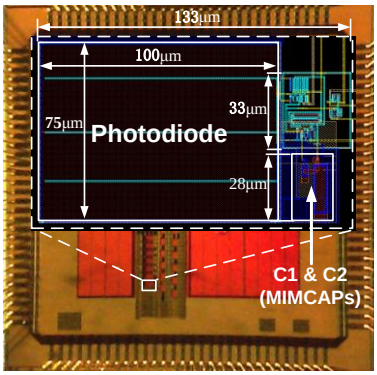


Fig. 9 The micrograph of the fabricated chip and photodetector layout.

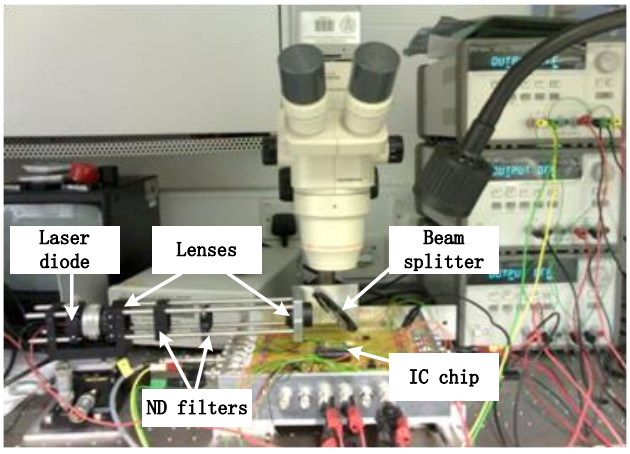


Fig. 10 The testing environment of photodetector.

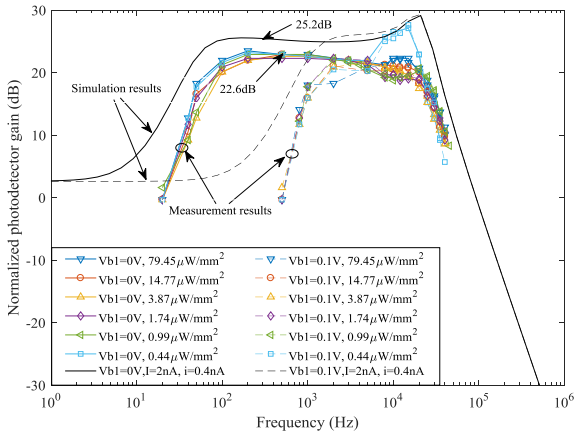


Fig. 11 The measurement results of normalized photodetector gain for different illuminations. Two Gm bias voltages (Vb1) are used. One is 0V, the other is 0.1V.

the photodetector output is connected to an on-chip source follower buffer for measurement purposes. The buffer has a gain of 0.68 and this causes the measured gain to drop by 3.3dB. A typical photodetector output signal is shown in Fig. 12. The illumination intensity is $0.44\mu W/mm^2$ and Gm bias is 0V. In this case, the total current consumption is 6.51nA. The turn-on time is also measured by monitoring the photodetector output when driving the voltage supply by an on-off signal, as shown in Fig. 13. It is approximately 16.6ms due to the large time constant of the circuit. The summary of performance parameters and comparison with previous works are shown in Table II.

A separate Gm circuit is also fabricated on the chip. The DC offset of 14 chips has been measured and the results are plotted in Fig. 14. The mean value is 7.03mV and standard deviation is 5.34mV. Although the chip quantity is not large, we get a good match with our estimation.

Table II Summary of performance and comparison with previous works.

	This work	Delbruck [17] 1995	Klosowski [6] 2016	Spivak [8] 2016	Ge [9] 2017
Technology	0.25μm	2μm	0.18μm	0.35μm	0.18μm
Tunable BW	Yes	No	No	No	No
Pixel size (μm^2)	100*133	80*80	21*21	30*30	11*11
Fill factor	75%	6.25%	5.5%	16.3%	50%
Vdd (V)	1	NA	1.8	3.3	3.8
Linear/log	log	log	linear	linear	linear

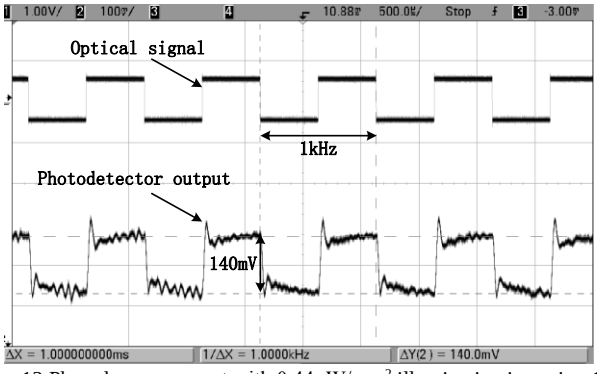


Fig. 12 Photodetector output with $0.44\mu W/mm^2$ illumination intensity, 1V supply, 0V Gm bias, 20% modulation depth and 1 kHz signal. The output signal has a little ringing due to the limited phase margin.

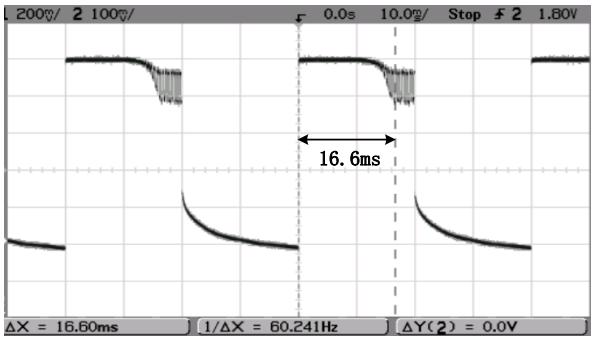


Fig. 13 Photodetector output signal when voltage supply is turned on and off. It needs approximate16.6ms to generate a stable small signal output

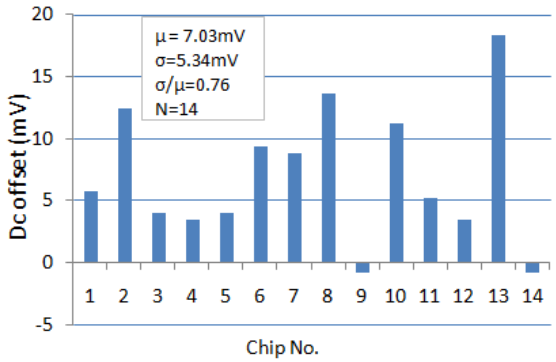


Fig. 14 Measured DC offset of Gm circuit for 14 chips, Gm bias is 0.1V and common mode input voltage is 0.4V.

IV. Conclusion

This paper discussed a logarithmic photodetector with a tunable passband for IoT smart dust applications. Theoretical analysis has been made and based on it the photodetector was designed by sizing each component and pole. A Gm circuit is proposed for the high impedance element in the photodetector. The tunable passband logarithmic photodetector was fabricated using a standard 0.25μm CMOS process and tested under five different illumination intensities. Measurement results show that the output voltage of photodetector is consistent with the theoretical analysis and simulation results. The lower cut-off frequency increases as Gm bias and the minimum is approximately 100Hz when Gm bias is 0V. The photodetector output and Gm DC offset matches with theoretical analysis. By adjusting the photodetector bias and Gm bias, the upper and lower cut-off frequencies can be tuned respectively. The feature of tunable passband enables the flexibility of selectively receiving optical signals and filtering out unwanted optical noise.

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References

[1] G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integration mode," *IEEE Journal of Solid-State Circuits*, vol. SC-2, pp. 65–73, 1967.

[2] J. Guo and S. Sonkusale, "A CMOS imager with digital phase readout for fluorescence lifetime imaging," 2011 Proceeding of the ESSCIRC, pp. 115-118, Sept. 2011.

[3] E. Kamrani, F. Lesage and M. Sawan, "A low-power photon-counter front-end dedicated to NIRS brain imaging," *IEEE Sensors Journal*, vol. 15, issue 7, pp. 3724-3733, July 2015.

[4] J. Ohta, Smart CMOS image sensors and applications, Illustrated Edition, CRC Press, section 2.5.2 at page 38, 2008.

[5] S. S. George, M. F. Bocko and Z. Ignjatovic, "Current sensing-assisted active pixel sensor for high-speed CMOS image sensors," *IEEE Sensors Journal*, vol. 15, issue 8, pp. 4365-4372, Aug. 2015.

[6] M. Klosowski, W. Jendernalik, J. Jakusz, G. Blakiewicz and S. Szczepanski, "A CMOS pixel with embedded ADC, digital CDS and gain correction capability for massively parallel imaging array," *IEEE Transactions on Circuits and Systems I*, vol. 64, issue 1, pp.38-49, Oct. 2016.

[7] H. T. Wang and W. D. L. Salas, "An image sensor with joint sensing and energy harvesting functions," *IEEE Sensors Journal*, vol. 15, issue 2, pp. 902-916, Feb. 2015.

[8] A. Spivak, A. Belenky and O. Yadid-Pecht, "Very sensitive low-noise active-reset CMOS image sensor with in-pixel ADC," *IEEE Transactions on Circuits and Systems II*, vol. 63, issue 10, pp.939-943, March 2016.

[9] X. Ge and A. J. P. Theuwissen, "A 0.5erms temporal noise CMOS image sensor with Gm-cell-based pixel and period-controlled variable conversion gain," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5019-5026, Dec. 2017.

[10] B. Choubey, "A wide dynamic range CMOS pixel with Steven's power law response," Proceedings of SPIE, vol. 7780, Aug. 2010.

[11] K. N. Glaros and E. M. Drakakis, "Self-biased logrithmic photoreceptor with low settling time," *IEEE Transactions on Circuits and Systems I*, vol. 59, issue 10, pp.2244-2251, Oct. 2012.

[12] M. K. Law, A. Bermak and C. Shi, "A low-power energy-harvesting logarithmic CMOS imaging sensor with reconfigurable resolution using two-level quantization scheme," *IEEE Transactions on Circuits and Systems II*, pp.80-84, Feb. 2011.

[13] D. Das and S. Collins, "A circuit that creates a logarithmic response from an integrating CMOS pixel," 2011 IEEE ISCAS, pp. 2201-2204, May 2011.

[14] J. J. Liu, Y. M. Zhou, G. F. Faulkner, D. C. O'Brien and S. Collins, "Optical receiver front end for optically powered smart dust", *International Journal of Circuit Theory and Applications*, vol. 43, issue 7, pp. 840-853, July 2015.

[15] D. C. O'Brien, J. J. Liu, G. E. Faulkner, et al.,"Design and implementation of optical wireless communications with optically powered smart dust motes," *IEEE Journal on Selected Areas in Communications*, vol. 27, No. 9, pp. 1646-1653, Dec. 2009.

[16] M. A. Mahowald, "Silicon retina with adaptive photoreceptor," Proceedings of SPIE/SPSE Symposium on Electronic Science and Technology: from Neurons to Chips, vol. 1473, pp. 52–58, April 1991.

[17] T. Delbrück and C. A. Mead, "Analog VLSI phototransduction by continuous-time, adaptive, logarithmic photoreceptor circuits," Vision Chips: Implementing vision algorithms with analog VLSI circuits, C. Koch and H. Li editors, IEEE Computer Society Press, pp. 139-161, 1995.

[18] O. Bajdechi and J. H. Huijsing, Systematic design of sigma-delta analog-to-digital coverters, Springer, pp. 60-62, 2004.

[19] E. A. Vittoz, "The design of high-performance analog circuits on digital CMOS chips," *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 657–665, June 1985.

[20] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. SC-12, pp. 224–231, June 1977.

[21] J. J. Liu, G. E. Faulkner, B. Choubey, J. Liu, R. Q. Chen, D. C. O'Brien and S. Collins, " Optically powered energy source in a standard CMOS process for integration in smart dust applications," *IEEE Journal of Electron Devices Society*, .vol. 2, No. 6, pp. 158-163, Nov. 2014.