An Optically Differential Reconfigurable Gate Array with a Holographic Memory

Minoru Watanabe, Mototsugu Miyano, and Fuminori Kobayashi
Department of Systems Innovation and Informatics
Kyushu Institute of Technology
680-4 Kawazu Iizuka, Fukuoka, 820-8502, Japan
Email: {watanabe,koba}@ces.kyutech.ac.jp

Abstract

Optically Reconfigurable Gate Arrays (ORGAs) offer the possibility of providing a virtual gate count that is much larger than those of currently available VLSIs by exploiting the large storage capacity of holographic memory. We developed an Optically Differential Reconfigurable Gate Array (ODRGA-VLSI) with no overhead and fast reconfiguration capability. This paper presents the results of development of a perfect optical reconfigurable system with the ODRGA-VLSI chip and holographic memory. Experimental results of the reconfiguration procedure and circuit performance on a gate array are also presented.

1. Introduction

Field Programmable Gate Arrays (FPGAs) are well known as reconfigurable devices [1],[2]. However, because their reconfiguration requires more than several milliseconds, FPGAs are not suitable for dynamically reconfigurable applications.

On the other hand, as fast reconfigurable devices, optically programmable gate arrays (OPGAs) have been developed that combine various optical and electrical techniques [3]-[10]. These devices present the possibility of providing a virtual gate count that is much larger than that of currently available VLSIs using a holographic memory. However, previously proposed ORGAs have remained limited to several tens of microseconds by the VLSI component.

Therefore, we have developed an Optically Differential Reconfigurable Gate Array (ODRGA-VLSI) to realize rapidly reconfigurable devices with no overhead [11],[12],[**?**]. The no overhead and nanosecond reconfiguration capability of a fabricated VLSI chip has been confirmed experimentally. However, up to now, a holographic memory part has never been developed to accommodate the ODRGA-VSLI chip.

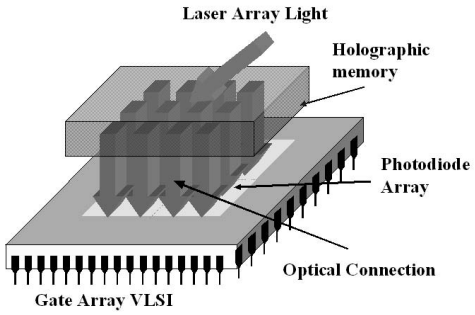

Figure 1. Overview of an ODRGA.

This paper presents the development result of a perfect optical reconfigurable system with the ODRGA-VLSI chip and a holographic memory. Experimental results of the reconfiguration procedure and circuit performance on a gate array are also presented here.

2. ODRGA system

2.1. Overview

Fig. 1 shows an overview of an ODRGA system. The ODRGA system consists of laser sources to address reconfiguration contexts, an optical memory to generate reconfiguration contexts and a gate array VLSI that has 340 photodiodes to detect the reconfiguration context light. The reconfiguration procedure is executed by writing the reconfiguration context light through an optical memory generated from a laser source onto the gate array VLSI. That architecture allows reconfiguration in nanoseconds.

2.2. Differential reconfiguration strategy

The differential reconfiguration circuit of an ODRGA-VLSI is shown in Fig. 2. A single-bit differential reconfig-

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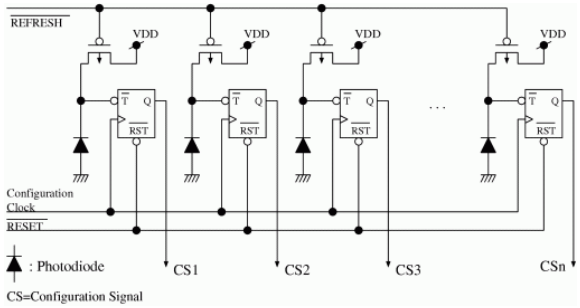

Figure 2. Circuit diagram of an array of differential reconfiguration circuits.

uration circuit consists of a refresh transistor, a photodiode, and a toggle flip-flop. The flip-flop is used for maintaining the state of the gate array. Consequently, the optical reconfiguration procedure for a gate array and circuit operation implemented on the gate array can be executed in parallel. As a result, the architecture has no overhead and nanosecond reconfiguration capability.

In addition, because the reconfiguration procedure is executed based on previous configuration data, bit-by-bit reconfiguration is available. Therefore, reconfiguration of an arbitrary portion of a gate array is enabled. That capability is used for reducing the optical power consumption or increasing the memory efficiency.

2.3. ODRGA-VLSI Design

Fig. 3 shows a block diagram of a fabricated ODRGA-VLSI [12]. The VLSI chip functionality is fundamentally identical to that of typical FPGAs. The ODRGA-VLSI chip consists of four logic blocks, four I/O blocks, and five switching matrices. Each configuration bit of these blocks has a differential reconfiguration circuit with a photodiode.

Fig. 4 shows a logic-block diagram. The logic block consists of a four-input / one-output look-up table (LUT), four multiplexers, and a delay flip-flop with a reset function. These functions are optically reconfigurable using 40 photodiodes.

Fig. 5 shows a switching matrix diagram. The gate array includes one four-directional and four three-directional switching matrices. The four-direction and three-direction switching matrices respectively contain 24 and 12 photodiodes.

A block diagram of an I/O block is shown in Fig. 6. Each I/O block is controlled by nine photodiodes.

An ODRGA-VLSI chip was fabricated using 0.35 μm triple-metal CMOS process. In this fabrication, we designed the distance between each photodiode as 90 [μm]; the photodiode is 25.5 $\times$ 25.5 [μm^2] to ease optical alignment. The

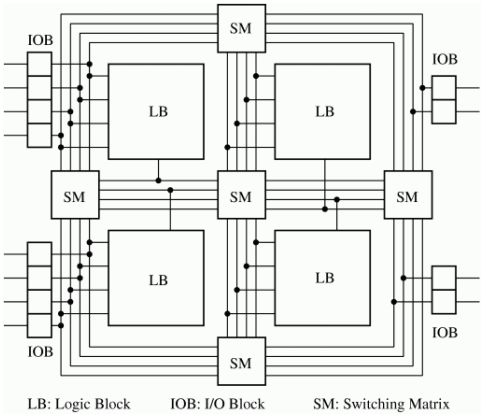

Figure 3. Block diagram of the ODRGA.

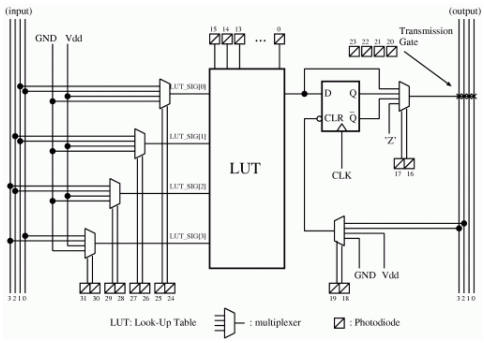

Figure 4. Block diagram of a logic block.

total number of photodiodes is 340. The specifications, the CAD layout, and a chip photograph of the ODRGA-VLSI are shown respectively in Table 1, Fig. 7.

3. Experimental System and Results

Figure 8 shows our construction of an optical system. A photograph of the experimental system is shown in Fig.

Technology	0.35μm double-poly triple-metal CMOS process
Chip size	4.9 $\times$ 4.9 [mm]
Photodiode size	25.5 $\times$ 25.5 [mm]
Number of photodiodes	340
Implementation Area of Photodiodes	221085[μm^2] 1.8%

Table 1. Specification of ODRGA-VLSI.

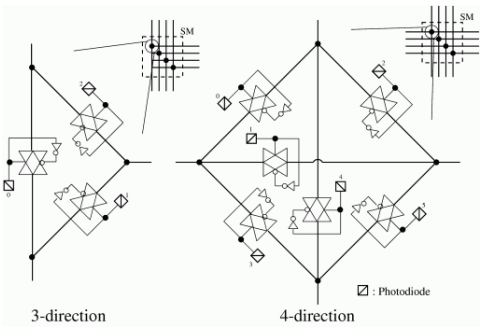

Figure 5. Block diagram of a switching matrix.

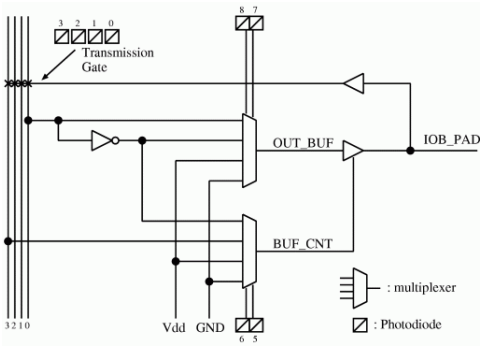

Figure 6. Block diagram of an I/O block.

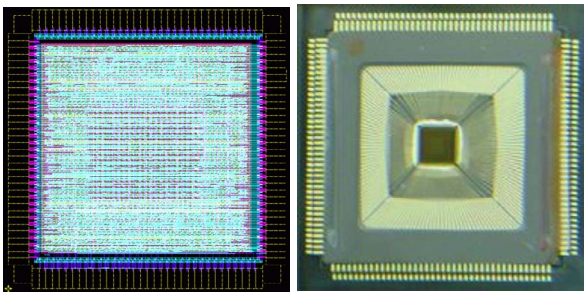

Figure 7. CAD layout and chip photograph of an ODRGA-VLSI.

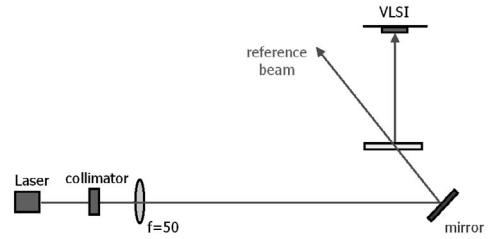

Figure 8. Block diagram of a holographic optical system.

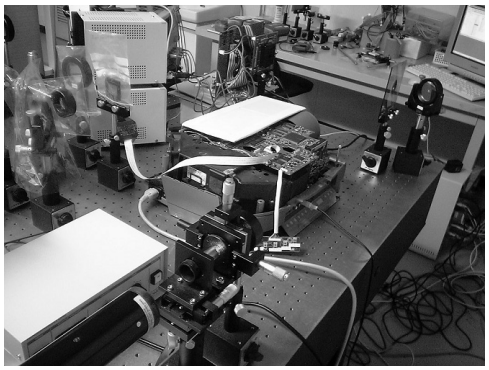

Figure 9. Photograph of the experimental system.

9. A He-Ne laser was used as light source; its power and wavelength were about 20 mW and 633 nm, respectively. The laser light was collimated and the parallel light beam was incident to a holographic memory with a certain angle that had previously written a context. The diffraction pattern from the holographic memory is impinged upon the ODRGA-VLSI. The number of connected optical buses is 340.

Using the experimental system, we implemented a four-bit up counter on the gate array. Previously, the reconfiguration pattern of a four-bit up-counter was written onto a holographic memory. The reconfiguration procedure was executed by generating a refresh pulse and then by increasing the configuration clock (CCLK). Results show that when a 20 mW He-Ne laser was used, the reconfiguration time was 1.44 ms. The diffraction efficiency was about 0.2%. Fig. 10 shows an experimental result for a four-bit up-counter that worked correctly after the configuration was completed.

The 1.44 ms reconfiguration speed is not faster than that of conventional ORGAs. However, the light power received by the VLSI is only 917 uW. We have confirmed that VLSI part can be reconfigured in nanoseconds using pulse lasers. Therefore, although the reconfiguration speed was not sat-

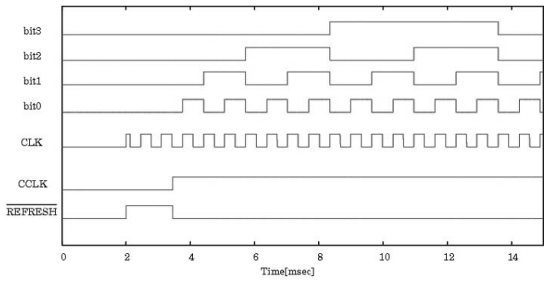

Figure 10. Experimental results of reconfigured 4bit up-counter.

isfied since this experimental system was constructed using a He-Ne Laser, if a pulse laser with 56 uJ will be adapted for this optical system, we can estimate that a future optical system can be reconfigured in less than 720 ns.

4. Conclusion

Optically Reconfigurable Gate Arrays (ORGAs) present the possibility of providing a virtual gate count that is much larger than currently available VLSIs by exploiting the large storage capacity of a holographic memory. In that case, because circuits implemented on a gate array must often be changed with virtual circuits stored on a holographic memory, rapid reconfiguration is required to reduce the overhead that is necessary for reconfiguration. We have already developed an Optically Differential Reconfigurable Gate Array (ODRGA-VLSI) with no overhead and fast reconfiguration capability. This paper presented a perfect optical reconfigurable system with the ODRGA-VLSI chip and a holographic memory.

We have implemented a four-bit up counter on gate array. Results demonstrate that when a 20 mW He-Ne laser is used, the reconfiguration time was 1.44 ms. Of course, the 1.4 ms reconfiguration speed is not faster than that of conventional ORGAs. However, the light power used on the VLSI in this experimental system was only 917 uW. Estimating the reconfiguration speed by using experimental results with pulse lasers [13], in the near future, when a pulse laser with 56 uJ will be adapted for this optical system, we can estimate that a future optical system can be reconfigured in less than 720 ns.

5. Acknowledgment

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