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An Optimized Vertical GaN Parallel Split Gate Trench MOSFET Device Structure for Improved Switching Performance

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ABSTRACT This work proposes a vertical gallium nitride (GaN) parallel split gate trench MOSFET (PSGT-MOSFET) device architecture suitable for power conversion applications. Wherein two parallel gates, and a field plate are introduced vertically on the sidewalls and connected, respectively, to the gate and source. Technology computer-aided design (TCAD) simulator was used in the design process to achieve a specific on-resistance as low as 0.79 mΩ.cm^2 for the device, which has the capacity of blocking voltages up to 600 V. The peak electric field of the PSGT-MOSFET could well be lowered to 2.95 MV/cm, which is about 17% lower than that of a conventional trench gate MOSFET (TG-MOSFET) near the trench corner with help of suitable design and optimization of trench depth, drift doping, and field plate thickness. The TCAD simulation shows that the higher drift doping on the device performance of PSGT-MOSFET produces $\sim 2\times$ lower switching losses when compared with a similarly rated conventional TG-MOSFET device.

INDEX TERMS Vertical GaN, trench MOSFET, split gate, on-resistance, switching loss, TCAD.

I. INTRODUCTION

POWER semiconductor switches are the basic components of any power converter circuit to improve the efficiency of modern electronics systems. The automotive semiconductor industry uses high voltage batteries (200 to 300 V) in the hybrid electric vehicles (HEV) [1]. To make HEV conversion efficient, the development of 600 V power MOSFET switches are desired to reduce the power losses [2]. The existing Si-based power device has reached its performance restriction due to the limitation of its material property, and it is difficult to enhance overall performance through the innovation of device principles, the improvement of structure and the progress of the manufacturing process [3], [4]. To achieve better conversion efficiency, the high-performance power devices are needed which have smaller conduction losses and lower switching losses, making them feasible for high-frequency, high-temperature operations. The two most promising WBG semiconductors are silicon carbide (SiC) and gallium nitride (GaN). SiC switches and diodes have been developed over the past decade to meet certain demanding military and commercial applications and have demonstrated high efficiency and high-temperature operation. GaN switches are projected to have a $100\times$ performance advantage over silicon-based devices, and $10\times$ over SiC, owing to their excellent material properties such as high electron mobility, a high breakdown field, and a high electron velocity. GaN-based power electronics feature both low on-resistance and fast switching, leading to substantial reductions in conduction and switching losses, respectively [5]–[10]. The first generation of GaN transistors has been the high electron mobility transistors (GaN HEMTs) that have demonstrated an excellent trade-off between R_{on} and V_{br} [11]–[13].

However, the GaN HEMT device has a normally-on behaviour, and negative gate bias is required to turn off the transistor [14], [15]. Hence, the use of normally-off GaN lateral transistors has led to the development of cascode devices. In a cascode device, the depletion-mode GaN lateral transistor and enhancement-mode Si-MOSFET are packed in series to form a normally-off behaviour [16]. The drawback of GaN based cascode devices is that the series connection of the two devices increases packing complexity, resulting in parasitic inductances that might upset the switching performance of the device [17], [18].

On the other hand, vertical GaN transistors show promising characteristics for high power switch applications to benchmark against GaN HEMT [19]–[22]. Because of their normally-off behavior, suitability for having the peak elec-

tric field (E-field) distant from the surface, and capacity to handle larger power densities. Some of the earlier reports demonstrated that the device performance of 600 V GaN vertical transistors are based on the structure; such as the MOS channel [23], quasi vertical [24], fully vertical [25], regrowth channel types [26], and split gate power MOSFET [27]. Among these structures, the MOS channel based GaN vertical trench gate MOSFET (TG-MOSFET) design has a significantly smaller on-resistance due to the lack of a junction field effect transistor (JFET) region [28]–[31], leading to low switching loss. However, TG-MOSFETs have a significantly higher gate-to-drain capacitance (C_{GD}) and gate-to-drain charge (Q_{GD}) owing to the gate, having been separated from the drain by a thin layer of gate oxide, both of which contribute to a substantial increase in the switching loss and lowers converter efficiency [32]. A critical issue for TG-MOSFET is to lower the E-field which is present in gate oxide around the trench bottom. The split gate technique has been implemented in order to mitigate the issue [33]–[35].

The split-gate MOSFET (SGT-MOSFET) is an innovative trench structure, which uses an isolated FP between gate and drain to reduce the gate-to-drain charge and improve the figure of merit while it benefits from low switching loss compared with conventional TG-MOSFET [34]. Another technique for improving the figure of merit and optimizing the electric field distribution is to use an additional charge control electrode (i.e. floating electrode) in the SGT-MOSFET, as known as a floating gate power MOSFET (FG-MOSFET) [35]. However, in order to realize the SGT-MOSFET and FG-MOSFET, many additional process steps such as deposition and etching were needed due to an interlayer dielectric (ILD) layers used to isolate the gate to field-plate (FP) and field-plate to floating gate (FG). During ILD growth step, thermally grown oxide on top of the FP and FG electrodes become challenging due to the temperature controllability. In this work, a distinct design technique known as the vertical GaN parallel split gate MOSFET (PSGT-MOSFET) structure concept, is proposed with the aim of improving the switching performance. There is no ILD layer in the PSGT-MOSFET, which leads to a reduction in the number of mask steps during patterning. Hence, fabrication costs of PSGT-MOSFET could be reduced when compared to SGT-MOSFET and FG-MOSFET. This methodology was used in the development of Si-based shielded gate MOSFET [39], [40]. The PSGT-MOSFET structure uses a vertical field-plate oxide into a drift layer, which is significantly thicker than the gate oxide. Employing thick oxides at the bottom and trench sidewalls to facilitate field shaping, which involves controlling the location of peak electric fields and preventing an avalanche or significant hot carrier generation in the vicinity of the trench gate oxide. The vertical FP and thick oxide make it possible to use a larger drift doping while maintaining the same breakdown voltage device rating. This indicates that the R_{on} is lower for a given breakdown. The switching performance of the PSGT-MOSFET is also drastically enhanced due to the reduction in C_{GD} i.e. C_{rss}.

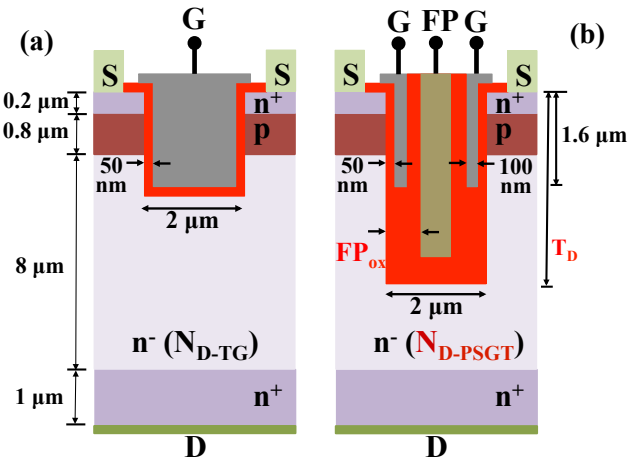

FIGURE 1. Cross-sectional representation of (a) TG-MOSFET and (b) PSGT-MOSFET.

The main objective of this study is to benchmark a vertical GaN PSGT-MOSFET for the first time, which will allow for a comparison with TG-MOSGET in terms of switching performance. The TCAD mixed-mode platform has been used in order to perform device and circuit simulations. The paper has been organized in the following manner: in section II, the device designs and simulation methodology are introduced. Section III presents the optimization of the PSGT-MOSFET in order to achieve the desired breakdown voltage of 600 V while simultaneously lowering the maximum GaN E-field at the trench bottom to below 3 MV/cm. The proposed fabrication process steps are highlighted in Section IV. Lastly, section V contrasts the static and dynamic characteristics of proposed a PSGT-MOSFET with those of a conventional device.

II. DEVICE OPERATIONS, AND SIMULATION METHODOLOGY

The device operation and simulation methodology have been performed using a TCAD simulator. Fig. 1(a) illustrates the cross-sectional representation of TG-MOSFET device structure. The structure has been based on our most recent publication, which includes an 8 μm thick Si doped (2×10^{16} cm^{-3}) GaN drift layer, a 0.8 μm thick Mg doped (1.3×10^{17} cm^{-3}) GaN base layer, and a 0.2 μm thick Si doped (5×10^{18} cm^{-3}) GaN source layer. These layers are built on a Si doped GaN substrate. The doping of the base layer has been optimized and adjusted to achieve a threshold voltage of $\sim$ 4.6 V and a breakdown voltage of 600 V. The device has been designed with a trench depth of 2 μm and a metal-oxide-semiconductor (MOS) structure has been built into both the sidewall and bottom of the trench.

The device structure parameters of PSGT-MOSFET coincide with those of TG-MOSFET, as shown in Fig. 1(b). Except to complete gate electrode in conventional TG-MOSFET, the middle section of gate electrode in PSGT-MOSFET is changed to thin parallel gate metal lining along

gate oxide, SiO_2. Furthermore, the trench depth in conventional TG-MOSFET is extended to the expected position into the drift layer, and is formed the FP. The FP electrode is connected to source electrode and splits with thicker oxide, thereby substantially reducing the overlapping capacitance, i.e., C_{rss} [34]. However, the gate-to-source capacitance (C_{GS}) will increase the input capacitance of PSGT-MOSFET. The thicker FP oxide will create a charge balancing effect by redistributing E-field at the trench bottom. Thanks to FP technology, which leads to the enhancement of the lateral depletion and allows a higher doping concentration in the drift layer, causing a reduction in R_{on} without impacting on breakdown voltage. As a consequence, it contributes to an increase in the switching speed of the device.

The device characteristics were calibrated amongst the experimental results of a fabricated TG-MOSFET, described by R. Li et al. [23] using TCAD simulation [41]. The TCAD device simulation methodology and important physics models have been reported in the previous work [27], [35]–[38], as shown in Table 1. TCAD Sentaurus provides users with access to a wide variety of physical models, each of which is designed to explain the physical behavior of semiconductor devices as precisely as is technically feasible in relation to the fabricated device. The important physics models have been included in device simulations in order to get accurate forecasts of the fabricated device characteristics. The simulation methodology has been adopted by computing the Poisson's equation, including the electron and hole continuity equations and 2D drift-diffusion carrier transport equations. The recombination phenomenon was taken into account by using three processes, specifically the Radiative, Auger, and Shockley-Read-Hall (SRH) models for a fixed minority-carrier lifetime. In order to take into consideration the effects of velocity saturation, the Caughey Thomas field dependent mobility model and Masetti model for doping dependency were incorporated into the simulation. Simulation models for vertical GaN power transistors were selected with reference to previously published works. According to the report in ref. [27], [35], the selected simulation models and the experiment [23] have a very good level of agreement with one another. At the gate dielectrics-trench contact, a fixed charge concentration of approximately 1.5 $\times 10^{12}$ cm^{-2} was implemented so that it achieves the desired match of the threshold voltage [43]. Furthermore, the experimentally determined breakdown voltage of 600 V was precisely matched by adjusting the effective base layer concentration (1.3 $\times 10^{17}$ cm^{-3}).

III. DEVICE OPTIMIZATION

The main focus of the optimization of PSGT-MOSFET is to obtain lower R_{on} and V_{br} of 600 V without modifying the thickness of drift layer and minimizing the electric field distribution at the trench when compared to TG-MOSFET. In order to meet the requirements of this desire, numerous optimizations have been implemented on devices, such as higher drift doping concentration (N_{D-PSGT}), deep trench depth (T_D), and thicker FP oxide (FP_{ox}) of proposed device.

TABLE 1. The parameters and models used in this work

Parameter	Value
Bandgap (eV)	3.437
Dielectric constant	8.9
Electron affinity (eV)	3.95
Activation energy for donor (meV)	15
Activation energy for acceptor (meV)	290
Electron saturation velocity (cm/s)	1.27×10^{7}
Hole saturation velocity (cm/s)	1.7×10^{7}
Maximum electron mobilities (cm$^2/V.s$)	1500
Maximum hole mobilities (cm$^2/V.s$)	150
Impact ionization coefficients for electrons (A_n) (/cm)	2.9×10^{8}
Impact ionization coefficients for electrons (A_p) (/cm)	5.41×10^{6}
Impact ionization coefficients for holes (B_n) (V/cm)	3.4×10^{7}
Impact ionization coefficients for holes (B_p) (V/cm)	1.96×10^{7}
Auger recombination model for electrons (cm$^6/s$)	3.0×10^{-31}
Auger recombination model for electrons/holes (cm$^6/s$)	3.0×10^{-31}
Direct recombination constant (cm$^3/s$)	2.0×10^{-10}
Carrier lifetime of electrons/holes (ns)	0.7/2.0
Critical electric field in this work (MV/cm)	3.75

TABLE 2. Device structure parameters during simulation

Parameter	TG-MOSFET	PSGT-MOSFET
n$^+$ Source layer depth (μm)	0.2	0.2
p Base layer depth (μm)	0.8	0.8
n$^-$ Drift layer depth (μm)	8.0	8.0
n$^+$ Source doping (cm^{-3})	5.0×10^{18}	5.0×10^{18}
p Base doping (cm^{-3})	1.3×10^{17}	1.3×10^{17}
n$^-$ Drift doping (cm^{-3})	2.0×10^{16}	3.5×10^{16}
Gate width (μm)	2.0	2.0
Gate oxide thickness (G_{ox}) (μm)	0.05	0.05
Gate trench depth (μm)	1.6	1.6
Deep trench depth (T_D) (μm)	1.65	7.0
Field plate oxide (FP_{ox}) (μm)	–	0.49

A higher N_{D-PSGT} doped has a low R_{on} and V_{br}. However, the incorporated deep T_D establishes a greater gate-modulated accumulation charge by the drain [42], which is suitable for increasing V_{br} while maintaining low R_{on}. Meanwhile, the extended deep of trench depth into the drift layer, the C_{GD} is enhanced, affecting the switching delays. Therefore, thicker FP oxide is an important parameter that reduces the C_{GD} by using higher oxide thickness at the trench bottom. Fig. 2 shows the influences of N_{D-PSGT}, T_D, and FP_{ox} on the V_{br}, the R_{on}, and E-field distribution near the trench bottom. During optimization, the pitch of PSGT-MOSFET device structure has been incorporated exactly the same as the TG-MOSFET.

As shown in Fig. 2(a), of the three variables (i.e. N_{D-PSGT}, T_D, and FP_{ox}), only two (N_{D-PSGT}, and T_D) are varied at a time, whereas the other one (FP_{ox}) will be

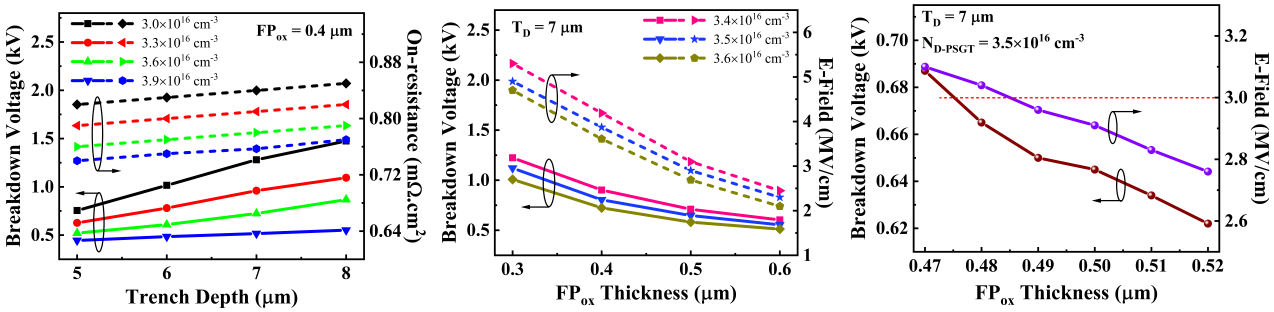

FIGURE 2. (a) Influences of V_{br} and R_{on} on T_D and N_{D-PSGT}, (b) Influences of V_{br} and E-Field on FP_{ox} and N_{D-PSGT}, and (c) Influences of V_{br} and E-Field on FP_{ox}.

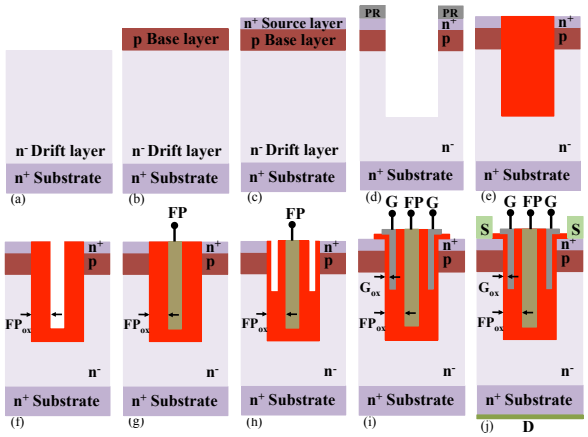

FIGURE 3. Fabrication process steps of PSGT-MOSFET device.

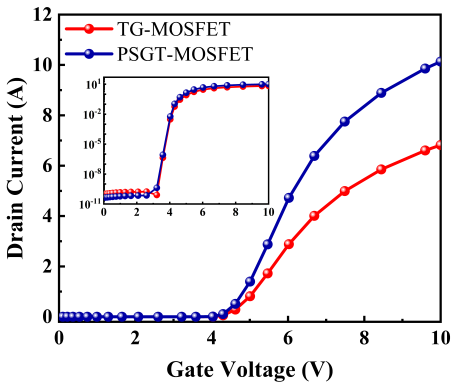

FIGURE 4. Transfer characteristics of devices.

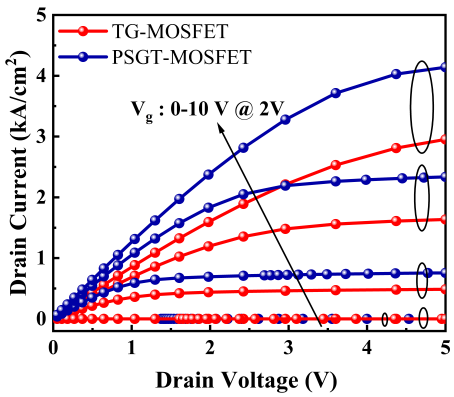

FIGURE 5. Output characteristics of devices.

set at a fixed value. The N_{D-PSGT} value is varied from 3.0 $\times 10^{16}$ cm^{-3} to 3.9 $\times 10^{16}$ cm^{-3}, and the T_D value is varied from 5 μm to 8 μm, respectively. As expected, when T_D increases, both the V_{br} and R_{on} increase. To reach the 600 V breakdown voltage target, doping levels need to be below 3.6 $\times 10^{16}$ cm^{-3}, and trench depth 7 μm. As a result, these parameters have been decided to constitute a beginning step for the simulation.

When considering these parameters, the peak E-field of PSGT-MOSFET device demonstrates a greater than 3.0 MV/cm surrounding the trench bottom. Hence, increasing the thickness of FP_{ox} can reduce the E-field profile around the trench bottom. The value of FP_{ox} is varied from 0.3 μm to 0.6 μm, and N_{D-PSGT} from 3.4 $\times 10^{16}$ cm^{-3} to 3.6 $\times 10^{16}$ cm^{-3}, whereas the other one (T_D= 7 μm) is fixed. Fig. 2(b) demonstrates the decrement of V_{br} with respect to the change in the FP_{ox} thickness with respect to N_{D-PSGT}. The desired breakdown voltage is achieved between 0.4 μm to 0.5 μm (FP_{ox}), and $\sim$ 3.5 $\times 10^{16}$ cm^{-3} (N_{D-PSGT}). To achieve high reliability, peak E-field should be maintained at less than 3.0 MV/cm at the bottom of FP_{ox}. As shown in Fig. 2(c), to obtain the accurate breakdown voltage (about 650 V) and electric field (less than 3.0 MV/cm), the field plate oxide thickness between 0.47 μm to 0.52 μm have been varied. Finally, it is found that the optimum values for PSGT-MOSFET are obtained as follows: N_{D-PSGT} of $\sim$ 3.5 $\times 10^{16}$ cm^{-3}, and FP_{ox} of $\sim$ 0.49 μm at T_D of 7 μm. The structural details are given in Table 2.

IV. PROPOSED FABRICATION PROCEDURE

In regards to the fabrication procedures, the optimized PSGT-MOSFET has been shown to be feasible in Fig. 3. The proposed process steps began with growth of low-doped n$^-$ GaN (Si doped) drift and p GaN (Mg doped) base layer on a freestanding n$^+$ GaN wafer [24], [25] (Fig. 3(a)-(b)). On the uppermost part of the base layer, a selective area regrowth of

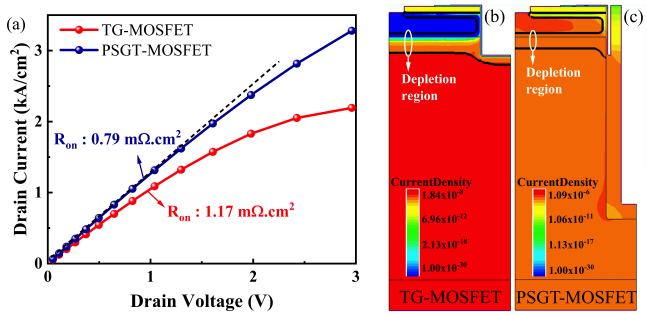

FIGURE 6. (a) Specific on-resistance estimation, depletion region at V_d = 1 V keeping V_g = 10 V (b) TG-MOSFET, and (c) PSGT-MOSFET.

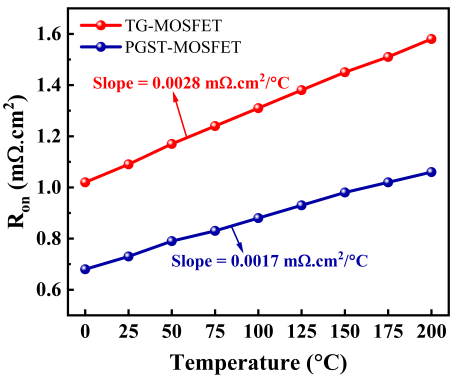

FIGURE 7. Comparison of the R_{on}, and temperature dependency of the PSGT-MOSFET to the counterparts of the TG-MOSFET.

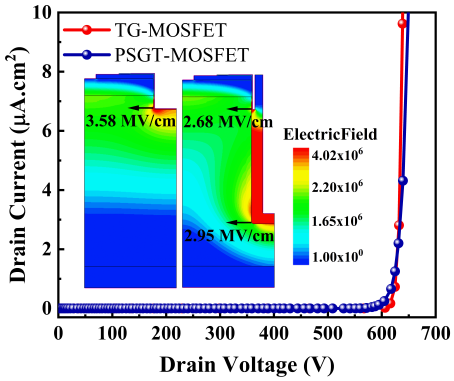

FIGURE 8. Breakdown characteristics of TG-MOSFET, and PSGT-MOSFET (Inset distribution of E-field).

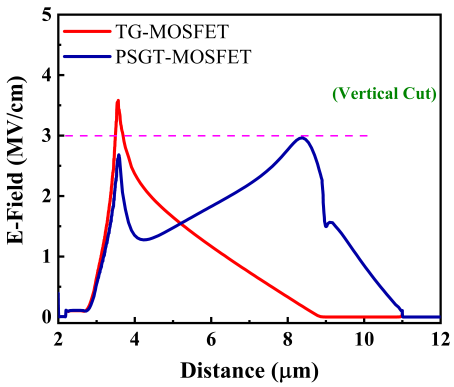

FIGURE 9. E-field profile during vertical cutline of TG-MOSFET, and PSGT-MOSFET.

an n^+ GaN source layer (Si doped) was performed [44] (Fig. 3(c)). A hard photoresist layer (PR) is used for patterning over the suitable region to remove a selective portion (Fig. 3(d)). An ICP-process was used to etch a gate width of 2 μm using the PR to a depth such that the bottom of the trench (7 μm) is located within the drift layer [45] (Fig. 3(d)). The wafer was then subjected to wet etching operations in order to clean the surface that had been etched and smooth the surface of the trench sidewall. Following etching, a dielectric layer (i.e. FP_{ox}) was deposited (Fig. 3(e)) and etched back to form an oxide sidewall (Fig. 3(f)). Metal was then filled inside the trenches for FP electrode. After that, the metal was isotropically etched and recessed within the trenches (Fig. 3(g)). Sputtering with metal was the technique of choice to provide complete coverage of the shielded FP [46]. The source and FP electrode will be electrically linked to one another. Following that, FP_{ox} was etched, revealing a portion of FP metal that forms two troughs on its sides inside the trench (Fig. 3(h)). After this, a dielectric layer of gate oxide (G_{ox}) (0.05 μm-thick) was formed across the top of the wafer, trench sidewalls, and troughs inside the trenches (Fig. 3(i)). The removed region is deposited with a suitable metal to form a gate contact. In order to create the source electrodes, a metal stack was first deposited, and then it was patterned. Lastly, the drain electrode was then made by placing a metal stack on the back of the substrate (Fig. 3(j)) [47]–[51].

V. RESULTS AND DISCUSSIONS

The transfer characteristics (I_d-V_g) of devices are plotted in Fig. 4. The PSGT-MOSFET presents a very similar threshold voltage (4.58 V) to that of the TG-MOSFET (4.6 V). The output characteristics (I_d-V_d) for both devices under different gate voltages are superimposed as shown in Fig. 5. Clearly, the current carrying capability is higher for PSGT-MOSFET as compared to that of TG-MOSFET device for a V_g = 10 V. The R_{on} value of 0.79 mΩ.cm^2 for PSGT-MOSFET is found to be $\sim$32% lower than that of TG-MOSFET for a drain voltage of 1 V, as indicated in Fig. 6(a). This is because the PSGT has been used with a higher drift doping concentration, which in turn causes an increase in the drive current and results in a lower R_{on} in the drift layer. As observed from Fig. 6(b)-(c), the depletion regions (the region enclosed by black lines) formed by the p base and trench region reduce to a great extent in the proposed structure as compared to the conventional structure because of the high dopant concentration of the drift region. As the current density increases, the on-resistance decreases (the proposed structure is 1.09 $\times 10^{-6}$ A/cm^2 and conventional structure is 1.84 $\times 10^{-8}$ A/cm^2), and electron flow occurs primarily in the parallel split gate with deep trench of the added region. The added region for electrons to flow through the drift region provides a low resistivity path, and the electrons

spread rapidly to the bottom of the substrate region. Thus, the proposed PSGT-MOSFET achieves a lesser value of the on-resistance as compared to the conventional device. On the other hand, the R_{on} values of proposed and conventional devices are shown as a function of different temperatures in Fig. 7. The temperature coefficient of PSGT-MOSFET is found to be 0.0017 mΩ.cm^2/°C (average slope), which is $\sim$39% lower than that of TG-MOSFET. It is observed that R_{on} of the PSGT-MOSFET is less dependent on temperature than that of the TG-MOSFET. Hence, applications requiring operation at high temperatures are a good fit for the PSGT-MOSFET.

The breakdown voltage characteristics are simulated as shown in Fig. 8. The PSGT-MOSFET shows a very comparable breakdown voltage (650 V) to that of the TG-MOSFET (623 V), when V_g = 0 V. The maximum reduction in R_{on} without compromising blocking voltage is achieved, which is attributed to its heavily doped drift layer and FP region. Later, Baliga's FOM (V_{br}^2/R_{on}) is expressed for indicating the trade-off amongst off-state breakdown voltage and on-state resistance [52], wherein PSGT-MOSFET is calculated to 531 MW/cm^2 which is $\sim$63% better than that of TG-MOSFET.

The distribution and contour line of E-Field at the blocking regime (V_d = 600 V, and V_g = 0 V) for TG-MOSFET and PSGT-MOSFET are shown in inset Fig. 8. In TG-MOSFET, the E-field is overcrowded in the channel region (under the gate). The overcrowding of the E-field leads to a reliability issue for TG-MOSFET. Instead, in the PSGT-MOSFET, the better charge balance phenomenon is observed in the trench corner where the E-field is more uniform across the drift layer, as shown in Fig. 9. This is because of the perpendicular splitting effect of the thicker FP region. The E-field of the PSGT-MOSFET is 2.68 MV/cm at the gate oxide. In addition, the peak oxide E-field (E_{ox}) of PSGT-MOSFET is observed to 2.95 MV/cm, which is $\sim$17% lower than that of TG-MOSFET around the trench corner, respectively.

In TG-MOSFET, the input capacitance [C_{iss} = C_{GS} (gate-source capacitance) + C_{GD} (gate-drain capacitance)], output capacitance [C_{oss} (=C_{GD} + C_{DS} (drain-source capacitance)], and reverse capacitance, C_{rss} (=C_{GD}), are shown in Fig. 10(a). Among all, C_{rss} plays a significant part in analyzing the switching speed of the device as well as preventing false turn-on. Fig. 10(b) shows that in PSGT-MOSFET, there are two capacitances associated with FP (i.e., C_{GS2}, and C_{DS2}). These capacitors are connected in series, which leads to lowering the C_{GD} value. However, C_{GS1} and C_{GS2} are connected in parallel, which slightly increases the input capacitance. Additionally, C_{DS1} and C_{DS2} help to lower the peak overshoot voltage stress on the SGT-MOSFET. This stress comes from circuit parasitic and high dv/dt immunity in switching converter circuits [53]. The terminal capacitance of both devices is shown in Fig. 10(c). The AC signal is established to be 1 MHz to obtain the capacitance by varying the V_d from 0 to 600 V while keeping V_g = 0 V. C_{iss} and C_{oss} of the PSGT-MOSFET are a little higher than that of TG-MOSFET, which has a small effect on switching time and efficiency in high-frequency DC-DC converters. However, the extracted C_{rss} for PSGT-MOSFET is 61 pF/cm^2, which is about 7 times lower than that of TG-MOSFET. It means that PSGT-MOSFET exhibits a quick transition during switched on-off. Furthermore, the HF-FOM (C_{rss} × R_{on}) of PSGT-MOSFET has been calculated [54], and found to be 48 mΩ.pF, which is 10 times larger than that of TG-MOSFET. The improved HFOM shows a reduction in total power loss.

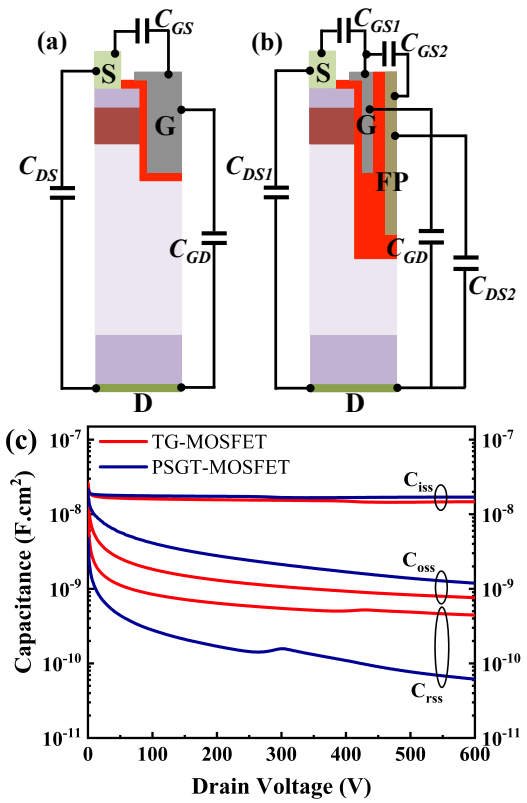

FIGURE 10. Parasitic capacitances of (a) TG-MOSFET, (b) PSGT-MOSFET, and (c) TCAD simulated CV characteristics.

VI. SWITCHING ANALYSIS

In Fig. 11(a), the mixed-mode simulation is incorporated to study the switching performance with the help of a double-pulse test circuit. The switching characteristics of the device under test (DUT), i.e., TG-MOSFET and PSGT-MOSFET, have been studied using an inductive load (L_1 = 100 μH). This inductive load and the freewheeling GaN schottky barrier diode (SBD) are connected in parallel. The GaN SBD is effective for higher switching speeds and low recovery [8], [55]. The gate pulse voltage (V_g) of 10 V is applied with an external gate resistance (R_g) of 1 Ω and a drain voltage (V_d) of 480 V [56]. The turn-off time is expressed in terms of turn-off delay time (from $\sim$90% of V_g to $\sim$10% of V_d), and the fall time (from $\sim$10% of V_d to $\sim$90% of V_d). Whereas, the turn-on time is expressed in terms of the turn-on delay

time (from ∼10% of V_g to ∼90% of V_d), and the rise time (from ∼90% of V_d to ∼10% of V_d) [57], as given in Fig. 11(b). We have been extracted the turn-off time at the falling edge of the first pulse, and the turn-on time at the rising edge of the second pulse, respectively, as shown in Fig. 12, and Fig. 13. Fig. 12(a) displays the TG-MOSFET switching transitions during the turn-off mode. The obtained turn-off delay time [t_d(off)] is 0.06 μs, and fall time (t_f) is 0.08 μs. Fig. 12(b) displays the PSGT-MOSFET switching transitions during turn-off mode. The obtained t_d(off) is 0.05 μs, and t_f is 0.04 μs. The total turn-off time of PSGT-MOSFET is about 1.5× faster compared to the TG-MOSFET. Next, Fig. 13(a) displays the TG-MOSFET switching transitions during turn-on mode. The obtained turn-on delay time [t_d(on)] is 0.02 μs, and rise time (t_r) is 0.05 μs. Fig. 13(b) shows the PSGT-MOSFET switching transitions during turn-on mode. The obtained t_d(on) is 0.01 μs, and t_r is 0.02 μs. The total turn-on time of PSGT-MOSFET is about 2× faster compared to the TG-MOSFET. The total switching energy loss (E_{SW}) of the DUTs has been calculated by integrating V_d, and I_d waveforms over the time interval between turn-off, and turn-on as shown in (1), and (2), respectively [58]. The turn-off (E_{off}), and turn-on (E_{on}) energy is extracted when the load current reaches at 23 A. Fig. 14 compares the energy loss components of the PSGT-MOSFET and TG-MOSFET counterparts. The extracted energy losses of TG-MOSFET during E_{on} and E_{off} transients are 41.9 μJ, and 1290 μJ, respectively. The extracted energy losses of PSGT-MOSFET during E_{on} and E_{off} transients are 10.9 μJ, and 702 μJ, respectively. The total energy loss during turn-on, and turn-off time of PSGT-MOSFET is around 2× less than TG-MOSFET. Finally, the total power loss (P_{SW}) is calculated as a function of total switching loss, and respective frequency as

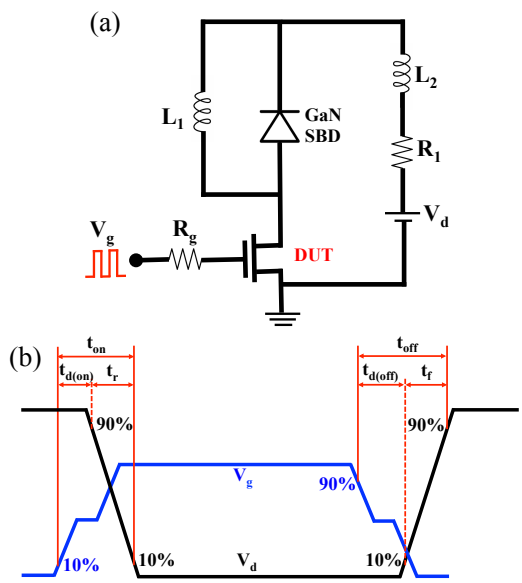

FIGURE 11. (a) Switching test circuit using DUT, and (b) Double pulse based graph definition of switching times.

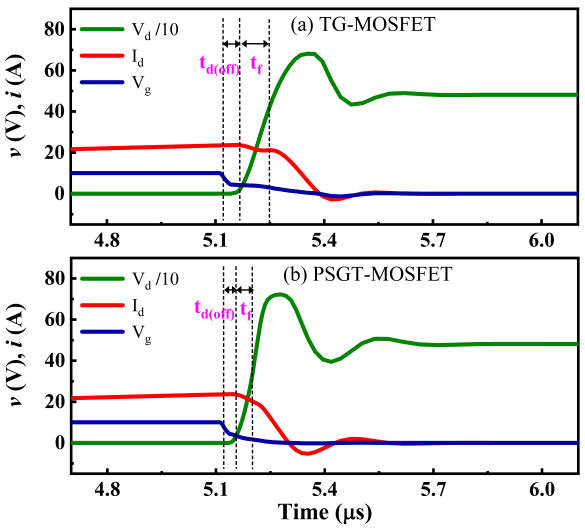

FIGURE 12. Turn-off switching times of TG-MOSFET, and PSGT-MOSFET.

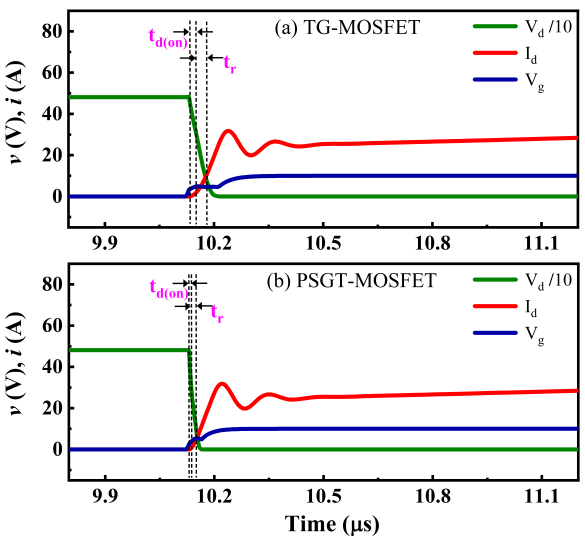

FIGURE 13. Turn-on switching times of TG-MOSFET, and PSGT-MOSFET.

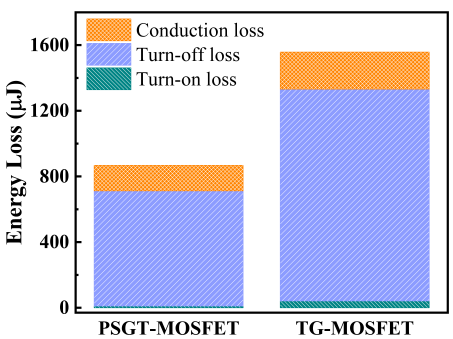

FIGURE 14. Energy loss components of both the devices.

shown in (3) [46]. The P_{SW} for PSGT-MOSFET is found to be 144 W, which is ∼45% better compared to TG-MOSFET. Because of its low power loss, the PSGT-MOSFET can be

employed in power conversion systems with high efficiency. Table 3 contains an outline of the most important parameters.

$$E_{off} = \left[\int_0^{t_d(off)+t_f} V_d(t).I_d(t)dt\right] \quad (1)$$

$$E_{on} = \left[\int_0^{t_d(on)+t_r} V_d(t).I_d(t)dt\right] \quad (2)$$

$$P_{SW} = (E_{on} + E_{off}).f \quad (3)$$

TABLE 3. An outline of the most important parameter of both devices

Parameter	TG-MOSFET	PSGT-MOSFET
R_{on} (mΩ.cm^2)	1.17	0.79
V_{br} (V)	623	650
BFOM (MW/cm^2)	331	534
E_{ox} (MV/cm)	3.58	2.95
C_{rss} (pF/cm^2)	444	61
HF-FOM ($C_{rss} \times R_{on}$) (mΩ.pF)	519	48
t_f (μs)	0.08	0.04
$t_d(off)$ (μs)	0.06	0.05
t_r (μs)	0.05	0.02
$t_d(on)$ (μs)	0.02	0.01
E_{on} (μJ)	41.9	10.9
E_{off} (μJ)	1290	702
E_{SW} (μJ)	1331.9	712.9
P_{SW} (W)	266	144

VII. CONCLUSIONS

The switching characteristics of a 600 V GaN vertical PSGT-MOSFET have been presented for the first time and compared to a conventional TG-MOSFET using the TCAD simulator. The parallel split gate technology consists of two thin parallel gates that have been aligned with gate oxide. Additionally, a field plate has been introduced vertically in between the gate electrodes, and connected to the source. It has been attributed to the (i) greater drift doping concentration and (ii) reduced surface E-field effect by thick bottom oxide. Hence, it causes a reduction in R_{on} without impacting on breakdown voltage. The simulation shows that the R_{on} of PSGT-MOSFET has decreased by nearly $\sim$32% compared to that of a TG-MOSFET. In comparison with similar rated conventional devices, the proposed device shows $10\times$ improvements in the HF-FOM ($C_{rss} \times R_{on}$). Furthermore, when simulated employing in mixed mode, the switching characteristics of PSGT-MOSFET demonstrate decreased switching losses at turn-off as well as turn-on transients. By comparing E_{SW}, it is found that PSGT-MOSFET shows $1.5\times$ faster switching transient and $2\times$ lower energy loss as compared to TG-MOSFET. The total power loss for PSGT-MOSFET is calculated to be $\sim$45% lower than that of a TG-MOSFET while operating in the same frequency range. However, in the PSGT-MOSFET fabrication process, challenges might exist due to the absence of stop layer where etching should be terminated. The addition of a P^+ shielding pinch structure and/or a P^+ shielding layer at trench bottom can potentially reduce the electric field. The improved performance of the PSGT-MOSFET would be expected to have a significant contribution to high power conversion used in the automotive applications.

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