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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2019.2920257

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2920257, IEEE Transactions on Power Electronics

An Overview of Capacitive DC Links-Topology Derivation and Scalability Analysis

Haoran Wang, *Member*, Huai Wang, *Senior Member*, *IEEE*, Guorong Zhu, *Senior Member*, *IEEE*, and Frede Blaabjerg, *Fellow*, *IEEE*

***Abstract*—Capacitive DC links are widely used in Voltage Source Converters (VSC) for power balance, voltage ripple limitation, and short-term energy storage. A typical solution which uses Aluminum Electronic Capacitors (E-cap) for such applications is assumed to be one of the weakest links in power electronic systems, therefore, also becoming one of the lifetime bottlenecks of power electronic systems. Various passive and active capacitive DC-link solutions have been proposed intending to improve the reliability of the DC links qualitatively, making great effort to diverting the instantaneous pulsating power into extra reliable storage components. In this publication, a generic topology derivation method for single-phase power converters with active capacitive DC link integrated has been proposed, which can derive all existing topologies, and identify a few new topologies. According to the synthesis results, the main achievements in research on capacitive DC-link solutions are reviewed and presented chronologically as well as thematically ordered. Further more, the reliability-oriented design procedure is applied to size the chip area of active switching devices and the passive components to fulfill a specific lifetime target and system specification, as well as compare the overall capacitive energy storage, energy buffer ratio, and the cost of different solutions. The cost comparisons are performed with a scalable lifetime target and power rating. It reveals that different conclusions can be drawn with different lifetime targets in terms of cost-effectiveness.**

I. Introduction

Capacitive DC links are widely used in Voltage Source Converters (VSC) for power balancing, voltage ripple limitation, and short-term energy storage. E-cap bank is the good candidate to buffer the pulsating power between the DC and AC side in industry applications due to their relatively high energy density and low cost [1]. However, because of the significant Equivalent Series Resistance (ESR) in the capacitor, the ripple current flowing pass will introduce higher thermal stress which will accelerate the degradation process of the E-cap. They are assumed to be one of the weakest links in power electronic systems, and therefore also becoming one of the lifetime bottlenecks in power electronic systems [2–5].

Research efforts have been made to either reduce the capacitor ripple current stresses or relaxing the required DC-link capacitances. The different categories of the capacitive DC links is shown in Fig. 1, and can be classified into passive and active solutions. Passive capacitive DC-link solutions include passive filters (e.g., additional resonant passive filter to absorb the ripple) [6–12], the control strategies for two stage capacitive DC-link systems, which is relied on a specific relationship in the operating frequency between the converters connected, and the interleave structures based passive filter control methods [13–28]. Active capacitive DC links introduce the additional separate circuit to the existing DC-link. Therefore, extra circuit paths including separate auxiliary circuit and integrated auxiliary circuit are provided to process the pulsating power, which otherwise would be fully processed by the DC-link capacitors. The separate auxiliary circuit could be DC-DC converter [29–52], DC-AC converter [53–65], or other structures [66–92] The integrated auxiliary circuits are novel single-phase topologies with integrating the active DC link, such as [93–114].

Recently, some review papers have been published to make an overview and comparisons on these capacitive DC links. [115] reviews the power decoupling techniques to release DC links for micro-inverters in PV (Photovoltaics) application qualitatively and it is mainly focusing on the isolated topologies. Different from that, from the aspect of development and construction laws of power decoupling topologies, [116] reviews the topologies with integrated active DC link in both current source and voltage source converter. It classified these solutions into independent and dependent topologies and found out several independent topologies can be derived from dependent topologies by sharing the common switches and passive components. The latest publication [117] presents a comprehensive overview which covers the isolated and non-isolated cases, voltage and current source, and considering control and circuits. While the review papers on the active DC links have the above potential benefits, there are the following limitations of the existing studies on active capacitive DC-links methods:

1) Even though [115], [116], and [117] have reviewed and

This work was supported by the Innovation Fund Denmark through the Advanced Power Electronic Technology and Tools Project and the National Natural Science Foundation of China under Grant (No. 51777146).

Partial results of this manuscript have been presented at the IEEE Energy Conversion Congress and Exposition (ECCE) 2016 and IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia) 2016, sponsored by power electronics society.

Haoran Wang, Huai Wang and Frede Blaabjerg are with Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (hao@et.aau.dk, hwa@et.aau.dk and fbl@et.aau.dk)

Guorong Zhu is with School of Automation, Wuhan University of Technology, China (zhgr_55@whut.edu.cn).

listed these methods, the derivation of these novel topologies is not clearly. It is worth to be deeply investigated, because it can illustrate the essence of these single-phase topologies with active DC link and maybe provide more possibilities.

2) There is still a lack of quantitative reliability analysis of the system with active DC link. The reliability improvement of the DC-link capacitor itself (i.e., by reducing its ripple current stress or replacement by a more reliable alternative) does not necessarily imply the improvement of the overall system, since active switches and other components are added with the active capacitive DC links. The lifetime of other components may therefore be changed.

3) It is still an open question to conclude, which active capacitive DC link is the most promising one. Existing comparative studies are based on either the number of components used, different case studies, or different criteria to size the components [115–117]. No assessment of the existing active capacitive DC links based on a specific case is done for a given lifetime target and the same component sizing criteria.

In order deeply to investigate the original ideas of these capacitive DC-link solutions, this paper proposes a generic topology derivation method to synthesis single-phase converter with integrated auxiliary circuit, which can review all the existing single-phase topologies with active DC link integrated [118]. Based on the synthesis results, the main achievements in research on capacitive DC-link solutions are reviewed and presented chronologically and thematically ordered, so as to clearly understand the development trend of the capacitive DC-link solutions. Moreover, an assessment approach of active capacitive DC links is proposed based on the overall cost of the respective solution to fulfill the same specifications in terms of functionality and lifetime [119]. The methods studied will be also applicable also to three-phase systems with unbalanced grids or loads [120] (i.e., there will be low-frequency harmonics, requiring large size capacitors).

The structure of this paper is as follows: Section II discusses the generic topology derivation method and the cases studied, followed by the summary of the main achievements in Section III. Section IV presents the proposed cost-benchmarking based on a reliability-oriented component sizing procedure; then, the cost-benchmarking and scalability analysis are presented in Section V. The performance factors assessment is shown in Section VI, followed by the conclusions in Section VII.

II. Generic Topology Derivation Method for Single-phase Converter with Capacitive Active DC Links

Through the power flow analysis, four general structures for decoupling the pulsating power at AC and DC sides can be obtained to provide an additional power flow path from the main circuit to the active energy storage elements. Based on the general structures, four synthesis modes to combine the main circuit and auxiliary circuit are presented, followed by enumerating all the possible topologies. In order to reduce the component count, the main circuit and the active capacitive DC-link circuit could share common elements in some of the derived topologies, which will be discussed later with examples.

A. Power Flow Analysis

The AC voltage $v_{\rm ac}(t)$ and current $i_{\rm ac}(t)$ are assumed to be sinusoidal with unity power factor, as shown in the following equations

$$v_{\rm ac}(t) = V_{\rm m}\sin(\omega t) \tag{1}$$

$$i_{\rm ac}(t) = I_{\rm m}\sin(\omega t) \tag{2}$$

where $V_{\rm m}$ and $I_{\rm m}$ are the amplitude of AC voltage and current, respectively; and ω is the supply angular frequency. Limit in the discussion to low-frequency harmonics, the power of the AC side can be expressed as follows:

$$p_{\rm ac}(t) = v_{\rm ac}(t)i_{\rm ac}(t) = \frac{V_{\rm m}I_{\rm m}}{2} - \frac{V_{\rm m}I_{\rm m}}{2}\cos(2\omega t) \tag{3}$$

There are two parts in (3), the first part is the DC power supplied by the DC source $P_{\rm dc}$ and the second part is the instantaneous unbalanced power $p_{2\omega}(t)$ which needs a storage component to buffer, such as inductor, capacitor and source (battery).

- Capacitor: Such as film capacitor and ceramic capacitor, which is widely used for power decoupling because of the great current capability [3].
- Inductor: Magnetic components are much more reliable and feature low failure rates that are more than one order of magnitude lower than those of the other power devices. But the high power loss and large volume/weight limit its extensive use [2].
- Source: Battery can also be used for power decoupling and long hold-up time support.

Focus in this paper is on the capacitor as the energy storage element in order to buffer the pulsating power. Inductor and battery as storage component can replace the film capacitor for specific DC-link applications with similar design procedure, which is not discussed in this paper.

For passive capacitive DC links, E-caps are usually used to filter low-frequency ripple current components, and additional capacitors with higher resonant frequency (e.g., film capacitors, ceramic capacitors) are usually used to assist the filtering of the high-frequency ripple current components. The one used for low-frequency ripple current filtering is the dominant one in terms of capacitance. An alternative solution is to use single-type of capacitors, such as film capacitors, or ceramic capacitors to filter both low-frequency and high-frequency ripple current components. For active DC-link solutions, additional active circuits (or modulation schemes) are mainly used to supply or absorb low-frequency power components due to the limitation of controller bandwidth. Capacitors for high-frequency ripple components filtering are still required in the DC link of the power electronic converter.

B. General Structure

Fig. 2 defines the terminals of the main circuit of a single-phase power converter and the auxiliary circuit used for the active capacitive DC link. There are ports AB and CD for the main circuits, and $A_{\rm aux}B_{\rm aux}$ and $C_{\rm aux}D_{\rm aux}$ for the auxiliary circuits. AB and CD could either be alternating current (AC) or direct current (DC), depending on the applications. For

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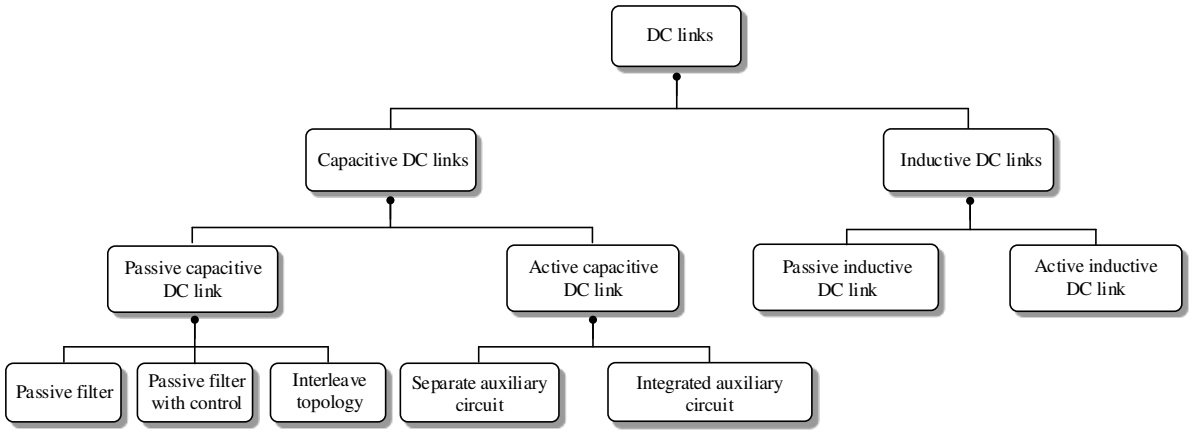

Fig. 1. Categorization of DC links in power electronic systems.

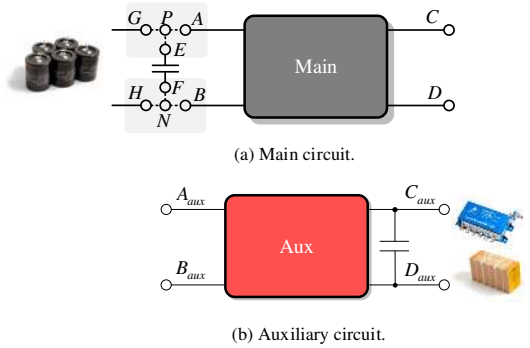

Fig. 2. Basic module for the main circuit and the auxiliary circuit.

illustration, Fig. 2 shows an inverter application case. EF and GH are the terminals of the DC-link capacitor and the input of the main circuit, respectively. Typically, without any auxiliary circuit, G, E, A are connected to P and the same to the terminal H, F, B, N.

By analyzing the possible flowing paths of the pulsating power, the general structures for a single-phase system with an auxiliary circuit can be divided into four types: DC series, DC parallel, AC series, and AC parallel.

1) DC Series: In the DC series structure, the auxiliary circuit and the main circuit are connected in series at the DC side in order to compensate the voltage distortion of the DC-link capacitor. From the basic module shown in Fig. 2, it can be seen that there are three ways to connect the auxiliary circuit in series with the DC port of the main circuit. Taking the positive side terminals as an example, the three connected locations are PA at converter side, PE at the capacitor side and PG at the input side as shown in Fig. 3 (a), (b) and (c) separately in order to keep each side constant. It is worth to mention that two auxiliary circuits are required at PA and PG if it is necessary to limit the voltage ripples at both the input side and the converter side.

With the responsibility to decouple the unbalanced power, the auxiliary circuit can either be the AC/DC, which contains only AC component at the $A_{\rm aux}B_{\rm aux}$ or the DC/DC and DC/AC converter which contain both DC and AC components. In such AC/DC auxiliary circuit application, the voltage across $A_{\rm aux}B_{\rm aux}$ has the inverse ripple component of the DC-link capacitors in single-phase system, so the average DC-link voltage of the single-phase system is constant. However, in DC/DC and DC/AC applications, except for an AC component, there will be a DC component in the $A_{\rm aux}B_{\rm aux}$ port of auxiliary circuit.

2) DC Parallel: This structure inserts an auxiliary circuit connected in parallel to the DC-link capacitors, which will introduce a new flowing path for the ripple current at the DC link. The voltage of the input port $A_{\rm aux}B_{\rm aux}$ of the auxiliary circuit is clamped by the DC link. Thus the auxiliary circuit can be DC/AC or DC/DC converters with a DC input. Terminal G, E, A are connected to P and the same to the terminal H, F, B, N as defined in Fig. 3 (d).

3) AC Series: The auxiliary circuit is connected in series with the AC side of the main circuit, as shown in Fig. 3 (e).

4) AC Parallel: The auxiliary circuit is connected in series with the AC side of the main circuit. It has the similar function as an active power filter in order to eliminate the harmonics at the AC side. The voltage of the $A_{\rm aux}B_{\rm aux}$ port is clamped by the AC voltage of the main circuit. Thus the topologies of the auxiliary circuit is AC/DC as shown in Fig. 3 (f).

C. Synthesizing from General Structures

The original cells for a single-phase system with active capacitive DC links are the main circuit and the auxiliary circuit. In order to reduce the component count and derive more possible topologies with active capacitive DC-links, a topology synthesis which links the output terminals of the auxiliary circuit to the main circuit is presented. Because of some novel connections for power flowing, more possibilities to share the common cells for higher power density will be provided. Following the general structure for single-phase system with the auxiliary circuit integrated presented above, four kinds of synthesis modes are presented in Fig. 4 and this can be used for the topology derivation:

1) Hang mode: Hang up the $C_{\rm aux}D_{\rm aux}$ port without any connection;

2) Float mode: Connect one terminal of the energy storage element to one of the terminals of the main circuit;

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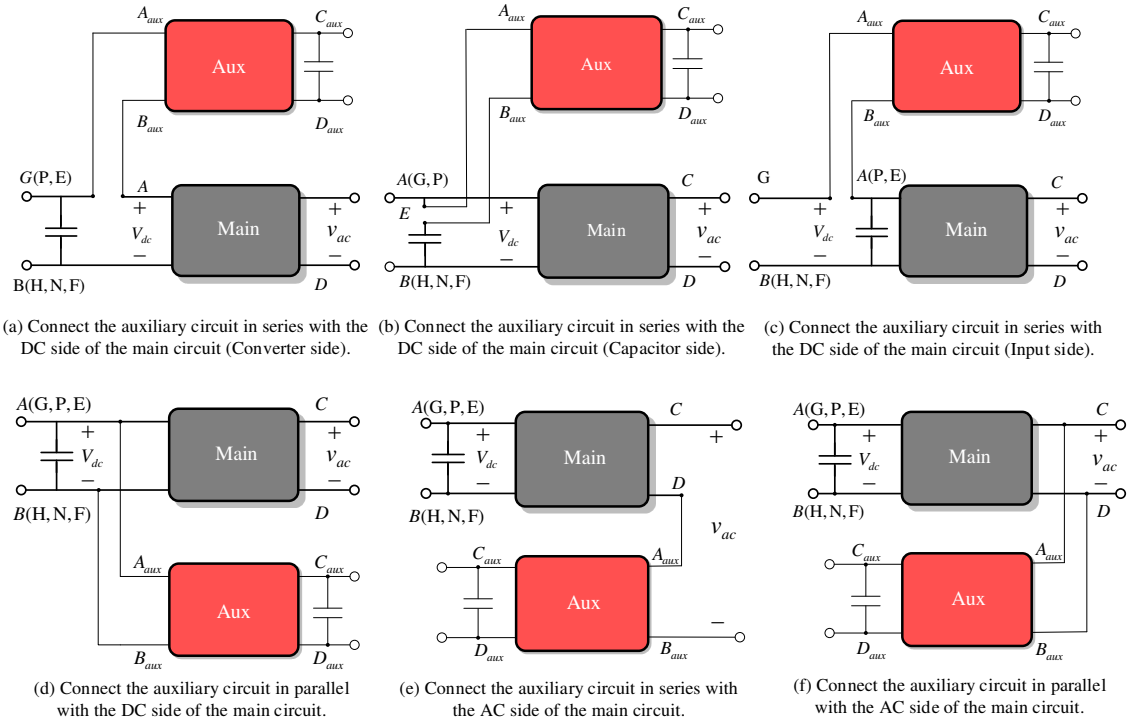

(a) Connect the auxiliary circuit in series with the DC side of the main circuit (Converter side).

(b) Connect the auxiliary circuit in series with the DC side of the main circuit (Capacitor side).

(c) Connect the auxiliary circuit in series with the DC side of the main circuit (Input side).

(d) Connect the auxiliary circuit in parallel with the DC side of the main circuit.

(e) Connect the auxiliary circuit in series with the AC side of the main circuit.

(f) Connect the auxiliary circuit in parallel with the AC side of the main circuit.

Fig. 3. Structure diagrams of the auxiliary circuit connected with the main circuit.

3) Parallel mode: Connect two terminals of the energy storage element and two terminals of the main circuit together;

4) Series mode: Link the energy storage element in series with one of the terminals of the main circuit.

D. Topology Simplification

The objective of the topology simplification is to reduce the component count in synthesis structure. An example to illustrate the simplification procedure can be seen in Fig. 5 and Fig. 6. The black and red line are the main circuit and auxiliary circuit, respectively. The dashed line is shared by a common cell. A step-by-step topology simplification procedure is discussed as follows:

1) First, the full-bridge inverter as the main circuit with another full-bridge inverter as the auxiliary circuit are taken as an example. $A_{\rm aux}B_{\rm aux}$ port of the auxiliary circuit parallelled with the DC link of the main circuit and $C_{\rm aux}D_{\rm aux}$ port series with one of AC terminals of main circuit are used in this example, as shown in Fig. 4 (d).

2) The topology has four legs as shown in Fig. 5. Each switching leg generates a square-wave voltage from the DC link. From the average model shown in Fig. 6, it can be seen that the legs $V_{\rm aux}$ and U have the same structure and the common DC-link input and output terminals $CD_{\rm aux}$.

3) Merge the leg $V_{\rm aux}$ into the leg U of the main circuit. The common switching cells and filter inductors can be shared by the main circuit and the auxiliary circuit.

4) The AC port voltage of the single-phase conversion system is not the AC voltage of main circuit, but the sum of the output voltages of the main circuit and the auxiliary circuit. Thus, the modulation strategy for the single-phase system must be changed, where the difference between the middle voltages of the leg $U_{\rm aux}$ and leg V is the AC voltage of the single-phase system.

A more general description of the topology simplification from the aforementioned analysis is as follows:

1) Select two topologies with one of the general structures to establish an additional power flow path for the pulsating power;

2) Check the possibility to share components (e.g., bridge legs) between the main circuit and the auxiliary circuit;

3) If it is applicable, integrate the components that can be shared by the main circuit and the auxiliary circuit;

4) Exclude the circuit topologies that do not work in principle;

5) Check the controllability for single-phase conversion and rebuild the modulation strategy to ensure the circuit are fully controllable.

It should be noted that some topologies derived from the synthesis method do not work in principle. Two examples are shown in Fig. 7. In Fig. 7 (a), when connect terminal A and $C_{\rm aux}$, the energy storage element is connected in parallel with the DC link directly. The voltage of the capacitor cannot be controlled by the power semiconductors in the auxiliary circuit. Moreover, the inductor in the auxiliary circuit is a filter inductor, which has limited energy storage capability, so the $S_{\rm aux1}$ is short circuited. In Fig. 7 (b), the terminal $C_{\rm aux}$ and B are connected, which makes the energy storage capacitor short circuit.

E. Topology Synthesis Cases

Following the proposed topology synthesis process, the full-bridge is taken as an example for the main circuit topology.

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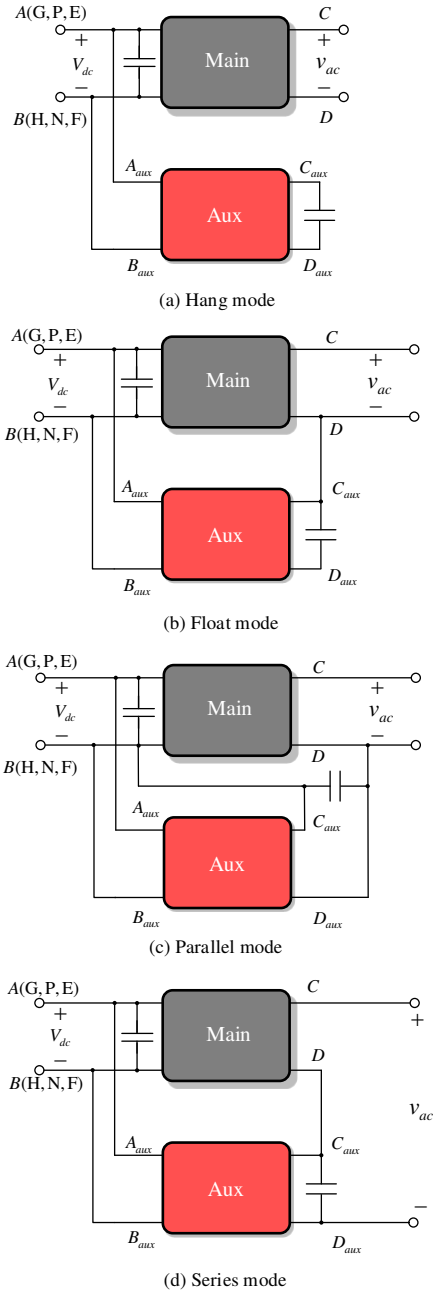

Fig. 4. Synthesis modes for the DC parallel case shown in Fig. 3 (d).

Full-bridge, half-bridge, buck, boost and buck-boost converters are taken as the auxiliary circuits connected in parallel or series at the DC or AC side. The synthesis results of the DC parallel, DC series, AC parallel and AC series are shown below separately.

1) DC parallel: The synthesis results of the DC parallel cases are shown in Table I. There exist 20 derived topologies excluding the ones that do not work in principle. Actually, the half-bridge inverter as the main topology with these auxiliary circuits have also been taken into account, and all the topologies with component reduced have been included in the above examples.

As there are common cell in parallel with the DC link,

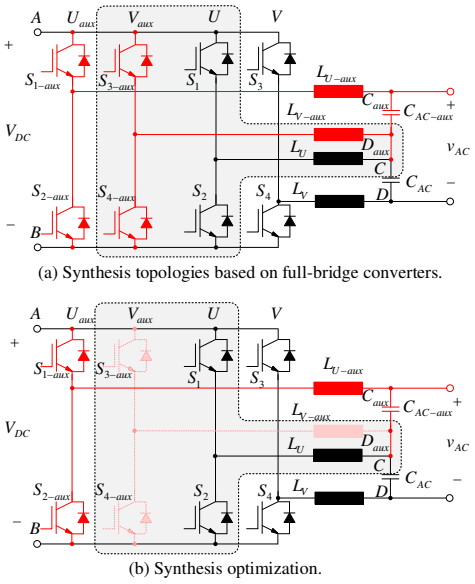

Fig. 5. Example of synthesis optimization based on full-bridge converters.

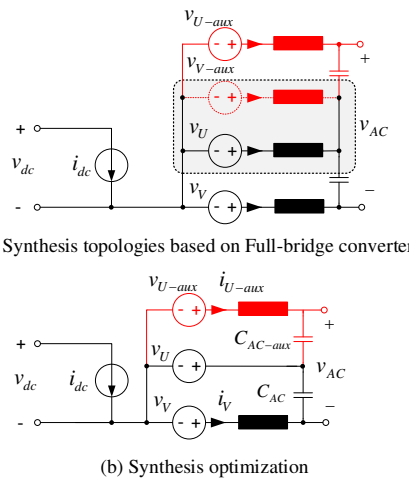

Fig. 6. Average model of the example of synthesis optimization.

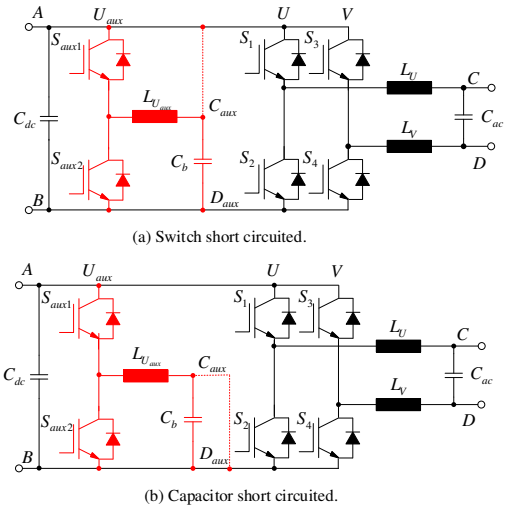

Fig. 7. Two topology examples that do not work following the principle in synthesis procedure.

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TABLE I
SYNTHESIS RESULTS WITH DC PARALLEL MODE.

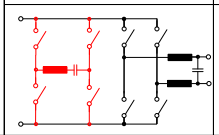
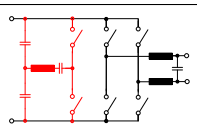
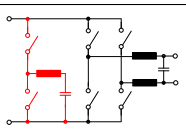
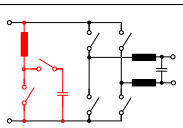
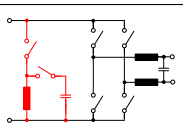
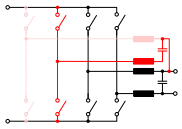
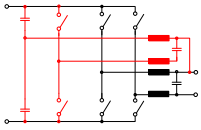
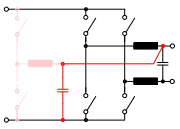
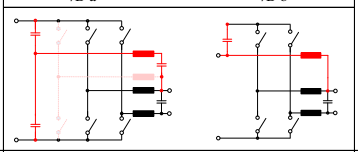
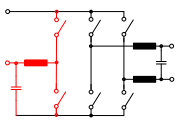
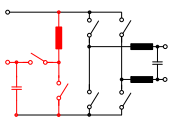
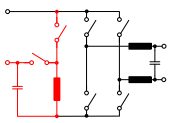
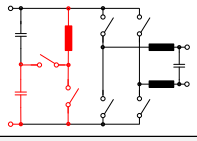
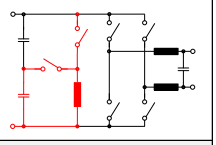
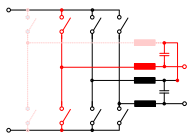
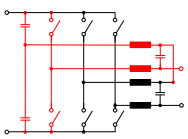
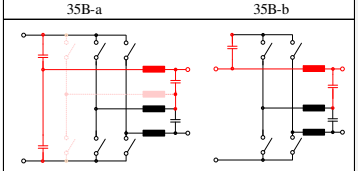
Main circuit topology (black)			Full-bridge				
Auxiliary circuit topology (red)			Full-bridge	Half-bridge	Buck	Boost	Buck-boost
			A	B	C	D	E
Hang mode		1	1A 	1B 	1C 	1D 	1E 
Float mode	A-C_{aux}	2	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	A-D_{aux}	3	swtich short circuit	swtich short circuit	1C	1D	1E
	B-C_{aux}	4	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-D_{aux}	5	swtich short circuit	swtich short circuit	1C	1D	1E
	C-C_{aux}	6	6A 	6B 	6C 	swtich short circuit	swtich short circuit
	C-D_{aux}	7	6A	7B-a 7B-b 	1C	1D	1E
	D-C_{aux}	8	6A	6B	6C	swtich short circuit	swtich short circuit
	D-D_{aux}	9	6A	7B	1C	1D	1E
Parallel mode	A-C_{aux}, B-D_{aux}	10	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	A-C_{aux}, C-D_{aux}	11	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	A-C_{aux}, D-D_{aux}	12	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-C_{aux}, A-D_{aux}	13	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-C_{aux}, C-D_{aux}	14	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-C_{aux}, D-D_{aux}	15	swtich short circuit	cap short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	C-C_{aux}, A-D_{aux}	16	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	C-C_{aux}, B-D_{aux}	17	swtich short circuit	swtich short circuit	6C	swtich short circuit	swtich short circuit
	C-C_{aux}, D-D_{aux}	18	swtich short circuit	7B	swtich short circuit	swtich short circuit	swtich short circuit
	D-C_{aux}, A-D_{aux}	19	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	D-C_{aux}, B-D_{aux}	20	swtich short circuit	swtich short circuit	6C	swtich short circuit	swtich short circuit
	D-C_{aux}, C-D_{aux}	21	swtich short circuit	7B	swtich short circuit	swtich short circuit	swtich short circuit
Series mode	A-C_{aux}, P-D_{aux}	22	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	A-D_{aux}, P-C_{aux}	23	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-C_{aux}, N-D_{aux}	24	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	B-D_{aux}, N-C_{aux}	25	swtich short circuit	swtich short circuit	25C 	25D 	25E 
	E-C_{aux}, P-D_{aux}	26	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	E-D_{aux}, P-C_{aux}	27	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	F-C_{aux}, N-D_{aux}	28	swtich short circuit	swtich short circuit	1B	28D 	28E 
	F-D_{aux}, N-C_{aux}	29	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	G-C_{aux}, P-D_{aux}	30	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	G-D_{aux}, P-C_{aux}	31	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	H-C_{aux}, N-D_{aux}	32	swtich short circuit	swtich short circuit	25C	25D	25E
	H-D_{aux}, N-C_{aux}	33	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit	swtich short circuit
	C-C_{aux}	34	34A 	34B 	swtich short circuit	swtich short circuit	swtich short circuit
	C-D_{aux}	35	35A	35B-a 35B-b 	swtich short circuit	swtich short circuit	swtich short circuit
	D-C_{aux}	36	36A	35B	swtich short circuit	swtich short circuit	swtich short circuit
	D-D_{aux}	37	37A	35B	swtich short circuit	swtich short circuit	swtich short circuit

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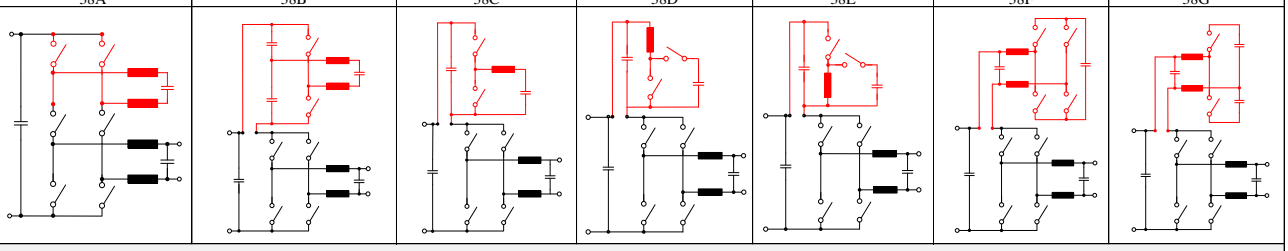
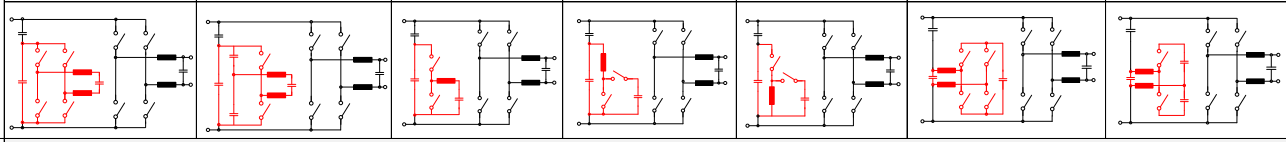
TABLE II
SYNTHESIS RESULTS WITH DC SERIES MODE.

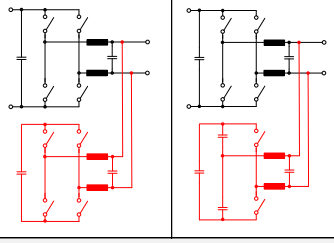
Main circuit topology (black)		Full-bridge						
Auxiliary circuit topology (red)		DC-AC circuit		DC-DC circuit			AC-DC circuit	
		Full-bridge	Half-bridge	Buck	Boost	Buck-boost	Full-bridge	Half-bridge
		A	B	C	D	E	F	G
		38A	38B	38C	38D	38E	38F	38G
Hang mode	38							
Float mode	39	No common cell can be shared						
Parallel mode	40							
Series mode	41							

(a) Connect the auxiliary circuit in series with the DC side of the main circuit (Converter side).

Main circuit topology (black)		Full-bridge						
Auxiliary circuit topology (red)		DC-AC circuit		DC-DC circuit			AC-DC circuit	
		Full-bridge	Half-bridge	Buck	Boost	Buck-boost	Full-bridge	Half-bridge
		A	B	C	D	E	F	G
		42A	42B	42C	42D	42E	42F	42G
Hang mode	42							
Float mode	43	No common cell can be shared						
Parallel mode	44							
Series mode	45							

(b) Connect the auxiliary circuit in series with the DC side of the main circuit (Capacitor side).

TABLE III
SYNTHESIS RESULTS WITH AC PARALLEL MODE.

Main circuit topology (black)		Full-bridge	
Auxiliary circuit topology (red)		Full-bridge	Half-bridge
		A	B
		46A	46B
Hang mode	46		
Float mode	47	No common cell can be shared	
Parallel mode	48		
Series mode	49		

most of the existing topologies mentioned in recent papers are belonging to this synthesis mode. As shown in Table I, the topologies 1A, 1B, 1C, 1D, and 1E include a full-bridge converter [53], a half-bridge converter [60], a buck converter [44], a boost converter [35], and a buck-boost converter [50] as the auxiliary circuit connected in parallel with the DC link, respectively. Some topologies can share the common cell between the main circuit and the auxiliary circuit, such as 6A [95], 7B [112], 6C [111] and 34A [93]. All of these typical topologies will be evaluated in following section.

2) DC series: For the converter side cases, the synthesis results can be seen in Table II (a). When the auxiliary circuit is DC/AC or DC/DC topology, besides an AC component, there will be a DC component in $A_{\text{aux}}B_{\text{aux}}$, which will lower the voltage utilization ratio of the main circuit. Here, the five auxiliary circuits with DC input are taken as examples to derive the topologies as presented in Table II. By sharing the common cells at the DC link, the topology 38A can be derived, which has been proposed in [105]. When the auxiliary circuit

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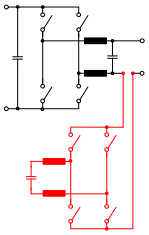
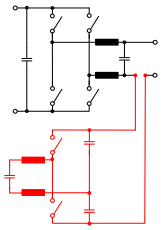
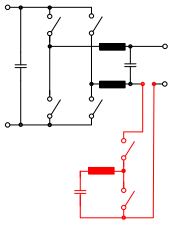
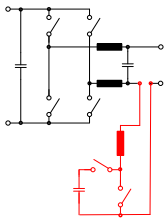
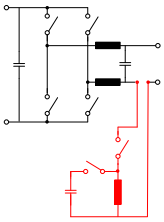
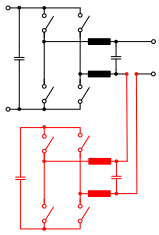
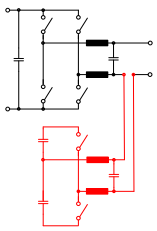
TABLE IV
SYNTHESIS RESULTS WITH AC SERIES MODE.

Main circuit topology (black)		Full-bridge						
Auxiliary circuit topology (red)		DC-AC circuit		DC-DC circuit			AC-DC circuit	
		Full-bridge	Half-bridge	Buck	Boost	Buck-boost	Full-bridge	Half-bridge
		A	B	C	D	E	F	G
		50A	50B	50C	50D	50E	50F	50G
Hang mode	50							
Float mode	51	No common cell can be shared						
Parallel mode	52							
Series mode	53							

is AC/DC topology, the voltage of $A_{\rm aux}B_{\rm aux}$ has the inverse voltage waveform with the ripple component of the DC-link capacitor, in order to achieve a constant DC-link voltage. The full-bridge inverter for main circuit and the full-bridge and half-bridge converters for auxiliary circuits are taken as examples to synthesis single-phase topology with integrated active DC link.

Except for the hang up mode, no more single-phase topology with integrated auxiliary circuits can be obtained, because there is no common cell that can be shared at the DC link. Similar synthesis results can be found for capacitor side cases as shown in Table II (b).

3) AC parallel: In this case, the auxiliary circuit is connected in parallel with the AC side of the single-phase inverter [121]. The derived topologies are shown in Table III. Because no common cell can be shared, no more novel topologies can be derived.

4) AC series: Different from the above three modes whose AC side votlage is CD, the AC voltage of the conversion system becomes the sum of CD and $A_{\rm aux}B_{\rm aux}$. The derived topologies are shown in Table IV with a full-bridge inverter as the main circuit and various auxiliary circuits. In this section, the output voltage of the main circuit contains other AC or DC components besides the fundamental component. Thus, the CD port of the main circuit is different from the traditional one. The auxiliary circuit could be AC/DC topologies or DC/DC (DC/AC) topologies. One of the cases proposed in [91] connects a buck converter in series with the AC side, while the topology and modulation strategy for the main circuit need to be changed.

III. MAIN ACHIEVEMENTS OF CAPACITIVE DC-LINK RESEARCH

In the academic community, research on the capacitive DC-link design has been performed for more than two decades and is still very popular, given the number of papers published on this topic every year. The solutions to eliminate $p_{2\omega}(t)$ from DC and AC side can be divided into two categories: the passive solutions and active solutions as shown in Fig. 1, which depends on whether an additional auxiliary circuit is needed or not. The main achievements in capacitive DC-link research are shown in Fig. 8 chronologically as well as thematically. Key solutions indicate novel topologies or concepts and important solutions represent contributions of control and optimization for different applications, which are based on the key solutions. According to the summary of the main achievements is presented in Table. V. The first two categories are passive solutions which includes passive filter and interleave structure. The other two categories are active solutions which includes separate auxiliary circuit and integrated auxiliary circuit.

IV. COMPONENT SIZING PROCEDURE FOR BENCHMARKING OF CAPACITIVE DC-LINK SOLUTIONS

In order to keep same specification to existing solutions for benchmarking, a reliability-oriented design procedure is incorporated to size the capacitor and power semiconductor considering the same operating performance and lifetime target. For the inductor, Total Harmonic Distortion (THD) is considered to size the inductor.

A. Capacitor

The reliability-oriented procedure to size the capacitors is shown in Fig. 9.

1) Expected Lifetime Definition: The selection of either E-caps or film capacitors should fulfill the lifetime requirement of the overall power conversion system. It should be mentioned that it is possible to select proper E-caps to achieve different lifetime targets by derating the operation conditions. Therefore, in principle, lifetime itself is not the determining factor to decide which type of capacitors that can be used. By considering the respective advantages of E-caps and film capacitors, the type of capacitors selected in the case studies is as follows: E-caps are used for the DC-link capacitor $C_{\rm dc}$

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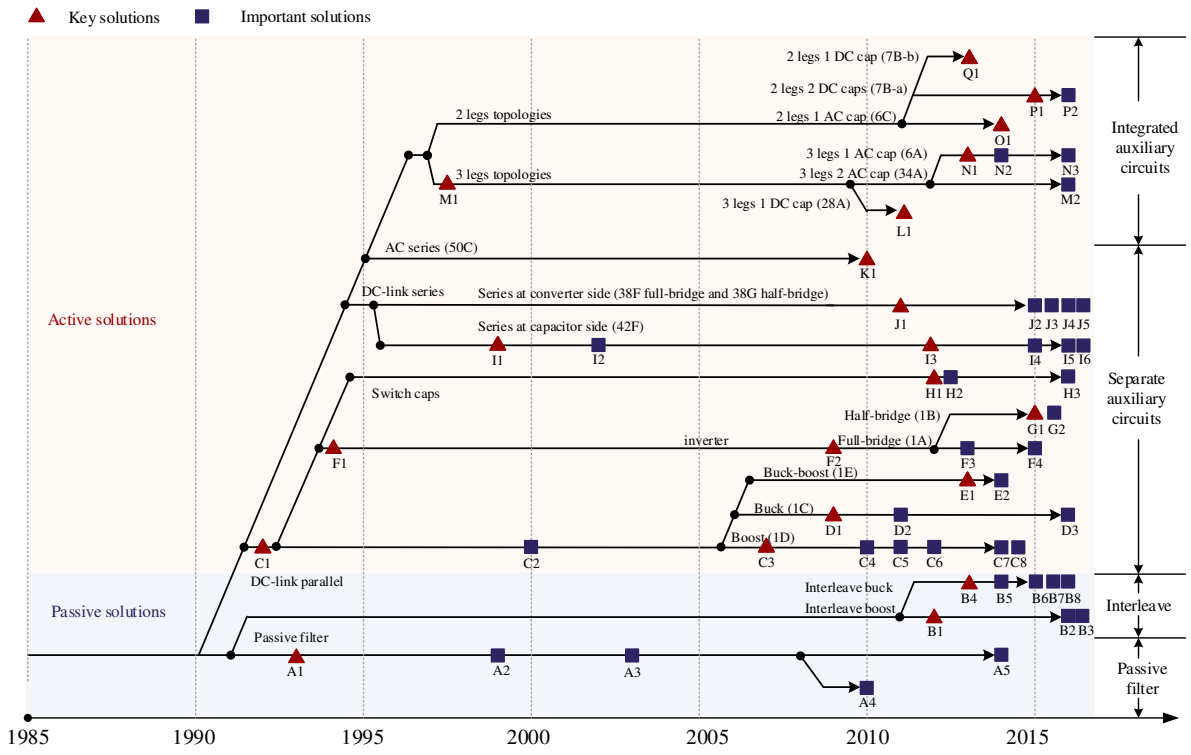

A1. K. Toyama, T. Takeshita et al, LC resonant, 1993.
A2. D. C. Hamill and P. T. Krein et al, saturable inductor, 1999.
A3. J. C. Das, passive filter, 2003.
A4.S. Y. Hui, et al, Passive Offline LED Driver 2010.
A5. M. Vasiladiotis and A. Rufer, control for resonant filters, 2014.
B1. G. R. Zhu, S.C. Tan et al, inverterleave boost, 2012.
B2. D. B. W. Abeywardana,et al, closed-loop control for boost, 2016.
B3. D. B. W. Abeywardana,et al, consider component tolerances, 2016.
B4. I. Serban, invterleave buck, 2013.
B5. S. Li, S. Y. Hui, et al, general interleave, 2014.
B6. I. Serban et al, grid connected with power decoupling, 2015
B7. W. Yao, F. Blaabjerg et al, close-loop control for buck, 2016
B8 W. Yao, F. Blaabjerg et al, robust control scheme, 2016.
C1. H. Irie, T. Yamashita et al, 2-quadrant chopper, 1992.
C2. Garcia, M. D. Martinez-Avial et al, harmonic reducer review, 2000.
C3. A. C. Kyritsis, E. C. Tatakis, boost buffer, 2007.
C4. M. Jang and V. G. Agelidis, battery storage, 2010.
C5. S. Wang, X. Ruan et al, E-cap free in LED, 2011.
C6. M. Jang, and V. Agelidis, Fuel cell system for grid connected, 2012.
C7. W. Cai, S. Duan,et al, virtual capacitor for high efficency, 2014.
C8. Y. Yang, X. Ruan, et al, Feed forward for all the harmonics, 2014.
D1. R. Wang, F. Wanget al, buck buffer with high power density, 2009.
D2. H. Li, K. Zhang, et al, continuous control, 2011.
D3. Z. Kong, K. Zhang, et al, buck buffer for MMC submodule 2016.
E1. K. W. Lee, T. J. Liang, et al, buck-boost buffer, 2013..
E2. X. Cao, Q. C. Zhong, improve stability, 2014.
F1. Y. Wang, DC shunt active filter, 1994.
F2. P. T. Krein, R. S. Balog. Three port for power decoupling, 2009.
F3. Chi Jin, Peng Wang,et al, APF application, 2013.
F4. Y. Tang, F. Blaabjerg et al, PQ control for power decoupling, 2015.
G1. Y. Tang, F. Blaabjerg et al, half bridge buffer, 2014.
G2. Y. Tang, F. Blaabjerg et al, closed-loop control, 2014.
H1. M. Chen, K. K. Afridi et al, Stacked switched capacitor, 2012.
H2. K. Afridi, and D. J. Perreault, Enhanced bipolar stacked, 2012.
H3. C. McHugh et al, high power density implementation, 2016.
I1. T. Tanaka and S. Funabiki, full-bridge series with cap as dc-link, 1999.
I2. T. Tanaka, S. Fujikawa and S. Funabiki, controller for buffer structure, 2002.
I3. Kuang Li, Jinjun Liu,et al, application for harmonics 2006.
I4. S. Qin, buffer sizing and design, 2015.
I5. V. Michal, buck buffer with dc link cap in series. 2016.
I6. H. Wang and H. Wang. Two terminal DC-link series module, 2017.
J1.H. Wang, H. S. H. Chung et al, series rectifier, 2011.
J2. W. Liu, H.S.H.Chung et at, modelling and control, 2015.
J3. Y. Qiu, Y. F. Liu et al, in LED system, 2015.
J4. V. S. P. Cheung, H. Chung et al, scalable multiparallel, 2016.
J5. X. Lyu, D. Cao et al, in series and in parallel buffer, 2016.
K1. B. J. Pierquet and D. J. Perreault, series converter at ac side, 2010.
L1. X. Liu, P. Wang et al, series inverter, 2011.
M1. T. Shimizu et al, three legs 2 ac caps topolog, 1997.
M2. G. Zhu, H. Wang et al, AC power decoupling 2016.
N1. H. Li, K. Zhang et al, three legs 1 ac caps topology, 2013.
N2. R. Chen, F. Z. Peng, modulation to reduce current stress, 2014.
N3. H. Wu, S.-C. Wong, inductor optimization, 2016.
O1. Q. Wenlong, W. Hui, 2 legs with an ac cap, 2014.
P1. Y. Tang and F. Blaabjerg, 2legs with 2 dc caps, 2015.
P2. S. Li, S.-C. Tan et al, modeling and controller design, 2016.
Q1. W. Cai, S. Duan et al, 2 legs boost inverter, 2013.

Fig. 8. Main achievements in capacitive DC-link research.

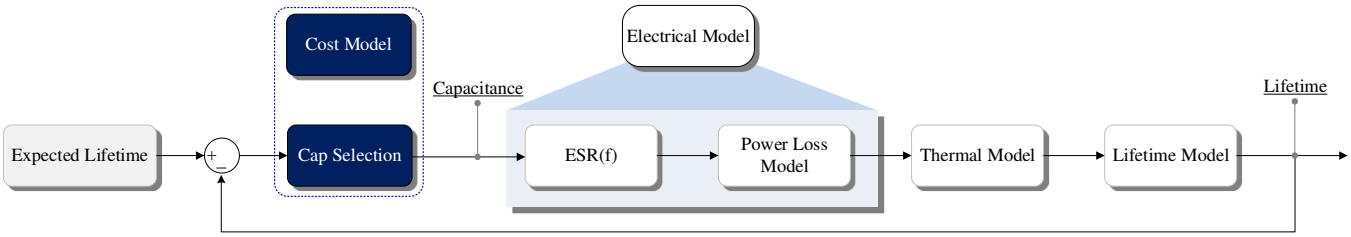

Fig. 9. Capacitor reliability-oriented design to fulfill certain specification.

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TABLE V
MAIN ACHIEVEMENTS SUMMARY.

Category	No	Type	Features	Limitation	Reference
Passive filters (Easy to be implemented becuase of no active devices inside)	A1	Topology	LC resonant filter for low-frequency	Parameter variaration and large volume	[6]
	A2	Topology	Adjust the resonant frequency	Large volume	[7]
	A3	Topology	Review kinds of passive filter for DC-link	Parameter variaration and large volume	[8]
	A4	Topology	Passive component only	High harmonics introduced	[10]
	A5	Control	Controller design consider the DC-link filter		[12]
Interleave structure (Topology born with power decoupling capability)	B1	Topology	Inverter is boost and without large E-cap	High voltage stress for all components	[13]
	B2	Control	Controller design for better dynamic performance		[27]
	B3	Control	Controller design consider tolerance		[28]
	B4	Topology	Full bridge structure is easy to be implemented	Low modulation index	[15]
	B5	Control	Different structure with current waveform control		[17]
	B6	Application	Consider grid code and component sizing		[23]
	B7	Control	Close-loop control consider component tolerance		[26]
	B8	Control	Robust control for differential topologies		[64]
Separate auxiliary circuit (No more change to the main system)	C1	Concept	2-quadrant DC chopper for ripple voltage concept		[30]
	C2	Concept	Review kinds of DC harmonics reducer		[31]
	C3	Topology (1D)	Boost converter for DC-link with small capacitance	High voltage stress and much energy storage	[35]
	C4	Control	Control design for fuel cell system		[36]
	C5	Application	Control design for LED system		[38]
	C6	Application	Control design for fuel cell consider grid code		[40]
	C7	Control	Control design for high efficiency and fast response		[42]
	C8	Control	Feed-forward control for high accuracy ripple mitigation		[43]
	D1	Topology (1C)	DCM buck buffer circuit	Components holds DC-link voltage	[44]
	D2	Control	CCM control for buck buffer circuit		[46]
	D3	Application	Buck buffer circuit for MMC application		[49]
	E1	Topology (1E)	Buck-boost buffer structure	Components holds DC-link votlage	[50]
	E2	Control	Controller optimization for stability		[51]
	F1	Concept	DC shunt active filter for low-frequency harmonics		[53]
	F2	Topology (1A)	Three port concept for power decoupling		[55]
	F3	Application	Full-bridge buffer for active power filter application		[57]
	F4	Control	PQ control for full-bridge buffer circuit		[58]
	G1	Topology (1B)	Half-bridge buffer	High voltage stress and much energy storage	[60]
	G2	Control	Close-loop control consider component tolerance		[61]
	H1	Topology	Switched capacitors as energy buffer	Control complexity and many devices	[66]
	H2	Concept	General concept of switched capacitors as buffer	Control complexity and many devices	[68]
	I1	Topology (42F)	Series full-bridge for damping harmonics	E-cap used in buffer circuit	[71]
	I2	Control	Control the full-bridge as a controllable impedance		[73]
	I3	Application	Series full-bridge with inductor as buffer	Additional DC-link capacitor is needed	[75]
	I4	Control	Control for low-frequency ripple voltage and power loss compensation		[76]
	I5	Topology (42E)	Series buck converter as buffer	Much energy storage	[79]
	I6	Control	Voltage control for two terminal buffer		[83]
	J1	Topology (38F)	Series full-bridge with the converter for voltage compensation	Make one side voltage constant	[85]
	J2	Application	Modeling the series module for PV application		[87]
	J3	Application	Control and implementation of series module for LED application		[88]
	J4	Topology (38G)	Half bridge series module and its scalable multiparallel	Make one side voltage constant	[89]
	J5	Application	Series and parallel connection in buffer circuit		[90]
	K1	Topology (50C)	Series buck converter at AC side	Change modulation strategy of main circuit	[91]
(Integrated auxiliary circuits) Reduce number of components in single-phase converter with power decoupling capability	L1	Topology (38A)	Six-swiches converter with power decoupling capability	Low modulation index	[105]
	M1	Topology (34A)	Three legs with 2 AC capacitors topology, which reuse the LC filter as energy buffer	Low modultion index and much energy storage	[93]
	M2	Control	Reduce total energy storage of buffer		[94]
	N1	Topology (6A)	Three legs with 1 AC capacitor as buffer, which can increase energy buffer ratio	Many switches are used	[95]
	N2	Control	Modulation to reduce current stress		[97]
	N3	Control	Component sizing optimization		[99]
	O1	Topology (6C)	Full-bridge with one buffer capacitors	Low modulation index	[111]
	P1	Topology (7B)	Full-bridge with two buffer capacitors	Low modulation index and high current stress	[112]
	P2	Concept	General structure to integrate half-birdge into full-bridge		[114]
	Q1	Topology (35B)	Boost inverter with only 4 switches	Swinging DC-link voltage	[109]

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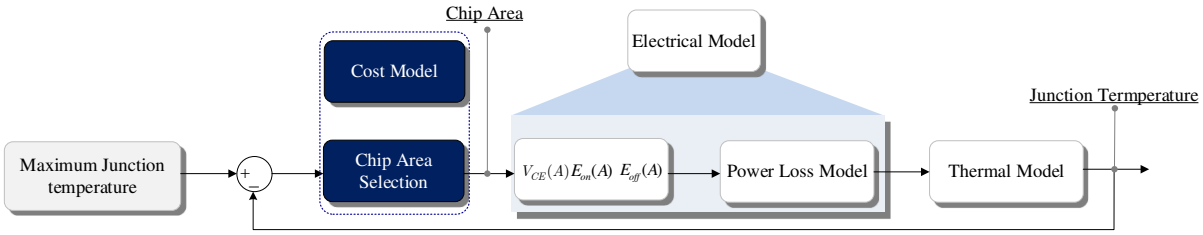

Fig. 10. Power Semiconductor reliability-oriented design procedure to fulfill the certain specification.

and film capacitors are used for the auxiliary capacitor $C_{\rm b}$. Such selections are based on the overall cost considerations as discussed later in cost assessment.

2) Capacitor Selection: Preliminary capacitor selection is done according to the electrical stress (voltage stress and current stress) and minimum required capacitance to limit the voltage ripple ratio derived from the electrical model. If the predicted capacitor lifetime is lower than the design target, another series of capacitors with longer rated lifetime or a capacitor in the same series with larger capacitance (i.e., smaller ESR) is chosen.

3) Electrical Stress Analysis: The electrical stress of each component is the basic for component selection. The voltage stress of DC-link electrolytic capacitor is constant, determined by the system specification. The DC-link voltage in this design is $V_{\rm dc}$ with voltage ripple ratio of $\alpha_{\rm v}$. In some existing topologies, because of DC-link voltage utilization of the system is lower, the DC-link voltage is set to be another specified value. Different from that, the buffer capacitor's voltage stress is related to the capacitance of buffer capacitor. Due to the total energy storage in the capacitor determines its cost and power density at certain voltage rating, in this paper, all the cases are designed for minimum total energy storage in capacitors. Then, the electrical stresses of the capacitors can be derived.

4) Thermal Stress Calculation: Thermal stress is one of the critical stressors for capacitors, resulting in the reduction of capacitance and the increase of ESR due to wear out. The current ripple and ambient temperature are the contributors to the internal thermal stress of the capacitor. Towards electrolytic capacitor, the dominant degradation mechanisms are electrochemical reaction in the oxide layer and the electrolyte vaporization [3]. Both factors lead to an increase in ESR over the operating life of a capacitor. Especially, the increase of capacitor power loss causes a higher operating temperature inside the capacitor. The hot-spot temperature of the capacitor, which is affected by the current stress and ambient temperature, is derived as

$$T_{\rm h} = T_{\rm a} + R_{\rm ha} \times \sum_{i=1}^{n} [ESR(f_{\rm i}) \times I_{\rm rms}^2(f_{\rm i})] \tag{4}$$

where $T_{\rm h}$ is the hot-spot temperature, $T_{\rm a}$ is the ambient temperature, $R_{\rm ha}$ is the equivalent thermal resistance from hot-spot to ambient, $ESR(f_{\rm i})$ is the equivalent series resistance at frequency $f_{\rm i}$, $I_{\rm rms}(f_{\rm i})$ is the RMS value of the ripple current at frequency $f_{\rm i}$. The hot-spot temperature $T_{\rm h}$ can then be estimated.

5) Lifetime Prediction: Lifetime prediction for the preliminarily selected capacitors can be done by the model which predicts the lifetime of capacitors under different operation conditions. According to the derivations in [3]

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times \exp[(\frac{E_{\rm a}}{K_{\rm B}})(\frac{1}{T} - \frac{1}{T_0})] \tag{5}$$

where L and L_0 are the lifetime under the use condition and testing condition, respectively. V and V_0 are the voltage at use condition and test condition, respectively. T and T_0 are the temperature in Kelvin at use condition and test condition, respectively. $E_{\rm a}$ is the activation energy, $K_{\rm B}$ is Boltzmann's constant $8.62 \times 10^{-5} eV/K$, and n is the voltage stress exponent. Therefore, the values of $E_{\rm a}$ and n are the key parameters to be determined in the above model. For electrolytic capacitor and film capacitors, a simplified model from the above equation is popularly applied as follows:

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times 2^{\frac{T_0 - T}{10}} \tag{6}$$

The model corresponds to a specific case of first equation when $E_{\rm a} = 0.94eV$ and T_0 and T are substituted by $398K$. For MPPF-Caps, the exponent n is from around 7 to 9.4, which is used by leading capacitor manufacturers. For electrolytic capacitors, the value of n typically varies from 3 to 5.

B. Power Semiconductors

The reliability-oriented procedure to size the chip area of active switches is shown in Fig. 10. The essence of selecting power semiconductor is sizing the chip area in each topology with the same loading conditions. By analyzing the power loss and thermal stress on each device, the optimal chip area can be selected for the maximum junction temperature, which is assumed to satisfy the lifetime requirement. The power semiconductor used in following analysis is IGBT. Similar sizing procedure can also be applied for MOSFET application.

1) Power Loss Calculation: The power losses in power semiconductor devices consist of the conduction loss and switching loss. If it is assumed that the current and voltage in a switching period is constant, the conduction loss in a switching period of each power device is

$$P_{\rm con_T} = v_{\rm CE}(|i_{\rm sw}|, T_{\rm j})|i_{\rm sw}| \tag{7}$$

$$P_{\rm con_D} = v_{\rm F}(|i_{\rm D}|, T_{\rm j})|i_{\rm D}| \tag{8}$$

where $P_{\rm con_T}$ is the conduction loss of the active device, and $P_{\rm con_D}$ is the conduction loss of the anti-parallel diode. $i_{\rm sw}$ and

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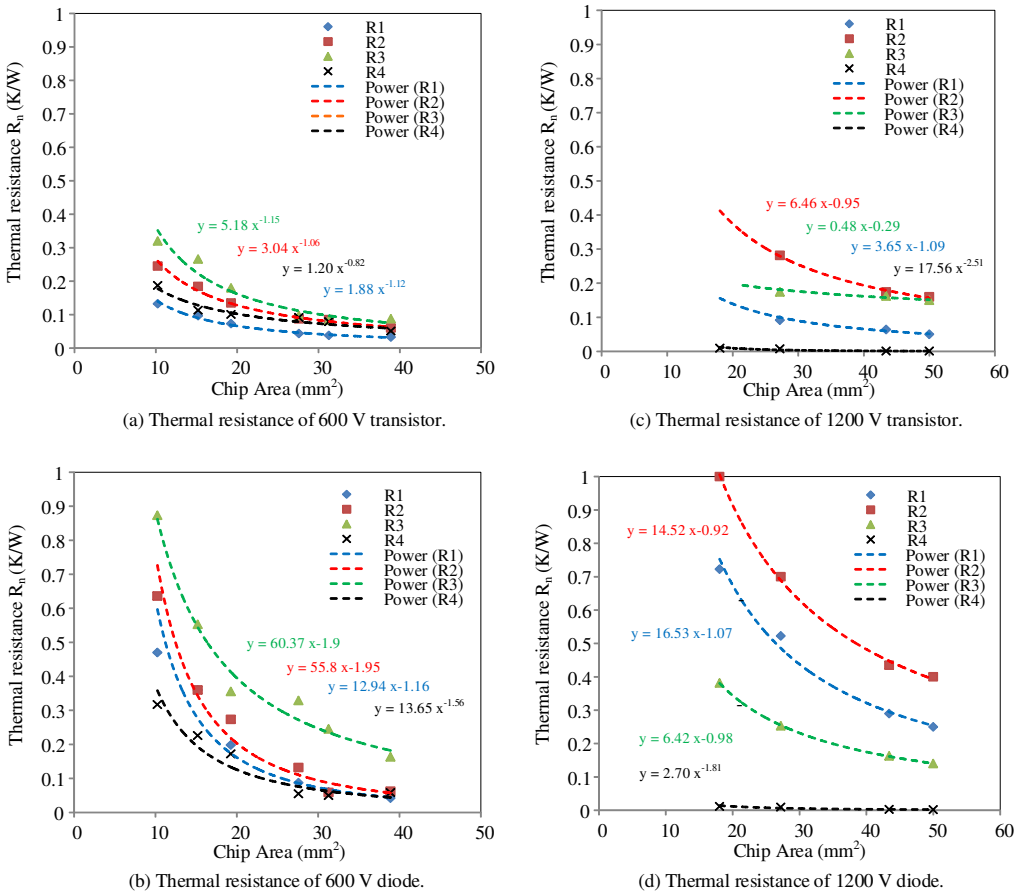

(a) Thermal resistance of 600 V transistor.

(c) Thermal resistance of 1200 V transistor.

(b) Thermal resistance of 600 V diode.

(d) Thermal resistance of 1200 V diode.

Fig. 11. Curve fitting results of thermal impedance parameters to the selected power devices.

$i_{\rm D}$ are the current flowing through the device and the diode, and $T_{\rm j}$ is the junction temperature of the devices. The $v_{\rm CE}$ and $v_{\rm F}$ are related to $i_{\rm sw}/i_{\rm D}$ and $T_{\rm j}$ which will be further discussed later. On the other hand, the switching loss in each power device can be calculated as

$$P_{\rm sw_T} = f_{\rm sw}[E_{\rm on}(|i_{\rm sw}|, T_{\rm j}, V_{\rm dc}) + E_{\rm off}(|i_{\rm sw}|, T_{\rm j}, V_{\rm dc})] \quad (9)$$

$$P_{\rm sw_D} = f_{\rm sw} E_{\rm rr}(|i_{\rm D}|, T_{\rm j}, V_{\rm dc}) \quad (10)$$

Similar as the equation above, $P_{\rm sw_T}$ is the switching loss for the switch, and $P_{\rm sw_D}$ is the switching loss for the freewheeling diode. $E_{\rm on}$ and $E_{\rm off}$ are the turn on and turn off energy dissipated by the device, while the $E_{\rm rr}$ is the reverse recovery energy loss dissipated by the diode, which are the functions of $i_{\rm sw}/i_{\rm D}$, $T_{\rm j}$ and $V_{\rm dc}$.

2) Thermal Stress Analysis: The power losses of active switches induces thermal stresses. The junction temperature of IGBTs can be modeled as

$$T_{\rm j}(t) = P_{\rm tot}(t) Z_{\rm th(j-c)}(t) + T_{\rm c}(t) \quad (11)$$

$$T_{\rm c}(t) = T_{\rm a} + [P_{\rm totS}(t) + P_{\rm totD}(t)] \times [Z_{\rm th(c-h)}(t) + Z_{\rm th(h-a)}(t)] \quad (12)$$

where $P_{\rm tot}$ gives the IGBT or diode power losses. $P_{\rm totS}$ and $P_{\rm totD}$ are the power losses in the IGBT and the diode respectively. $Z_{\rm th(j-c)}$, $Z_{\rm th(c-h)}$ and $Z_{\rm th(h-a)}$ give the thermal impedance from junction to case, case to heatsink and heatsink to ambient, respectively. $T_{\rm c}$ is the case temperature.

3) Sizing of the Chip Area: The power losses, thereby the thermal stresses and lifetime of the IGBTs are dependent on its chip areas. To achieve a specific lifetime target, a maximum allowable junction temperature is set in the design process, also as shown in Fig. 10. In order to size the chip area , the conduction loss model, the switching loss model, and the thermal model have to be adapted with the semiconductor chip area. The Infineon High Speed 3 (600 V and 1200 V) and Infineon IGBT Bare Die (600 V and 1200 V) have been chosen as the database because of the availability of sufficient information [122], [123]. For low voltage cases, Infineon HEXFET series (100 V and 150 V MOSFET) data are used for cost bechmarking. According to the associated data-sheets, the chip size is approximately proportional to the current rating. Moreover, the chip size determines the switch on and off energy $E_{\rm tot}$, $V_{\rm CE}$ and $Z_{\rm th}$ which have influence on the junction temperature of the devices. Based on the complete loss and thermal model including device rating information [124], the relationships can be approximately obtained by

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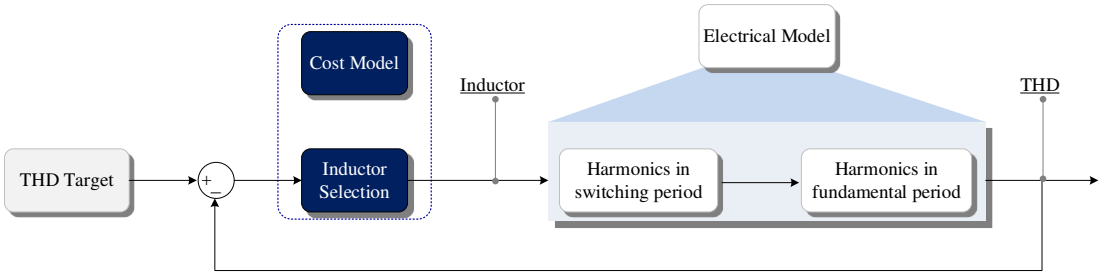
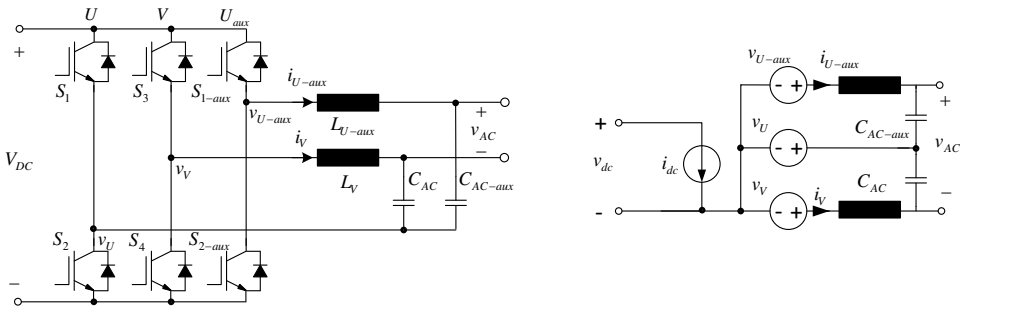


Fig. 12. Inductor design procedure to fulfill the certain specification.



(a) Topology used for inductor design.

(b) Average Model of the topolgoy used for inductor design.

Fig. 13. Three legs single-phase structure used for the inductor design and analysis.

TABLE VI
PARAMETERS RELATED TO CHIP AREA BY CURVE FITTING (SOURCE:INFINEON [122]).

Voltage Rating(V)	Parameters	a_0	a_1	a_2	a_3
600	V_{ce}	2.64	-1.32E-1	7.18E-3	3.14E-2
600	E_{tot}	9.89E-08	1.71E-10	2.06E-10	
1200	V_{ce}	2.61	-0.0648	6E-3	4.13E-2
1200	E_{tot}	1.14E-07	1.12E-09	8.10E-10	

TABLE VII
DIODE PARAMETERS RELATED TO CHIP AREA BY CURVE FITTING (SOURCE: INFINEON [122]).

Voltage Rating (V)	Parameters	a_0	a_1	a_2	a_3
600	V_F	1.7	-4.2E-2	3.1E-04	3.3E-2
600	E_{tot}	1.3E-05	2.76E-05	6.31E-06	
1200	V_F	2.5	-0.04	1.3E-3	7.1E-2
1200	E_{tot}	3.6E-04	2.9E-04	1.1E-05	

curve fitting of the equation given below.

$$\begin{cases} V_{\rm CE}(A_{\rm chip}, T_{\rm j}, i_{\rm sw}) = a_0 + a_1 A_{\rm chip} + a_2 T_{\rm j} + a_3 i_{\rm sw} \\ E_{\rm tot}(A_{\rm chip}, T_{\rm j}, i_{\rm sw}, V_{\rm dc}) = V_{\rm dc} \times i_{\rm sw} \times (a_0 + a_1 A_{\rm chip} + a_2 T_{\rm j}) \end{cases} \tag{13}$$

The constants a_0, a_1, a_2, and a_3 of the specifically analyzed IGBTs are listed in Table VI. The confidence level is 95% and R^2 (R^2 is computed from the sum of the squares of the distances of the points from the best-fit curve determined by nonlinear regression) are higher than 0.9. Similar analytical models for diodes can be obtained by curve fitting according to the equations below

$$\begin{cases} V_{\rm F}(A_{\rm chip}, T_{\rm j}, i_{\rm sw}) = a_0 + a_1 A_{\rm chip} + a_2 T_{\rm j} + a_3 i_{\rm sw} \\ E_{\rm tot}(A_{\rm chip}, T_{\rm j}, i_{\rm sw}, V_{\rm dc}) = V_{\rm dc} \times i_{\rm sw} \times (a_0 + a_1 A_{\rm chip} + a_2 T_{\rm j}) \end{cases} \tag{14}$$

The constants for the above equations are listed in Table VII. The thermal impedance of the power semiconductor can also be seen as a function of chip area, which is shown below

$$\begin{aligned} Z_{\rm th}(A_{\rm chip}) &= \sum_{n=1}^{4} R_{\rm n}(A_{\rm chip})(1 - e^{-\frac{t}{\tau_{\rm n}}}) \\ &= \sum_{n=1}^{4} a_{\rm n_0} A_{\rm chip}^{a_{\rm n_1}} (1 - e^{-\frac{t}{\tau_{\rm n}}}) \end{aligned} \tag{15}$$

where $R_{\rm n}$ is the thermal resistance for n layer RC lump of IGBT and $\tau_{\rm n}$ is the time constants. The curve fitting results for thermal resistances $R_{\rm n}(A_{\rm chip})$ is presented in Fig. 11.

C. Inductor

Since it is assumed that the magnetic components usually has less degradation compared to active switches and capacitors, the lifetime analysis of magnetic components is not considered in this paper. Because the modulation strategies of the single-phase systems presented above have changed, the sizing of the inductor is based on achieving the same THD of the inductor currents. The inductor design diagram can be seen in Fig. 12. An example including 3 legs is presented in Fig. 13 to illustrate the inductance design process, which can be extended to other 2 and 3 legs single-phase topologies with integrated active DC link. $U_{\rm aux}$ and V leg are connected to AC port of single-phase converter and U leg is used for power decoupling, which seems as float ground of the capacitors.

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TABLE VIII
SPECIFICATION OF THE SINGLE-PHASE SYSTEM AS A STUDY CASE.

Parameters	Description	Value
$P(W)$	Power rating	2200
$V_{\mathrm{dc}}(V)$	DC-link voltage	400 (800)
$V_{\mathrm{m}}(V)$	Peak voltage of AC	$220\sqrt{2}$
$I_{\mathrm{m}}(\mathrm{A})$	Peak Current of AC	$10\sqrt{2}$
α_{v}	DC-link voltage ripple ratio	4 %
α_{i}	Inductor current ripple ratio	20 %
$f_{\mathrm{a}}(Hz)$	Fundamental frequency	50
$f_{\mathrm{sw}}(Hz)$	Switching frequency	20 k
$T_{\mathrm{jmax}}(^{\circ}\mathrm{C})$	Maximum Junction Temperature	100
$T_{\mathrm{a}}(^{\circ}\mathrm{C})$	Ambient temperature	50
L(years)	Lifetime target of capacitors	10

This structure is able to be transformed to several single-phase topologies with integrated active DC link from above topology derivation, such as full-bridge by deleting U leg, interleave buck converter by connecting float ground to negative terminal of DC source, topology 6A with only one buffer capacitor C_{AC} and 34A, while the inductor design procedure for these cases is similar.

Based on the mathematical analysis, the RMS value of total harmonics over one period of the fundamental output voltage T can be obtained, which is limited to $\alpha_{\mathrm{i}} I_{\mathrm{AC,rms}}$. $I_{\mathrm{AC,rms}}$ is the RMS value of the AC port current and α_{i} is the current ripple ratio presented in Table VIII.

$$\tilde{I}_{\mathrm{U-aux,rms}} = \sqrt{\frac{1}{T}\left(\int_{t_{\mathrm{c}}}^{t_{\mathrm{c}}+\frac{T}{2}} \tilde{I}^2_{\mathrm{U-aux,p}}(t)dt + \int_{t_{\mathrm{c}}+\frac{T}{2}}^{t_{\mathrm{c}}+T} \tilde{I}^2_{\mathrm{U-aux,n}}(t)dt\right)} \tag{16}$$

where t_{c} is the crossover time of the AC current, $\tilde{I}^2_{\mathrm{U-aux,p}}(t)$ and $\tilde{I}^2_{\mathrm{U-aux,n}}(t)$ is the RMS current of leg U in a switching period. Detail analysis for parameter derivation is shown in Appendix A. Following above design procedure, the inductors for other leg can be derived and calculated by numerical computation, which can also be extended to all the cases. The analysis results for all the cases following above method have been listed in Table B.2. The inductor implementations are based on the Design software from Magnetics-2014 version [125]. The winding factor for each inductor is set to be similar for all the cases, between 35% and 40%, to keep same winding utilization.

V. COST ASSESSMENT AND SCALABILITY ANALYSIS OF ACTIVE DC LINKS

In this section, a reliability-oriented design method for cost-benchmarking is proposed, which can sizing the components with the specified lifetime target. The cost assessment and scalability analysis in terms of lifetime and power rating are studied to compare the typical capacitive DC-link solutions.

A. Cost Assessment

The cost assessment of the existing capacitive DC links is based on the same specification as shown in Table VIII. All of them have the same design target, which is the minimum energy storage in capacitors, with the same system specification and lifetime requirement.

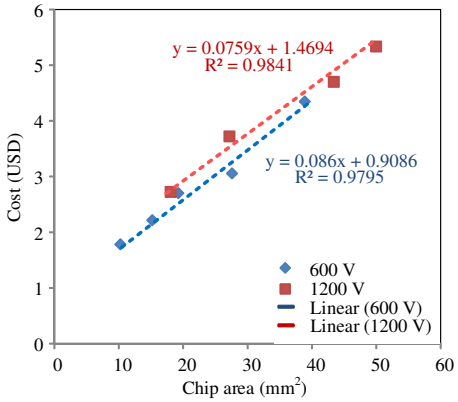

Fig. 14. Statistical results of power semiconductor cost which is represented as unit price for 1000 pieces ordering quantity (source: [122], [123]).

1) Power Semiconductor: The cost of the IGBT switches is modeled as the chip cost and package cost as discussed in details in [126]. The chip cost is proportional to its area and the packaging cost is a fixed one for a given packaging form. Therefore,

$$\sum\nolimits_{\mathrm{cd}} = \sum\nolimits_{\mathrm{chip}} + \sum\nolimits_{\mathrm{pack,x}} = \left(\sum_{\mathrm{n}} \sigma_{\mathrm{chip,x(n)}} A_{\mathrm{chip,n}}\right) + \sum_{\mathrm{pack,x}} \tag{17}$$

where $\sigma_{\mathrm{chip,x(n)}}$ is the specific cost per chip area, $A_{\mathrm{chip,n}}$ depending on the chip technology, and $\sum_{\mathrm{pack,x}}$ is the package cost (including chip integration and bonding). The parameter $\sigma_{\mathrm{chip,x(n)}}$ can hence be interpreted as the sum of all processing and $R\,\&\,D$ costs for a given chip technology. The statistical results are presented in Fig. 14.

2) Capacitor: The cost of E-caps and film capacitors of certain voltage rating scales with the rated stored energy. Therefore, the cost model can be written as

$$\sum\nolimits_{\mathrm{cap}} = \sum\nolimits_{\mathrm{Energy}} + \sum\nolimits_{\mathrm{pack}} = \sum\nolimits_{\mathrm{unit}} E_{\mathrm{cap}} + \sum\nolimits_{\mathrm{pack}} \tag{18}$$

where $\sum_{\mathrm{Energy}}$ is the cost for energy stored in the capacitor which can be described as the multiple of the cost for unit energy $\sum_{\mathrm{unit}}$ and the energy requirement for circuit E_{cap}. Fig. 15 (a) and (b) show the statistical results of unit cost of standard E-cap (450V rated voltage, snap-in terminals, and 20% tolerance) and polypropylene thin film capacitors from leading manufacturers.

The design results and costs for the capacitors of existing solutions are in given Table B.1 (Data supported by Digikey [123]). It is worth to note that the lifetime of DC-link capacitor in 1C with 110 μF is 9 years which are shorter than the lifetime target. By increasing the capacitance (i.e., with lower ESR value) in the same series of products, the lifetime extends to be 11 years at 150 μF.

3) Inductor: Based on the inductor cost model presented in [126], high flux ferrite core and solid round winding are selected in the three design cases. Inductors for converters in the considered power range are often material and labour intense, of which a simplified version can also be found in

$$\sum\nolimits_{\mathrm{L}} = \sum\nolimits_{\mathrm{mat,L}} + \sum\nolimits_{\mathrm{lab,L}} \tag{19}$$

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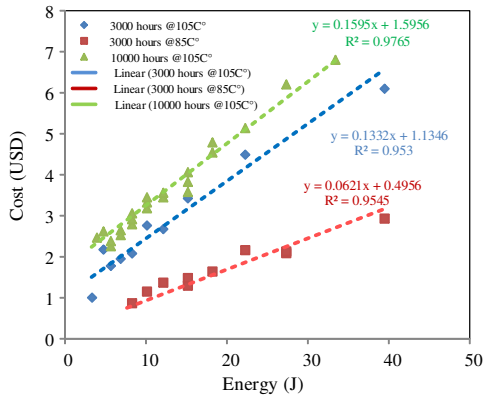
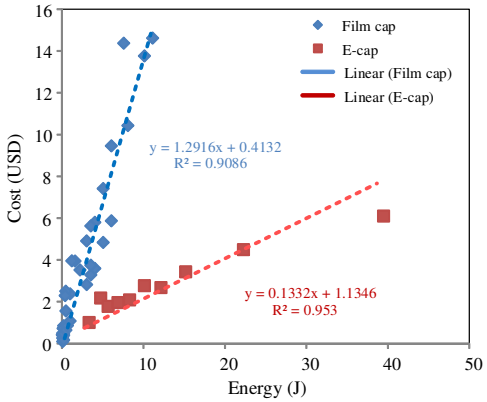


(a) Cost models of different types of E-caps.



(b) Cost models of 3000 hours @105° E-cap and film capacitors.

Fig. 15. Statistical results of unit cost of different kinds of capacitors which are represented as unit price for 1000 pieces ordering quantity (source: [123]).

where

$$\sum\nolimits_{\mathrm{max,L}} = \sum\nolimits_{\mathrm{core,x}} + \sum\nolimits_{\mathrm{wdg,x}} + \sum\nolimits_{\mathrm{mat,x}}^{\mathrm{fac}} = \sigma_{\mathrm{core,x}} W_{\mathrm{core}} + \sigma_{\mathrm{wdg,x}} W_{\mathrm{wdg}} + \sum\nolimits_{\mathrm{mat,x}}^{\mathrm{fac}} \tag{20}$$

$$\sum\nolimits_{\mathrm{lab,L}} = \sigma_{\mathrm{lab,x}} W_{\mathrm{wdg}} + \sum\nolimits_{\mathrm{lab,x}}^{\mathrm{fac}} \tag{21}$$

$\sigma_{\mathrm{core,x}}$, $\sigma_{\mathrm{wdg,x}}$ and $\sigma_{\mathrm{lab,x}}$ are specific costs per weight W_{core}, W_{wdg} of the core and winding depending on the employed core and winding type. $\sum_{\mathrm{mat,x}}^{\mathrm{fac}}$ and $\sum_{\mathrm{lab,x}}^{\mathrm{fac}}$ are fixed material and labour costs (e.g. coil former, connectors). The design results of inductors' costs for the existing active power decoupling solutions are in Table B.2.

4) Total: The total cost of the single-phase topologies with active DC link integrated are calculated, which have been presented in Fig. 16 (Detail information are shown in Appendix B). It can be seen that the cost of capacitors plays the greatest impact on the total cost in all the cases. The passive solution cost lower than the others for 10 years lifetime requirement, which is the reason for most industry applications still using passive way to buffer the pulsating power. 1A, 1B, 1C, 1D and 1E are separate auxiliary circuits parallelled at the DC link which is practical for replacing the E-cap. Because of decoupling the fluctuating power by the AC component of capacitor voltage, the current stress of the buffer capacitor, filter inductor and power semiconductors in 1B are larger than other solutions, which will result in more cost. 6A costs lower than interleave boost, interleave buck, 6C, 7B and 34A, due to the high voltage and energy utilization ratio. Moreover, because of low DC-link voltage utilization, interleave buck, 6C, 7B and 34A work with 800 V DC-link voltage in this design case, which is higher than 400 V DC-link. Among all the single-phase topologies with integrated auxiliary circuits, 42F solution costs the lowest, because the electrical stress of all the components in auxiliary circuit is low. In this study, the cost for sensor, controller, PCB and wire are not included.

B. Scalability Analysis

For different mission profile, the sizing results are different, which further impact on the whole life cycle cost of the system. This section presents the cost assessment results with scalable lifetime target and power rating to benchmark these capacitive DC-link solutions.

1) Lifetime Target: The cost assessment results for 10 year lifetime target have been shown in Fig. 16. Following the same design process, the cost assessment results with a more strictly lifetime target of 20 and 35 years are shown in Fig. 17 and Fig. 18, respectively.

With 20 years lifetime target, the cost of passive solution increase 58 % compared with 10 years lifetime target. The reason for the cost increase is the capacitor used in this series can not work for 25 years. It need to be replaced one time during the whole life cycle, therefore increasing the whole life cycle cost of the system. It can be seen that the topology with active DC-link solution 1A, 1D, 6A, 38F, and 42F cost lower than the passive solution in this condition. Especially, topology 42F costs lowest among all the solutions, because of lower apparent power handled by the auxiliary circuit in 42F.

With 35 years lifetime target, the cost of the passive solution increases 133 % with 10 years lifetime target. Except for the 1B, 34A, and 7B, all the active capacitive DC links cost lower than the passive solution. 42F costs 48 % of passive solution, which is the most cost-effectiveness one among all the solutions.

To study the relation between the lifetime target and the cost, four cases are investigated for comparisons. Case I is the passive solution, which is implemented by E-caps at the DC link to buffer the pulsating power. Case II is the active solutions which is the separate auxiliary energy buffer 1A connected in parallel with the DC link. Case III is the single-phase topology with integrated auxiliary circuit 6A, which can be derived from full-bridge converter integrated with half-bridge active DC link. Case IV is the 42F which is the most cost-effectiveness solution from above benchmarking.

Fig. 19 shows that the cost of passive solution and 42F topology within the lifetime range is increasing almost linearly, while the cost of 1A and 6A solutions are constant because there is no E-cap in the two solutions. Therefore, if the power devices and film capacitors are assumed sufficient reliable within this lifetime target, no additional cost will be introduced.

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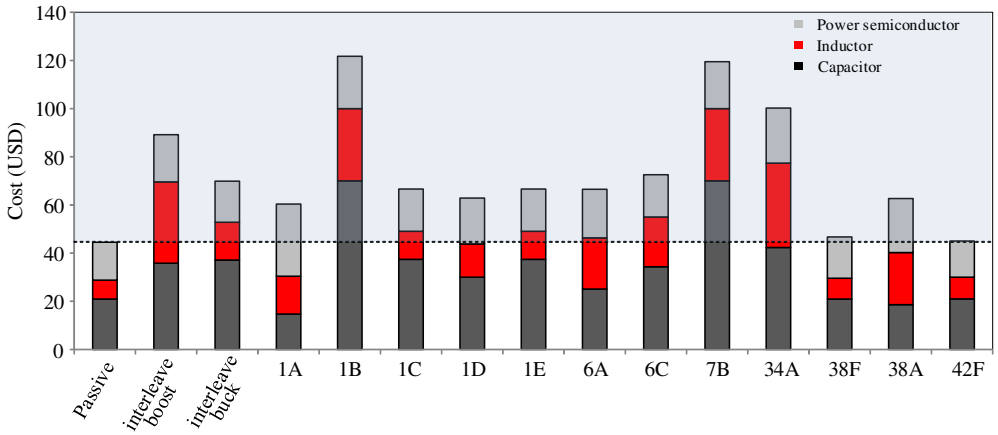

Fig. 16. Total cost of capacitors, inductors and power devices of the existing methods with 10 years lifetime target.

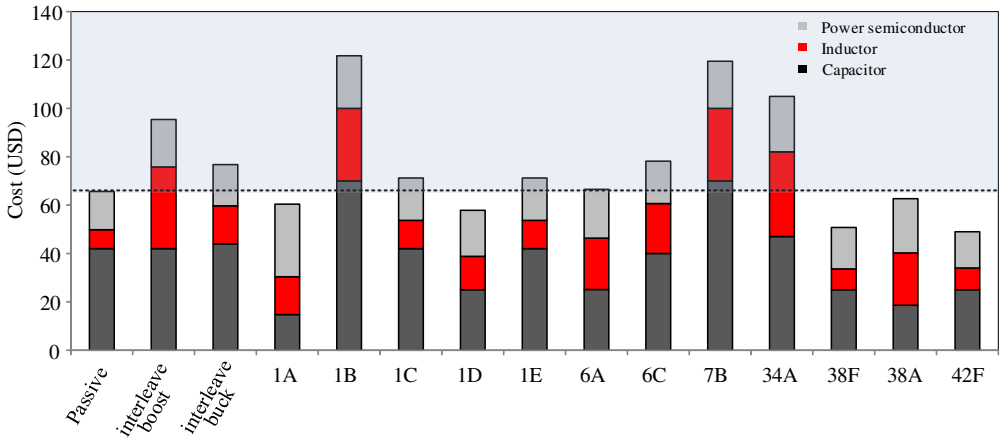

Fig. 17. Total cost of capacitors, inductors and power devices of the existing methods with 20 years lifetime target.

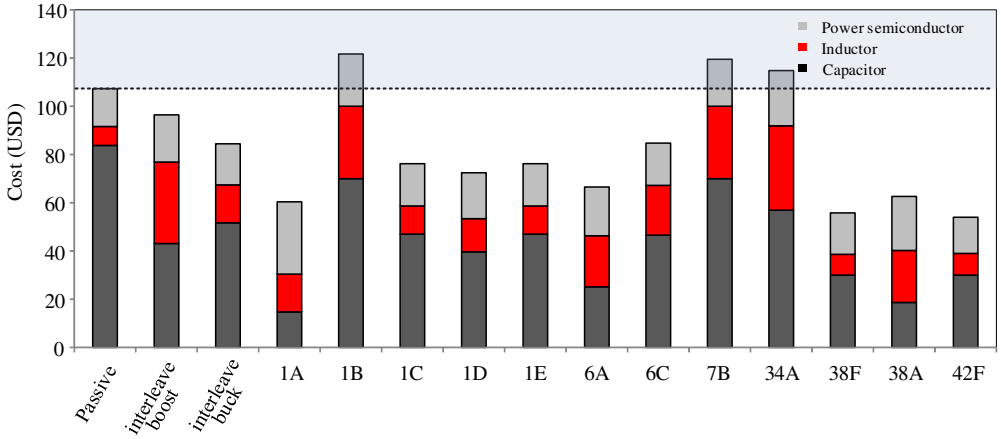

Fig. 18. Total cost of capacitors, inductors and power devices of the existing methods with 35 years lifetime target.

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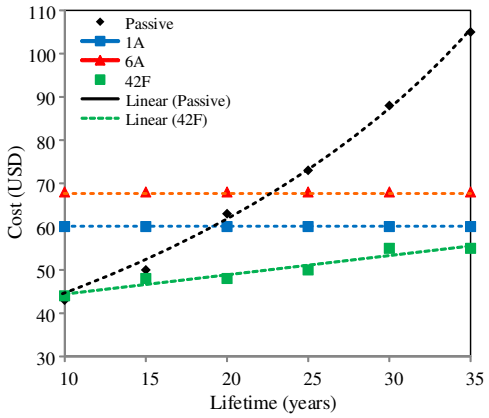


Fig. 19. Relation between the lifetime target and cost of 4 cases.

2) Power Rating: This section studies the relation between the scalable power rating and the cost of the system with active DC link. Following the component sizing procedure for cost-benchmarking, the cost assessment of the above four cases with range of power rating are shown in Fig. 20. It can be seen that, with 10 years lifetime target, the passive solution costs lower than the other three active capacitive DC-link solutions in all the power rating. This is the reason for the products whose lifetime requirement is lower than 10 year still use passive solution. It also can be seen that the cost of the four cases increase almost linearly with scalable power rating.

For 20 and 35 years lifetime targets, the cost assessment results of the four cases are different at scalable power rating. From Fig. 21, it can be seen that, the life-cycle cost of active solutions are higher than the passive DC-link solutions at the low power rating, while the cost are lower at higher power rating and more stringent reliability requirement applications.

VI. Energy Storage Assessment and Analysis

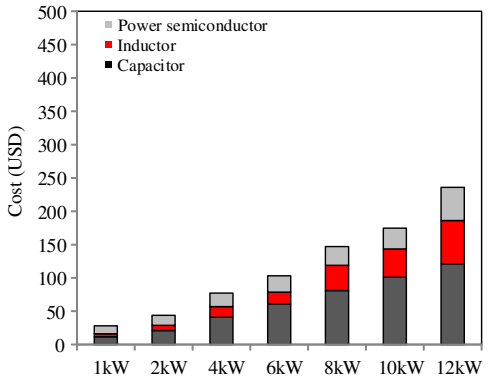
Energy storage of active DC link is a key factor to determine the cost of the capacitor, and indirect reflects the electrical stress of the DC link. In this section, the energy storage and energy buffer ratio are considered as the criteria to benchmark the active DC-link solutions.

A. Capacitor Energy Storage

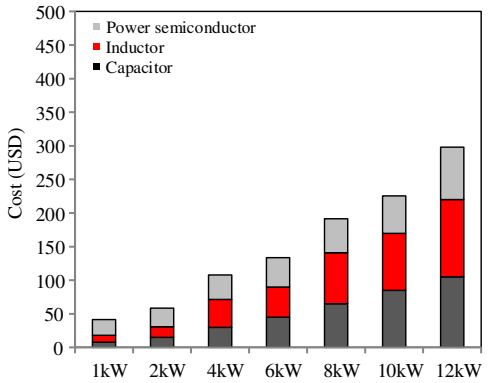
As design target and one of the assessment factors, total energy storage is the sum of the energy storage in all the capacitors, which determines the cost of capacitors in a system as presented below

$$E_{\mathrm{c-tot}} = \frac{1}{2} C_{\mathrm{dc}} V_{\mathrm{dc-max}}^2 + \frac{1}{2} C_{\mathrm{b}} V_{\mathrm{c-max}}^2 \qquad (22)$$

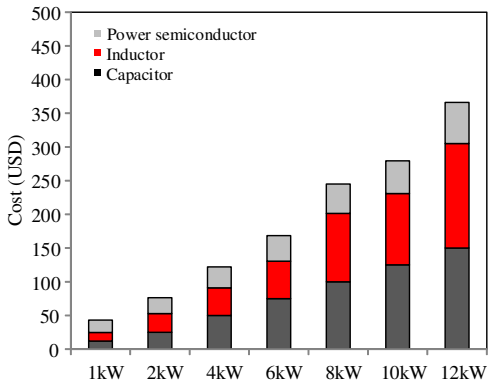
where $E_{\mathrm{c-tot}}$ is the total energy storage in capacitors, C_{dc} and C_{b} is the capacitance of the DC-link capacitor and buffer capacitor, and $V_{\mathrm{dc-max}}$ and $V_{\mathrm{c-max}}$ are the maximum DC-link voltage and buffer capacitor voltage, respectively.



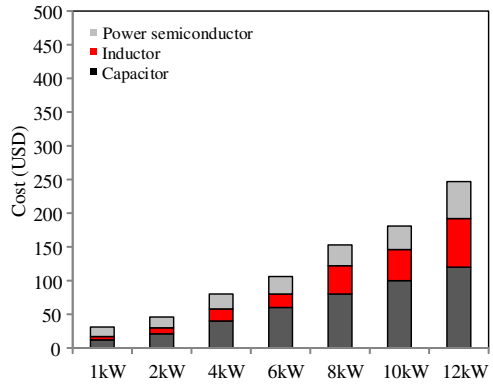
(a) Cost of passive solution with scalable power rating.



(b) Cost of 1A solution with scalable power rating.



(c) Cost of 6A solution with scalable power rating.



(d) Cost of 42F solution with scalable power rating.

Fig. 20. Cost evaluate results of the four cases with 10 years lifetime target and scalable power rating.

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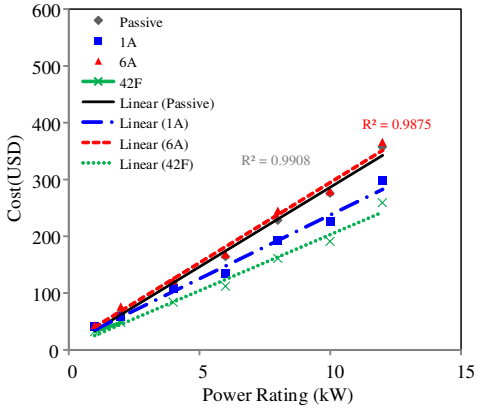
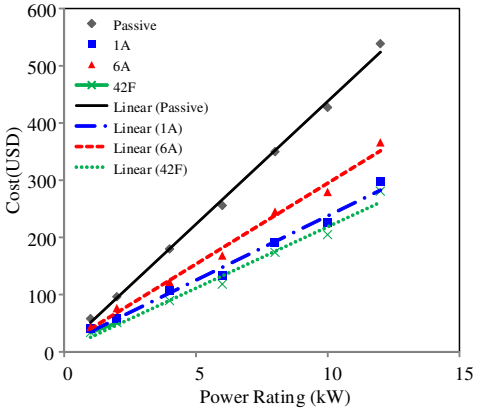
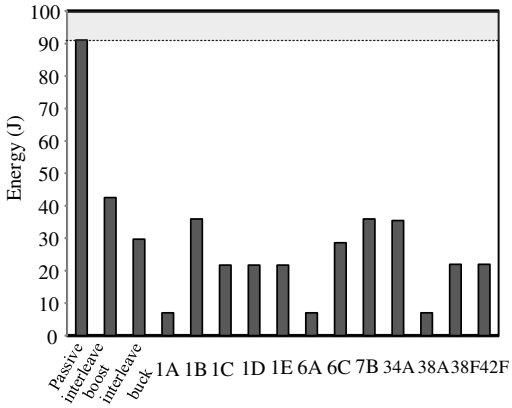


(a) With 20 years lifetime target.

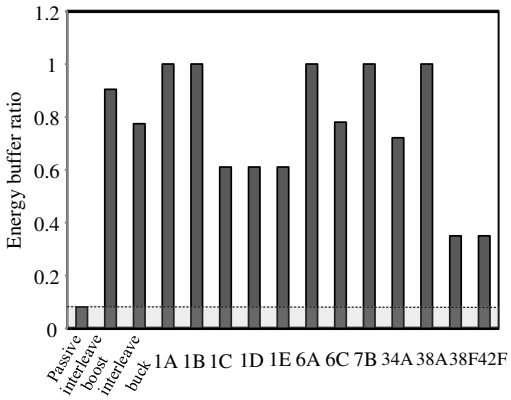


(b) With 35 years lifetime target.

Fig. 21. Cost evaluate results of four cases with 20 and 35 years lifetime target and scalable power rating.



(a) Total energy stored in capacitors of key solutions.



(b) Energy buffer ratio of key solutions.

Fig. 22. Total energy stored in capacitors and energy buffer ratio comparisons among typical active DC-link solutions.

B. Energy Buffer Ratio

It is defined to be the ratio of the fluctuating energy to the maximum energy in the capacitor. The total fluctuating energy in both DC-link capacitor and buffer capacitors is

$$E_{\mathrm{f-tot}} = (\frac{1}{2}C_{\mathrm{dc}}V_{\mathrm{dc-max}}^2 - \frac{1}{2}C_{\mathrm{dc}}V_{\mathrm{dc-min}}^2) + (\frac{1}{2}C_{\mathrm{b}}V_{\mathrm{c-max}}^2 - \frac{1}{2}C_{\mathrm{b}}V_{\mathrm{c-min}}^2) \tag{23}$$

where $V_{\mathrm{dc-min}}$ and $V_{\mathrm{c-min}}$ are the minimum voltage of the DC link and buffer capacitor respectively. Thus, the energy buffer ratio is the division of total fluctuating energy and total energy storage in capacitors

$$\Gamma = \frac{E_{\mathrm{f-tot}}}{E_{\mathrm{c-tot}}} \tag{24}$$

C. Cases Study

Cases analysis for these single-phase topologies with active DC links are presented in Fig. 22, in terms of total energy storage in capacitor and energy buffer ratio.

From Fig. 22 (a), it can be seen the passive solution stores the maximum energy in capacitor with the lowest energy buffer ratio among all the assessment solutions. It indicates a lot of energy is not benefit of power decoupling. 1A, 6A and 38A solutions store minimum energy in capacitors and all of it is utilized for energy buffer. The similarity of these solutions is that both of them are synthesised from full-bridge inverter as the main circuit and full-bridge bidirectional converter as the auxiliary circuit, where there is only AC component in the buffer energy storage component. In Fig. 22 (b), the energy buffer ratios of 1B and 7B solutions is 1, while they store much energy in capacitor, which means the auxiliary circuit can eliminate the DC-link E-cap and support longer hold up time compared with other cases. The buffer capacitor implementation of these two solutions are both two capacitors in series, and then in parallel at the DC link, whose voltage contains DC and fundamental frequency AC components to support the DC-link voltage and decouple the pulsating power.

VII. Discussions

The component sizing procedure presented in Section IV allows a cost comparison of different capacitive DC-link solutions to fulfill same system-level specifications, which can be applied for different case studies. Nevertheless, the numeric results shown in Section V and Section VI are corresponding to the specifications given in Table VIII only. The DC-link sizing criteria in the case study is based on the DC-link voltage ripple ratio of 4 % in the steady-state operation under rated loading condition. If the DC-link voltage ripple limit is changed, the comparative results could be different as well.

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Moreover, it is noted that the majority studies on active capacitive DC links are based on the steady-state DC-link voltage ripple specification, which are relevant to applications where the required DC-link is determined by its ripple voltage criteria. Nevertheless, in many other applications, the sizing of capacitative DC links are determined by its ripple current capability or energy storage requirement [86]. It is still lack of study in literature to evaluate the feasibility of active capacitive solutions from the perspectives of ripple current capability and energy storage requirements. Therefore, the comparative results in Section V and Section VI should be treated with caution. Future research efforts are needed to applications which ripple current or energy storage requirement is the decisive factor for capacitor sizing.

VIII. Conclusion

An overview of capacitive DC-link solutions in single-phase power electronic system is presented in this paper. 1) A generic topology derivation for single-phase power converters with integrated auxiliary circuit is proposed in this paper. 2) The main achievements in research on capacitive DC-link solutions are reviewed and presented chronologically and thematically, in order to understand the development trend of capacitive DC-link solutions. 3) For the cost assessment of capacitive DC-link solutions, a component sizing procedure based on a consistent converter level specification is proposed by considering the reliability as a performance factor that influences on the sizing of power semiconductors and capacitors and sizing the inductors according to the THD limitations. The topology derivation method and the scalability study through the case study in terms of power level and lifetime specifications provide new perspectives than existing overview literature on the presented topic.

The review also identifies a key limitation in the existing studies, which the ripple current and energy storage requirements are rarely considered when active capacitor solutions are demonstrated, even though they are relevant for many practical applications. Future research to address the limitation is suggested. Moreover, the component sizing criteria presented in this paper can be extended to other capacitor sizing criteria, and also to three-phase applications with unbalanced loads or grids. An additional research effort is suggested to experimentally reliability validation of different proposed active capacitive DC links.

Appendix A
Inductor Design

Based on the circuit of Fig. 13, the voltage equation of the loop between $U_{\rm aux}$ leg and U leg can be written as

$$v_{\rm s} = L_{\rm U-aux}\frac{di_{\rm U-aux}}{dt} + v_{\rm c_{AC-aux}} \tag{A.1}$$

where $v_{\rm s}$ is the voltage between middle voltage of $U_{\rm aux}$ and U legs

$$v_{\rm s} = v_{\rm U-aux} - v_{\rm U} \tag{A.2}$$

The capacitor voltage $v_{\rm C_{AC-aux}}$ and inductor current $i_{\rm U-aux}$ can be separated into the average (average over one switching cycle) and the harmonic (ripple) components, that is,

$$v_{\rm c_{AC-aux}} = \bar{v}_{\rm c_{AC-aux}} + \tilde{v}_{\rm c_{AC-aux}} \tag{A.3}$$

$$i_{\rm U-aux} = \bar{i}_{\rm U-aux} + \tilde{i}_{\rm U-aux} \tag{A.4}$$

Upon substituting (A.3) and (A.4) into (A.5), the following equation is obtained

$$v_{\rm s} = L_{\rm U-aux}\frac{d(\bar{i}_{\rm U-aux} + \tilde{i}_{\rm U-aux})}{dt} + \bar{v}_{\rm c_{AC-aux}} + \tilde{v}_{\rm c_{AC-aux}} \tag{A.5}$$

In a well designed filter, the values of $\tilde{v}_{\rm c_{AC-aux}}$ are small compared to $L_{\rm U-aux}\frac{d\tilde{i}_{\rm U-aux}}{dt}$ and, therefore, the ripple component of the filter inductor current can be calculated as

$$\tilde{i}_{\rm U-aux} = \frac{1}{L_{\rm U-aux}}\int(v_{\rm s} - \bar{v}_{\rm s})dt \tag{A.6}$$

where

$$\bar{v}_{\rm s} = \bar{v}_{\rm c_{AC-aux}} + L_{\rm U-aux}\frac{d\bar{i}_{\rm U-aux}}{dt} \tag{A.7}$$

is the average value of the output voltage of the inverter. Although there are various PWM techniques that can be used to control the inverter, the sampling based PWM techniques are the most commonly used because the implementation is simpler. The most popular implementation of the sampling based PWM techniques is based on the comparison between a sinusoidal reference and a high frequency triangular carrier signals, which is also referred to natural sampling.

The modulation waveforms are plotted in Fig. A.1, where the blue and the gray curves are for $v_{\rm U_{aux}}$ and $v_{\rm U}$ separately and the red curve is for $v_{\rm C_{AC-aux}}$, which is the difference of $v_{\rm U_{aux}}$ and $v_{\rm U}$. There are two types of switching sequences in one fundamental frequency as shown in Fig. A.1.

Below the crossover time $t_{\rm c}$, $v_{\rm U-aux}$ is larger than $v_{\rm U}$ which means the $v_{\rm s}$ is positive, vice versa. Because switching sequence determines the switching patterns in a switching period, the RMS value of harmonic current in one fundamental period should be calculated individually for the two switching sequences. The positive and negative switching sequences are shown in Fig. A.2 (a) and (b), respectively. D and $D_{\rm aux}$ are the duty cycles of S_1 and $S_{1-\rm aux}$. The mean square values of this current harmonic over one switching period of positive and negative period can be calculated as

$$\tilde{I}^2_{\rm U-aux,p} = \frac{1}{T_{\rm s}}\int_{t_0}^{t_0+T_{\rm s}}\tilde{i}^2_{\rm U-aux,p}dt \tag{A.8}$$

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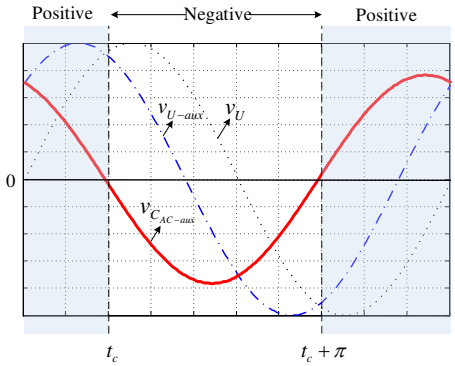

Fig. A.1. Modulation waveforms for each two legs in one fundamental frequency.

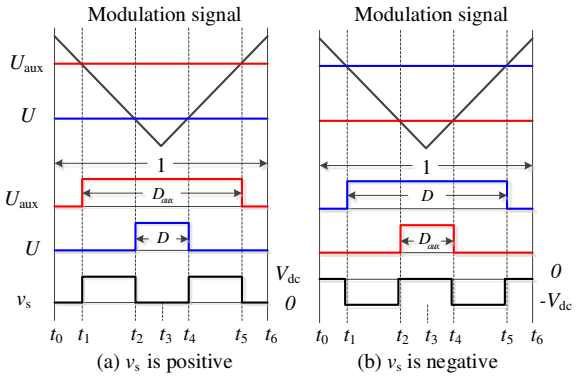

Fig. A.2. Switching sequences of each two legs in one switching period.

$$\tilde{I}^2_{\mathrm{U-aux,n}} = \frac{1}{T_\mathrm{s}} \int_{t_0}^{t_0+T_\mathrm{s}} \tilde{i}^2_{\mathrm{U-aux,n}} dt \tag{A.9}$$

where T_s is the switching period.

At the steady state, the capacitor voltage can be written as follows

$$v_{\mathrm{AC-aux}} = \frac{1}{2} V_\mathrm{m} \sin(\omega t) + B \sin(\omega t + \varphi) \tag{A.10}$$

where B and φ are the amplitude and phase angle of power decoupling function [94]. V_m is the amplitude of AC voltage and V_dc is the average DC-link voltage. Therefore, the duty cycles for U_aux and U legs can be obtained as

$$\begin{cases} D_{\mathrm{U-aux}} = \frac{1}{2} + \frac{\frac{1}{2} V_\mathrm{m} \sin \omega t}{V_\mathrm{dc}} \\ D_\mathrm{U} = \frac{1}{2} - \frac{B \sin(\omega t + \varphi)}{V_\mathrm{dc}} \end{cases} \tag{A.11}$$

In the positive half period of v_s, the harmonic can be integrate from $i_{\mathrm{U-aux,p}}$, while in negative half period can be integrated from $i_{\mathrm{U-aux,n}}$. The crossover time t_c in Fig. A.1 can be found by setting $v_{\mathrm{AC-aux}}$ equal to 0. The crossover time t_c can be found as

$$t_\mathrm{c} = \frac{k\pi - \arctan \frac{B \sin \varphi}{V_\mathrm{m} + B \cos \varphi}}{\omega} (k = 0, 1, 2...) \tag{A.12}$$

APPENDIX B
COST ASSESSMENT RESULTS

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TABLE B.1
COST ANALYSIS RESULTS OF CAPACITORS IN SINGLE-PHASE TOPOLOGIES WITH INTEGRATED ACTIVE DC-LINK.

		Voltage level (V)		Capacitance (uF)		Configuration		Tot cost (USD)
		Implementation voltage	Theoretical voltage	Implementation capacitance	Theoretical capacitance	Components	Lifetime (year)	
Passive	Electrolytic	450	408	1800	1094	TDK, B43508A5687M0, 3000hr, 105°C	11	21
Interleave boost	Electrolytic Film	450 450*2	408 794	82 61*2	51 61*2	TDK, B43508A5826M0, 3000hr, 105°C	13	36
Interleave buck	Electrolytic Film	450 450*2	808 671	82 121*2	21 121*2	TDK, B43508A5826M0, 3000hr, 105°C	13	37
1A	Film	450	167	110	110			15
1B	Film	450	358	280*2	280*2			74
1C	Electrolytic Film	450 450	408 311	150 260	110 260	TDK, B43508A5157M0, 3000hr, 105°C	11	37
1D	Electrolytic Film	450 450*2	408 709	150 100	110 50	TDK, B43508A5157M0, 3000hr, 105°C	10	30
1E	Electrolytic Film	450 450	408 311	150 260	110 260	TDK, B43508A5157M0, 3000hr, 105°C	10	37
6A	Film	450	264	190	190			25
6C	Electrolytic Film	450*2 450	808 438	47 230	20 230	TDK, B43508A5826M0, 3000hr, 105°C	10	34
7B	Film	450	358	280*2	280*2			74
34A	Electrolytic Film	450*2 450	808 425	82 141	31 141	TDK, B43508A5826M0, 3000hr, 105°C	13	42
38A	Film	450	167	140	140			19
38F	Electrolytic Film	100 450	80 400	270 110	270 110	TDK, B41858C9277M, 3000hr, 105°C	12	21
42F	Electrolytic Film	100 450	80 400	270 110	270 110	TDK, B41858C9277M, 3000hr, 105°C	12	21

TABLE B.2
COST ANALYSIS RESULTS OF INDUCTORS IN SINGLE-PHASE TOPOLOGIES WITH INTEGRATED ACTIVE DC-LINK [125]

		Theoretical Inductance (mH)	Part number	Winding factor(%)	Turns	Wire size (AWG)	Core weight (g)	Winding weight (g)	Cost (USD)	Tot cost (USD)
Passive	U	1.16	MAGNETICS C058617A2	35	150	15	410	215	8	8
Interleave boost	U U_{aux}	1.25 1.25	MAGNETICS C058099A2 MAGNETICS C058099A2	36.2 36.2	280 280	13 13	440 440	633 633	17 17	34
Interleave buck	U U_{aux}	1.67 1.67	MAGNETICS C058617A2 MAGNETICS C058617A2	35 35	150 150	15 15	410 410	215 215	8 8	16
1A	U U_{aux}	1.16 1.04	MAGNETICS C058617A2 MAGNETICS C058867A2	35 35	150 150	15 15	410 410	215 215	8 8	16
1B	U U_{aux}	1.16 1.15	MAGNETICS C058617A2 MAGNETICS C058339A2	35 15.1	150 200	15 12	410 1200	215 766	8 25	33
1C	U U_{aux}	1.16 0.62	MAGNETICS C058617A2 MAGNETICS C058089A2	35 38.6	150 200	15 17	410 120	215 119	8 4	12
1D	U U_{aux}	1.16 0.99	MAGNETICS C058617A2 MAGNETICS C058110A2	35 38.8	150 250	15 16	410 160	215 207	8 6	14
1E	U U_{aux}	1.16 0.62	MAGNETICS C058617A2 MAGNETICS C058089A2	35 38.6	150 200	15 17	410 120	215 119	8 4	12
6A	U U_{aux}	1.16 1.22	MAGNETICS C058617A2 MAGNETICS C058907A2	35 38.1	150 300	15 14	410 340	215 499	8 13	21
6C	U U_{aux}	2.06 1.40	MAGNETICS C058099A2 MAGNETICS C058254A2	35.8 38.8	480 220	15 19	440 87	682 77	18 3	21
7B	U U_{aux}	2.27 2.29	MAGNETICS C058099A2 MAGNETICS C058099A2	35.8 35.8	480 480	15 15	440 440	682 682	18 18	36
34A	U U_{aux}	2.41 2.41	MAGNETICS C058737A2 MAGNETICS C058737A2	37.3 37.3	250 250	14 14	700 700	579 579	18 18	35
38A	U U_{aux}	2.14 1.40	MAGNETICS C058099A2 MAGNETICS C058438A2	35.8 38.6	480 140	15 17	440 170	682 96	18 4	22
38F	U U_{aux}	1.16 0.12	MAGNETICS C058617A2 MAGNETICS C058204A2	35 37.2	150 70	15 20	410 9.1	215 10	8 1	9
42F	U U_{aux}	1.16 0.12	MAGNETICS C058617A2 MAGNETICS C058204A2	35 37.2	150 70	15 20	410 9.1	215 10	8 1	9

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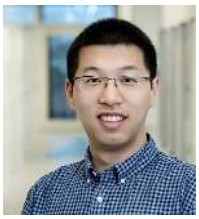

Haoran Wang (S'15-M'18) received the B.S. and M.S. degrees in control science and engineering from Wuhan University of Technology, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in power electronics from Center of Reliable Power Electronics (CORPE), Aalborg University, Aalborg, Denmark, in 2018, where he is currently a Postdoc Research Fellow.

From Jul. 2013 to Sep. 2014, he was research assistant with the Department of Electrical Engineering, Tsinghua University, Beijing, China. He was a Visiting Scientist with the ETH Zurich, Switzerland, from Dec. 2017 to Apr. 2018. His research interests include capacitors in power electronics, reliability of power electronic systems and multi-objective life-cycle performance optimization of power electronic systems.

Huai Wang (M'12-SM'17) received the B.E. degree in electrical engineering, from Huazhong University of Science and Technology, Wuhan, China, in 2007 and the Ph.D. degree in power electronics, from the City University of Hong Kong, Hong Kong, in 2012. He is currently an Associate Professor at the Center of Reliable Power Electronics (CORPE), Aalborg University, Aalborg, Denmark. He was a Visiting Scientist with the ETH Zurich, Switzerland, from Aug. to Sep. 2014, and with the Massachusetts Institute of Technology (MIT), USA, from Sep. to Nov. 2013. He was with the ABB Corporate Research Center, Switzerland, in 2009. His research addresses the fundamental challenges in modelling and validation of power electronic component failure mechanisms, and application issues in system-level predictability, condition monitoring, circuit architecture, and robustness design. Dr. Wang received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016, and the Green Talents Award from the German Federal Ministry of Education and Research in 2014. He is currently the Award Chair of the Technical Committee of the High Performance and Emerging Technologies, IEEE Power Electronics Society, and the Chair of IEEE PELS/IAS/IE Chapter in Denmark. He serves as an Associate Editor of IET POWER ELECTRONICS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and IEEE TRANSACTIONS ON POWER ELECTRONICS.

Guorong Zhu (M'11-SM'15) was born in Hunan, China. She received Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, China, in 2009. From 2002 to 2005, she was a Lecturer at the School of Electrical Engineering, Wuhan University of Science and Technology, Wuhan. From 2009 to 2011, she was a Research Assistant/Research Associate in the Department of Electronic and Information Engineering, the Hong Kong Polytechnic University, Kowloon, Hong Kong. From 2016 to 2017, she was a Visiting Scholar in the Department of Energy Technology, Aalborg University, Denmark. She is currently an Associate Professor at the School of Automation, Wuhan University of Technology, Wuhan, China. Her research interests are focused in the areas of Power Electronics Equipment Reliability, Battery Energy Storage Technology and Wireless Power Transfer Technology.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 500 journal papers in the fields of power electronics and its applications. He is the co-author of two monographs and editor of 7 books in power electronics and its applications. He has received 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2018 he is President Elect of IEEE Power Electronics Society. He is nominated in 2014, 2015, 2016 and 2017 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world. In 2017 he became Honoris Causa at University Politehnica Timisoara (UPT), Romania.