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An Overview of Carrier-based Modulation Methods for Z-Source Inverter

Review Article

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Abstract: Single-stage energy converters, in particular, the Z-Source Inverter (ZSI) or impedance source inverter, has gained significant attention in the recent years. ZSI ensures flexible energy conversions (dc–dc, dc–ac, ac–ac and ac–dc) because of its unique ability to boost the output voltage in typical renewable energy systems. The impedance network integrated between the energy source and the load contributes to the unique functionality of the ZSI. As substantial research has been conducted on the ZSI, this article provides a review on the operation of ZSI. The article initially examines the various topologies commonly adopted for the application of the ZSI. Subsequently, details of the various modulation methods that are commonly used to obtain the voltage boosting using ZSI are documented. Additionally, the phenomenon of neutral point formation, which is an important impediment to the adoption of multilevel ZSIs and the limitation of the modulation methods, is explained.

Keywords: *ac–dc power conversion • impedance source inverter • modulation methods • shoot through • phase opposition disposition • reference disposition*

1. Introduction

In the era of world transition, it is vital to redefine the means of energy generation in order to obtain affordable low carbon energy and to overcome deregulation of electricity. One of the best solutions is to utilize the renewable energy sources (Chambers et al., 2001; Jenkins et al., 2010) such as photovoltaic (PV), wind turbine and fuel cell technology (Roomi et al., 2014; Roomi et al., 2015; Roomi et al., 2016). However, PV and wind systems are prone to environmental factors. In the case of PV systems, intermittency and unpredictability of solar energy due to weather make the system unreliable. Variations in wind speed lead to uncertain and randomly fluctuating power from the wind power generator. Even though fuel cells are not prone to the fluctuations observed in PV or wind, low power generation remains a major downside. Hence, renewable energy sources require buffering elements such as energy storage systems and power electronic conditioning circuits before connecting to the utility mains or a power grid. Additionally, these systems experience problems with efficiency. Therefore, energy regulation is indispensable during the interfacing stage to provide efficient energy usage. With recent developments in power electronics, the aforementioned hurdles can be ameliorated.

Power electronic regulators consist of a power controller and a power converter and play a vital role in energy regulation. The power controller performs maximum power point tracking, grid synchronization and fast dynamic response in the system. The magnitude, frequency and electrical phase conversions are performed by the power converters. Energy conversion for applications involving ac motor drives (Banerjee and Ranganathan, 2009; Levi

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et al., 2007; Wu and Narimani, 2017; Zhang et al., 2012), renewable system interface (Carrasco et al., 2006; Panwar et al., 2011; Sørensen, 2007), distributed power generation (Bojoi et al., 2011; Mohamed and El-Saadany, 2008; Tuladhar et al., 2000; Xue et al., 2004), energy storage systems (Chen et al., 2009) and uninterruptible power sources (Deng et al., 2005; Escobar et al., 2007; Rymarski and Bernacki, 2016; Zhang et al., 2016) requires power converters with two-level and multilevel configurations. Fig. 1 demonstrates the outline configuration of energy conversion by renewable energy sources.

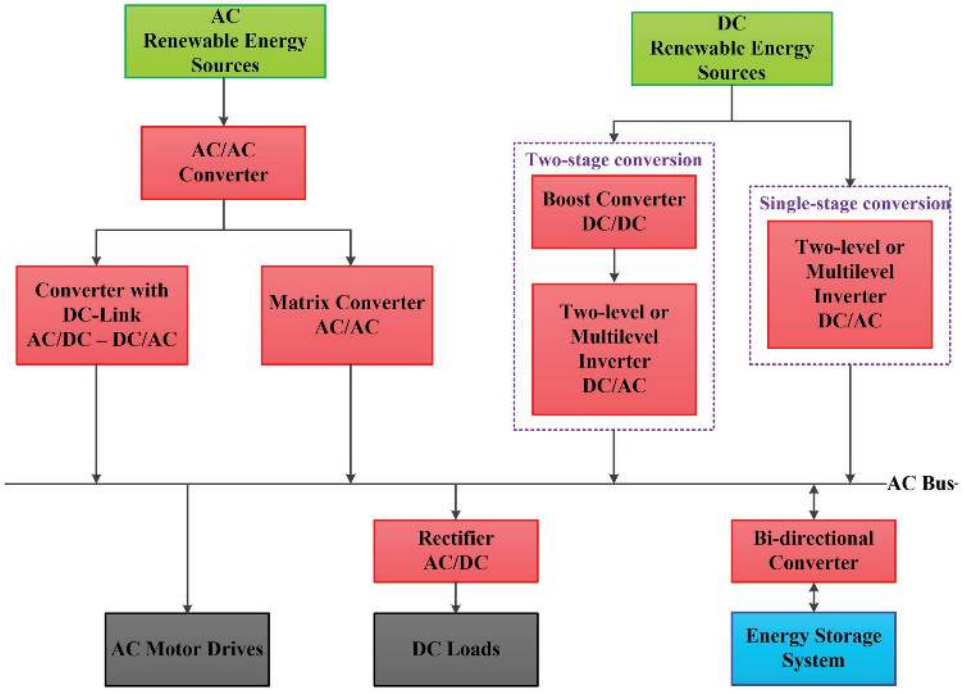

Fig. 1. Outline configuration of energy conversion by renewable energy sources.

The power converters are classified into Voltage Source Inverters (VSIs) and Current Source Inverters (CSIs) based on their power flow directions. The number of switches remains identical for both the converters. However, the difference is observed in the construction of the switches and the diode combination. VSI has an anti-parallel diode connected to each switch to provide bidirectional current flow and unidirectional voltage blocking characteristics (Colak et al., 2011). CSI has a diode connected in series with each switch to provide unidirectional current flow and bidirectional voltage blocking (Sahan et al., 2011). The dc input voltage needs to be greater than the ac output voltage in VSI, and ac output voltage should be greater than the dc input voltage in CSI. In order to operate the inverters efficiently, an additional boost or buck converter should be incorporated prior to the inverter. This mode of energy conversion involves a dc–dc conversion followed by a dc–ac inversion, hence named as two-stage energy conversion. Alternatively, energy conversions without employing boost or buck converter have been utilized in the research field. These inverters perform a direct conversion from dc to ac, and thereby this mode of energy conversion is referred to as single-stage energy conversion (Benavides and Chapman, 2005; Kumar and Sensarma, 2017; Rico-Secades et al., 2005; Walker and Sernia, 2004).

As mentioned earlier, the traditional VSI and CSI require a dc–dc conversion interface, which increases the system cost and lowers efficiency. When compared to the normal six-switch converter, boost converter has one additional switch. Inclusion of this additional switch, its corresponding driving circuits and other passive components, has rendered the boost converter with multiple components. Additionally, dead time protection must be provided in VSI to avoid Shoot Through (ST; gating 'on' of all the switches in the same phase leg). Safe current commutation in CSI is achieved by introducing overlap time (gating 'on' of one of the upper and one of the lower switches) to avoid open circuit of the dc inductor. The ST problem in VSI and the open circuit problem in CSI, which are caused by electromagnetic interference, highly affect the reliability of the converter. Furthermore, LC filter at the output of VSI causes additional power loss and adds to the complexity. Traditionally, two-stage energy

converters operate in eight switching states and provide either buck or boost operation. Therefore, the output voltage range is limited to the input voltage. The limitations of the traditional VSI and CSI can be amended by implementing a single-stage energy conversion. Some of the single-stage converters proposed in the literature include Cuk-derived buck–boost (Kikuchi and Lipo, 2001), Single-Ended Primary-Inductor Converter (SEPIC)-derived buck–boost (Veerachary, 2005) and Z-Source Inverter (ZSI; Peng, 2003). Among these inverters, ZSI is an emerging topology for dc–ac conversion. The advantages of ZSI over other converters are discussed in Section 2. Hence with primary focus being ZSI, a review on the carrier-based modulation methods for the ZSI is provided in this article.

Two-level inverters are highly preferred for induction motor applications due to their fast switching characteristics. Some applications require two-level inverters to operate at high switching frequency, in order to eliminate low-order harmonic (Steinke, 1999), which may reduce the filter size. However, high voltage stresses are introduced across the switches. Therefore, for high-power applications, additional switches are required to improve the voltage rating of the inverter. As a solution to this problem, Multilevel Inverters (MLIs) are proposed (Chen and He, 2006; Gupta et al., 2016; Ma et al., 2007; Peng, 2000; Rodriguez and Leeb, 2006; Rodriguez et al., 2002). Due to the advantages (Ghosh et al., 2017; Manjrekar et al., 2000; McGrath et al., 2006; Rech and Pinheiro, 2007) of the MLIs, these inverters are used for high-power applications. Some of the advantages include:

- MLI can be operated at both higher switching frequencies and lower switching frequencies
- Lower switching frequency indicates lower switching losses as the number of levels in the output voltage increases
- Total Harmonic Distortion (THD) reduces with the increase in the output voltage levels.
- MLI can draw input current with low distortion
- Selective harmonic elimination technique along with MLI topology results in low THD in the output waveform without using any filter circuit
- For high- and low-power inverter applications, low-rated semiconductor devices can be used due to low conduction loss

Among all the MLI topologies available, diode-clamped inverter (Bendre et al., 2006; Rodriguez et al., 2010; Wang et al., 2013; Zambra et al., 2010), flying capacitor inverter (Dargahi et al., 2015; Feng et al., 2007; Ghias et al., 2014; Huang and Corzine, 2006; Kang et al., 2005) and cascaded H-bridge inverter (Cortes et al., 2010; Corzine and Familiant, 2002; Kouro et al., 2009; Prasad et al., 2013) are the most common topologies. Integrating these topologies to provide single-stage energy conversion remains a highly preferred area of research.

The remainder of this review is structured as follows. It begins with a review on the single-stage energy converters in Section 2, followed by the description of the concepts of ZSI operation and their topologies in Section 3. A review of the multiple carrier-based modulation methods that can be implemented to insert the additional ST state to the traditional inverter operation is presented in Section 4. Finally, the concluding remarks are given in Section 5.

2. Single-stage energy converters

The main difference between the two-stage and single-stage converters is that the latter possess some functionalities to reduce the number of active and/or passive components in the system. Therefore, the single-stage energy converters combine the advantages of the buck and boost converters within one converter. These converters can act as a buck as well as a boost converter. Providing voltage buck–boost capabilities is achieved through the insertion of additional ST state during the inverter switching. The time interval of the state is adjusted to make the inverter operate in a buck or boost mode. Fig. 2(a) depicts the topology of Cuk-derived converters, and Fig. 2(b) shows the topology of SEPIC-derived converters for a two-level VSI. The voltage boost circuitries of these converters include an additional switch, an inductor and a capacitor connected to the rear end of the traditional VSI.

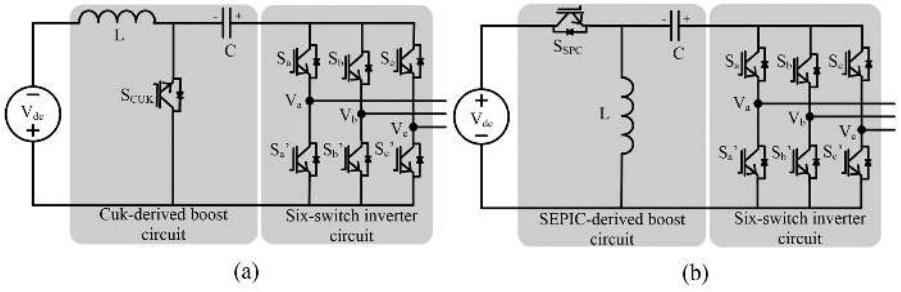

Fig. 2. Topology of single-stage converters: (a) Cuk-derived and (b) SEPIC-derived.

Traditional VSIs operate in eight switching states, including six active and two zero states. The operation of the inverter in these eight switching states is considered as Non-Shoot Through (N-ST) state in single-stage converters. However, the single-stage converters include an additional ST state that provides voltage boost capability. This state is introduced when the VSI is in its zero states. Therefore, no transfer of energy to the load occurs and the line voltage across the load remains zero. In the Cuk- and SEPIC-derived converters, the circuit operates in the ST state when the switches, S_{CUK} and S_{SEPIC}, are gated 'off'. The inductor is discharged, and the inductor current flows through the anti-parallel diode to charge the capacitor. Similarly, ZSI uses the ST state for voltage boosting. The carrier-based modulation methods are discussed and reviewed in Section 4, primarily focusing on the insertion of the ST states.

The single-stage topology to achieve voltage boost/buck abilities and fewer high frequency switching devices provides the ZSI with substantial advantages over the traditional boost or VSI. Furthermore, ZSI protects the devices from damage when the upper and lower switches of a leg are simultaneously switched 'on'. Another significant advantage of the ZSI topology is that a single controller is sufficient to perform inverter switching. Therefore, the complexity of the circuit is substantially reduced. Unlike Cuk- and SEPIC-derived inverters, dc-link current of the inverter does not flow through the antiparallel diode during the ST state. Instead, the current flows through the switches that are shorted. The dc inductors limit the current through the shorted switches, thereby preventing any damage to the switches. Therefore, ZSI exhibits lower electromagnetic noise when compared to other single-stage converters. A comparison of all the aforementioned converters is tabulated in Table 1.

Table 1. Comparison of two-stage and single-stage energy converters.

	dc/ac/dc converter		Cuk-derived	SEPIC-derived	Z-source
	dc/dc	VSI			
Input voltage	dc	dc	dc	dc	dc
Output voltage	dc	ac	ac	ac	ac
Voltage gain	Boost	Buck	Boost/buck	Boost/buck	Boost/buck
Inductors	1	0	1	1	2
Capacitors	1	0	1	1	2
Diodes	1	0	1	1	1
Switches	1	6	7	7	6
Merits	- Boost: Continuous input current, eliminates input filter - Buck: Continuous output current, low ripple in output voltage		- Continuous input and output currents - Output voltage can be either greater or less than input	- Minimal active components - Simple controller - Clamped switching provides low noise operation	- No dead time protection - Single controller for the switches - Output voltage can be any value between zero and infinity regardless of input voltage
Demerits	VSI: - Output voltage is limited - Gating of switches simultaneously in the same leg can damage the converter		- Complex compensation circuitry slows down the converter response - Uncontrolled and undamped resonance in output current-controlled Cuk	- Pulsating output current - High current capability capacitors required	- Not suitable for very low dc voltages - More passive components - Input current is discontinuous

VSI, voltage source inverter.

In addition, from Table 1, it can be surmised that ZSI requires additional passive components unlike other converters. This may result in greater conduction losses. Nevertheless, due to the smallness of the parasitic resistors, its effects can be disregarded. Due to these advantages, ZSI is considered a safer topology wherein the dead time protection is rendered redundant.

3. ZSI

Although ZSI has multiple advantages over other voltage buck–boost topologies, there are drawbacks associated with the inverter. The fundamental drawbacks include the discontinuity in the input current during boost mode and the difficulties in suppressing the inrush current by the impedance network during start-up. The topological configuration of the inverter has been modified to ameliorate these drawbacks. Some of the developed topologies are quasi-ZSI (Florez-Tapia et al., 2017), embedded ZSI (Loh et al., 2010), improved ZSI (Tang et al., 2009), trans-Z-source (Qian et al., 2011), distributed Z-source (Cha et al., 2010), extended boost ZSI (Gajanayake et al., 2010), T-source (Strzelecki et al., 2009) and Y-source (Siwakoti et al., 2014). Nevertheless, the topology includes a combination of inductors and capacitors for the different configurations and the modulation method for inverter switching remains the same. Therefore, in this article, the basic ZSI is considered for the two-level and three-level networks.

3.1. Two-level ZSI

The topology of ZSI consists of two inductors and two capacitors connected in X-shape forming an impedance network. Therefore, ZSI can also be considered as an impedance inverter. The two-level and three-level topologies of ZSI are portrayed in Fig. 3. The impedance network is fed by either a dc voltage source or a dc current source. The inductors used in the impedance network can be a split inductor or two different inductors. The inverter circuitry for the voltage-fed and current-fed ZSI follows the same configuration as the traditional VSI and CSI, respectively. ZSI is considered an attractive option superior to traditional converters due to its capability of delivering any value of output voltage regardless of the input, theoretically (Peng, 2003). As mentioned earlier, single-stage converters consist of an additional state, which is called the ST state. This state is introduced into the inverter operation by shorting the switches in any one-phase leg, or by shorting the switches in any two-phase leg, or by shorting the switches in all the three-phase legs. This state causes damage to the circuit in the traditional inverter, whereas it provides the unique buck–boost characteristic to the ZSI. The ST state is introduced in both the two-level and three-level operations of ZSI to ensure output voltage boosting.

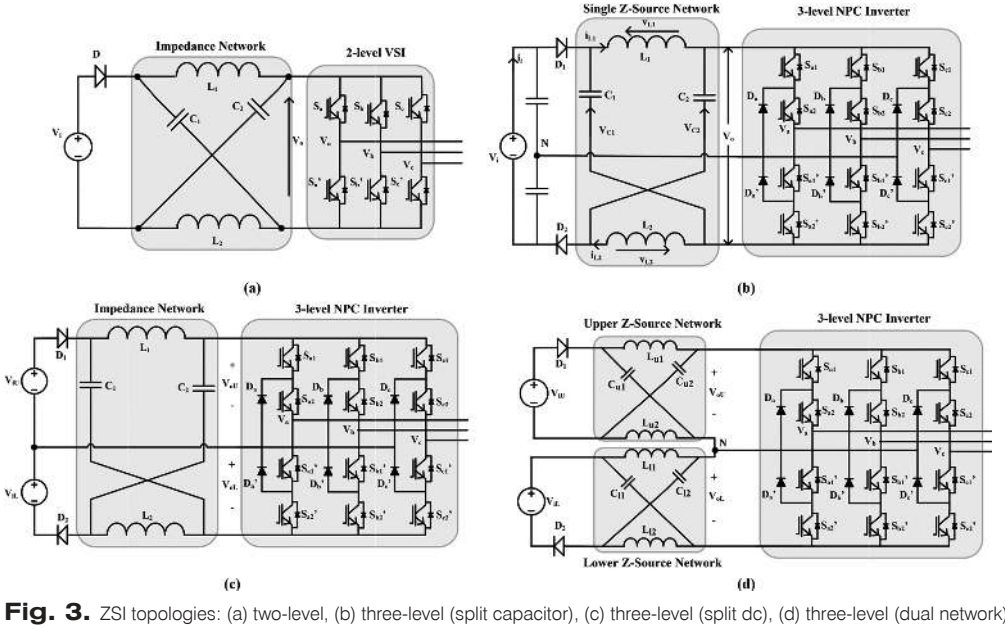

Fig. 3. ZSI topologies: (a) two-level, (b) three-level (split capacitor), (c) three-level (split dc), (d) three-level (dual network). ZSI, Z-source inverter.

For the two-level operation, ZSI operates in nine switching states (eight states such as traditional inverter and the additional ST state). The operation involves the charging of the two inductors in the impedance network that results in voltage boosting. In the two-level configuration as shown in Fig. 3(a), the ST state is achieved by shorting two switches in the same leg. This shorting causes damages to the circuit in the traditional inverter. However, due to the restricting action by the inductors, damages are prevented in ZSI. Furthermore, this aids in the boosting of the output voltage. As this gating of switches 'on' and 'off' in the same leg does not affect the circuit, ZSI can be operated without any dead time protection (Loh et al., 2008).

The operation of ZSI in nine switching states is classified into two modes: N-ST and ST states. N-ST state represents the operation of the inverter by comparing the three-phase reference sinusoidal signals with the triangular carrier signal. ST state represents the operation of the inverter due to an additional comparison with the carrier signal. Various modulation methods have been proposed to perform this additional comparison for the ST operation of the inverter. The objective of these modulation methods is to achieve a wide range of modulation, lower stress on the devices, minimum commutation per switching cycle and simpler implementation. Among the several modulation methods, ST insertion by carrier-based comparison methods is reviewed in Section 4.

3.2. Three-level ZSI

The three-level topologies as shown in Fig. 3 depict the possibilities of connecting ZSI to one of the MLIs. For medium-voltage applications such as ac motor drives, Neutral Point Clamped (NPC) inverters are the preferred topology (Rendusara et al., 2000). Hence, diode-clamped multilevel inverter is considered as a rear-end inverter configuration for the three-level ZSI topology. Two of the main topologies are the Single Z-Source Network Neutral Point Clamped (SZSN NPC) inverter and the Dual Z-Source Network Neutral Point Clamped (DZSN NPC) inverter. The topologies are classified based on the number of impedance networks in the system and the neutral point formation. Fig. 3(b) illustrates the traditional way of creating the neutral point using split capacitor bank (Shi et al., 2014). Fig. 3(c) shows another way of neutral point connection, where the neutral point is created between the dc sources (Loh et al., 2008). The input dc sources can be two individual voltage sources with the same rating or split input dc source. If two impedance networks are used instead of one, then the neutral point can be formed by connecting the neutral line between the two impedance networks (Loh et al., 2008), as illustrated in Fig. 3(d). Among the three topologies, the split capacitor bank topology introduces additional passive components to the circuit. Therefore, the SZSN with split dc source NPC inverter and DZSN NPC inverter are highly preferred.

The three-level ZSI also operates in two different modes: ST and N-ST states, which resembles the operation of two-level ZSI. The principle of boosting the voltage in three-level ZSI is achieved by utilizing the ST states. In the traditional two-level inverters, the full dc-link is shorted to provide voltage boosting. However, for the three-level ZSI, the ST states can be inserted in three different variations of switching: Full ST (FST) state, where all the switches (e.g. S_{a1}, S_{a2}, $S_{a1'}$, $S_{a2'}$) in a single leg are gated 'on', Upper ST (UST) state, where the upper three switches are gated 'on', and Lower ST (LST) state, where the lower three switches are gated 'on'. Furthermore, the main challenge lies in the careful insertion of these ST states into the inverter operation to achieve proper voltage boosting and neutral point balancing. In order to achieve this, various topologies have been proposed based on the space vector modulation. However, limited research has been conducted on the carrier comparison methods for the three-level ZSI NPC. Therefore, the following section reviews the possibilities of inserting ST for the three-level ZSI using carrier-based modulation methods.

4. Modulation methods

One of the efficient methods for controlling the inverter output is employing the Pulse Width Modulation (PWM) techniques. The switching devices in the inverters are controlled by the PWM methods to deliver outputs based on the load requirements. The attributes of these modulation methods can be analyzed based on the amplitude of the fundamental component, the losses in the switching devices, the flexibility of control and implementation and the harmonics in the inverter output.

Numerous PWM methods have been proposed for VSI. The traditional inverter has six active states when the load is connected to the dc voltage and two zero states when the load is shorted through the upper or lower switches of any leg. The traditional carrier comparison control of the inverter is simple. It involves the comparison of the

three-phase sinusoidal signals and the carrier signal. The inverter switching for ZSI requires additional modification, which is the insertion of ST states. The insertion of ST states does not cause any change to the active states. The zero states of the traditional inverter are utilized for the ST insertion without affecting the 'on' and 'off' time intervals (Peng, 2003). Therefore, proper modulation for the ZSI requires careful integration of the ST states into the zero states of the traditional converter.

Fig. 4 illustrates an overview of the ST state inserted in the zero states of the inverter. The ST states are inserted evenly during the start and end of the zero states. The various carrier comparison-based modulation methods for inserting ST in a two-level ZSI are Simple Boost Control (SBC), Maximum Boost Control (MBC), and Maximum Constant Boost Control (MCBC) methods.

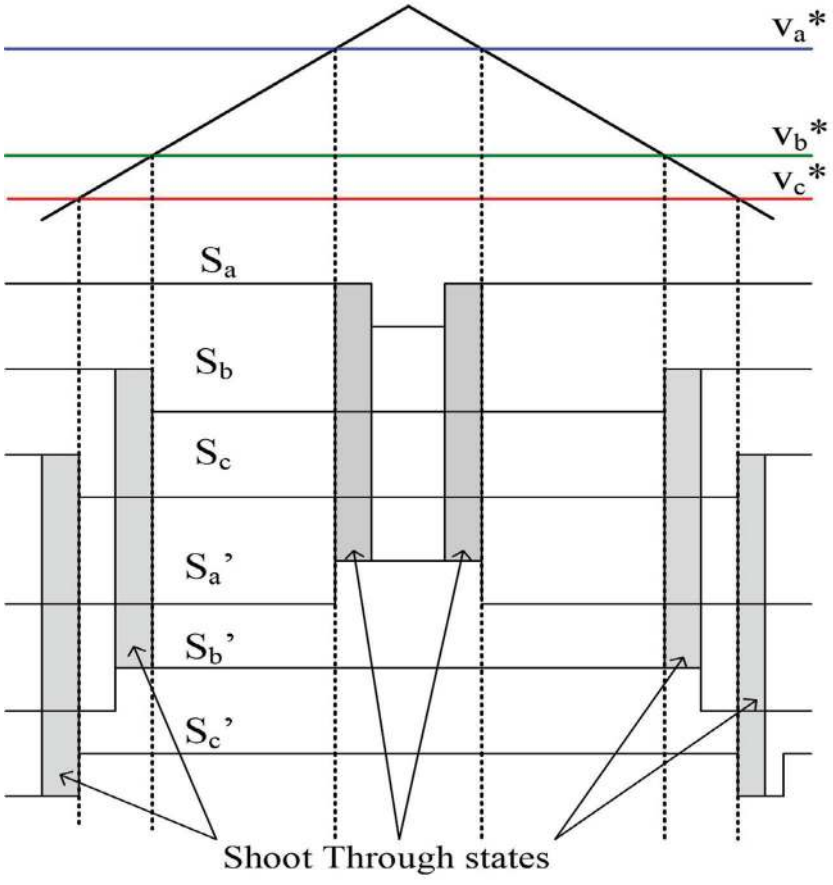

Fig. 4. Evenly distributed ST states in all the zero states. ST, shoot through.

4.1. Two-level ZSI

The modulation methods for a two-level ZSI are described as follows.

4.1.1. SBC method

The SBC method was developed by F. Z. Peng in 2003 (Peng, 2003). Fig. 5 portrays the carrier comparisons involved in inserting the ST state using the SBC method. Considered as the basic method for ZSI topology, this method involves the comparison of three-phase reference signals (V_a, V_b and V_c) with a carrier signal for N-ST operation of the inverter, and two straight ST lines (V_u and V_l) with the carrier for the ST operation of the inverter. The two straight lines, which should be greater than or equal to the peak value of the three-phase sinusoidal signals, are used to insert ST states in the modulation. When the carrier signal is greater than the upper line (V_u) or less than the bottom line (V_l), an additional state is introduced, and the circuit enters into ST mode.

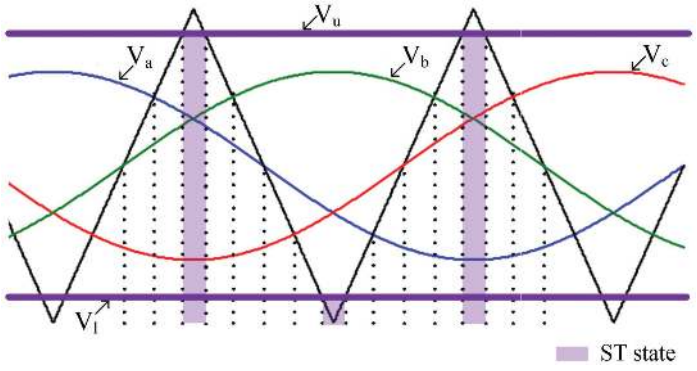

Fig. 5. Simple Boost Control method.

Even though this method provides simple control, the ST duty ratio (D) of the SBC method is limited by the modulation index (M), i.e. ($D_{max} = (1 - M)$). The ST duty ratio decreases with increase in the modulation index and reaches 0 for modulation index of 1. This attribute in SBC limits the boost factor. Therefore, SBC causes additional voltage stress on the switches for applications that require high voltage boost. This stress can be attributed to the fact that some traditional zero states are not utilized.

4.1.2. MBC method

Since the SBC method imposes voltage stress on the switches, it is necessary to minimize the stress, while maintaining the voltage gain. This can be achieved by increasing the ST duty ratio. This maximization technique ensures that all the traditional zero states are utilized, thereby changing every zero state to the ST state (Peng et al., 2005). Fig. 6 illustrates the signal comparisons using the MBC method. Unlike the SBC method, the MBC method does not possess two lines. Instead, the carrier signal is directly compared to the three-phase sinusoidal signals as illustrated in Fig. 6. The active states in the traditional PWM method remain unchanged. When the triangular signal is greater than the maximum reference sinusoidal signal or smaller than the minimum sinusoidal reference signal, the circuit enters into an ST state. The ST duty ratio is increased to the maximum possible value in this method, which subsequently improves the boost factor. This results in reduced voltage stress across the switches. However, the introduction of low-frequency ripples is a major drawback of the MBC method. As all the zero states are utilized as ST states, the time interval of the ST states varies. This results in the injection of ripple components in the inductor current and the capacitor voltage. Therefore, during low output frequency, a large inductor will be required. This increases the cost and volume of the passive components in the ZSI.

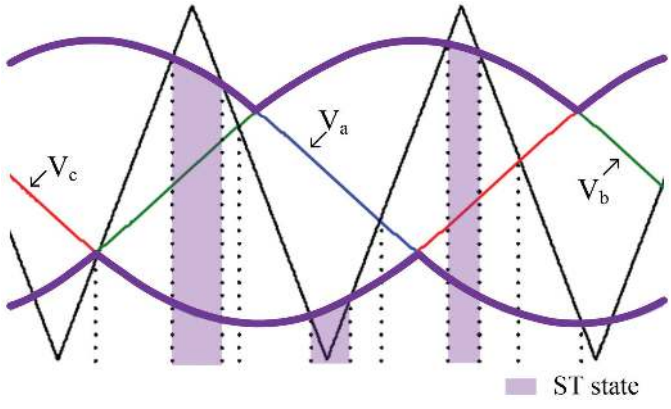

Fig. 6. Maximum Boost Control method.

4.1.3. MCBC method

Although the MBC method reduces voltage stress across the switches, the important challenge is the reduction of the ripple current and voltage in the circuit during the ST state. Additionally, if the volume and the cost need to

be reduced, it is necessary to maintain a constant ST duty ratio. Furthermore, in order to reduce voltage stress, the ST duty ratio must be at maximum, thereby providing maximum boost for any modulation index. All these drawbacks of the SBC and MBC methods are overcome by the MCBC method (Shen et al., 2006). Fig. 7 shows the ST insertion by implementing the MCBC method. This method obliterates the low-frequency ripple components in the impedance network. Therefore, the ripples in the inductor current and the capacitor voltage are reduced without increasing the volume of the passive components. Additionally, this method provides the maximum boosting capability while maintaining a constant duty ratio. This is achieved by using modified reference lines (V_u and V_l) as illustrated in Fig. 7. Using these modified reference lines, a constant interval is maintained between them, thereby providing a constant boost ratio. The upper modified reference line is greater than or equal to the positive peak of the reference signal and the lower modified reference line is equal to or lower than the negative peak of the reference signal. These modified lines are compared to the carrier signal. When the carrier signal is greater or less than the modified reference lines, the inverter enters into the ST mode of operation.

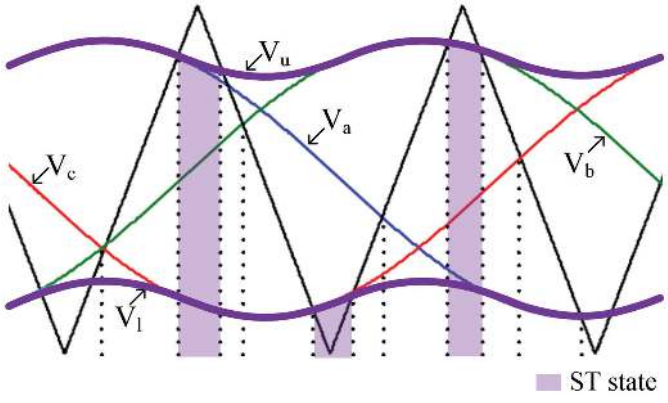

Fig. 7. Maximum Constant Boost Control method.

Alternatively, the MCBC method can be implemented by injecting a third harmonic component to the reference signals. By injecting the third harmonic components, the modulation index of the MCBC method can be increased from 1 to $2/\sqrt{3}$

4.2. Three-level ZSI

Several carrier modulation techniques are proposed and reviewed in the literature for MLIs (António-Ferreira et al., 2018). The basic Multi-Carrier PWM (M-C PWM) method provides an easy way to control the amplitude and frequency. The M-C PWM technique is categorized into Phase Shifted PWM (PS PWM) and Level Shifted PWM (LS PWM). Among these techniques, the most widely used technique for controlling the NPC inverter are the Phase Disposition (PD) modulation, the Phase Opposition Disposition (POD) modulation, and the Alternative POD (APOD) modulation methods (Gao et al., 2013; Hagiwara et al., 2010; McGrath and Holmes, 2002; McGrath et al., 2003; Shi et al., 2013; Song et al., 2013). For NPC MLIs, most carrier-based modulation methods are derived from disposition techniques, where for n-level inverter; $n-1$ carriers of identical frequency and amplitude are used to provide switching. The developed multi-carrier techniques for controlling the MLIs demonstrate the advantages of an optimized harmonic performance and a reduced common-mode voltage.

As mentioned in Section 3, voltage boosting in the ZSI occurs due to the addition of ST states to the traditional inverter. In the two-level ZSI, the ST occurs when all the switches in a single-phase, two-phase or three-phase leg are shorted. As mentioned earlier, the similar strategy of introducing ST in the three-level ZSI results in the additional ST states. These ST states are introduced due to the gating ‘on’ of top three switches in any leg (UST) or the gating ‘on’ of bottom three switches in any leg (LST). Therefore, the voltage boosting in the three-level ZSI occurs due to FST, UST and LST. The ZSI either uses an N-ST and an FST or an N-ST and a combination of UST and LST per switching cycle. During each state, the corresponding switches in the three-phase leg are triggered. The active switches and diodes for phase ‘a’ during the different operating states of the inverter are summarized and tabulated in Table 2. The carrier-based modulation methods that can be implemented for the three-level ZSI are

POD Level Shifted PWM (POD LSPWM), In-Phase Disposition Level Shifted PWM (I-PD LSPWM) and Reference Disposition Level Shifted PWM (RD LSPWM).

Table 2. Switching states of a three-level ZSI.

Operating states	Gated 'on' switches	Gated 'on' diodes	Output voltage
N-ST	S_{a1}, S_{a2}	D_1, D_2	$+v_i/2$
N-ST	S_{a2}, $S_{a1'}$	D_1, D_2 (D_a or $D_{a'}$)	0
N-ST	$S_{a1''}$, $S_{a2'}$	D_1, D_2	$-v_i/2$
FST	S_{a1}, S_{a2}, $S_{a1''}$, $S_{a2'}$	–	0
FST	S_{a1}, S_{a2}, $S_{a1''}$, S_{c2}, $S_{c1''}$, $S_{c2'}$	$D_{a''}$, D_c	0
UST	S_{a1}, S_{a2}, $S_{a1'}$	$D_{a''}$, D_1	–
LST	S_{a2}, $S_{a1''}$, $S_{a2'}$	D_a, D_2	–

FST, full shoot through; LST, lower shoot through; N-ST, non-shoot through; UST, upper shoot through; ZSI, Z-source inverter.

4.2.1. POD modulation method

In this method, the three-phase sinusoidal reference signals (V_{a*}, V_{b*} and V_{c*}) are compared to two triangular carrier signals (V_{carr+} and V_{carr-}), which are phase shifted by 180°. This comparison produces two individual gate signals for the upper two switches in each phase; and their corresponding inverted signals are given to the lower two switches. This modulation method used for the traditional three-level inverters can be extended to the three-level ZSI, because the rear end of both configurations is an NPC circuit (Shi et al., 2014). However, if no modification is made to the traditional switching sequence, this modulation method leads to voltage buck operation when used with ZSI.

Therefore, to boost the voltage using ZSI, the insertion of ST states must be carried out without making any modification to the normalized volt-sec average appearing across the load (Gao et al., 2010). Fig. 8 depicts the switching sequence of the POD modulation method for the three-level ZSI. As shown in Fig. 8, two additional signals, the UST and LST line, are utilized for the voltage boosting of the inverter.

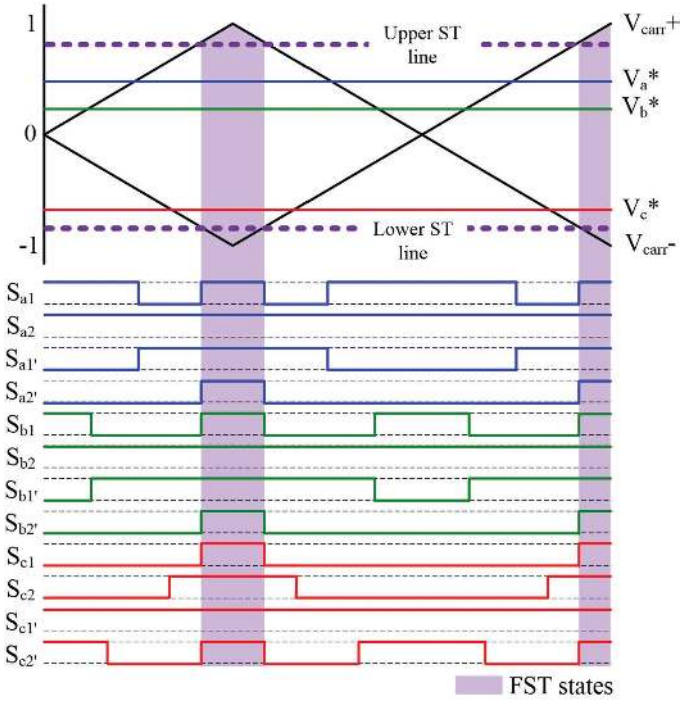

Fig. 8. POD LSPWM switching sequence for three-level Z-Source NPC. NPC, neutral point clamped; POD LSPWM, phase opposition disposition level shifted pulse width modulation.

The UST line is compared to one of the triangular carriers (V_{carr+}) and the LST line is compared to the other triangular carrier (V_{carr-}) to determine the insertions of ST states. From Fig. 8, it can be deduced that all switches are gated 'on' during the ST state leading to an FST state instead of a combination of UST and LST states. This is attributable to the fact that the ST due to the two ST lines occurs at the same period. From Table 2, it can be noted that the FST states are inserted either by gating 'on' all the switches in a single-phase leg or by gating 'on' a combination of switches from two-phase legs. However, implementing POD LSPWM leads to gating 'on' of all the switches in all three-phase legs at the same period. To maintain the normalized volt-sec average 'seen' by the load and to reduce the number of commutations per switching period, this method may not be suitable for the insertion of ST states in the three-level ZSI.

4.2.2. In-phase disposition modulation method

Similar to the POD modulation method, another method developed from multi-carrier comparison was I-PD LSPWM. This method produces less harmonic content. In this method, two triangular signals that are in phase with each other are compared to three reference sinusoidal signals to produce the switching sequence to the inverter. Like POD, a modified switching sequence is developed for using I-PD LSPWM with the three-level Z-Source NPC [49]. The modified method consists of two additional ST lines that are similar to the POD method. These ST lines are compared to the carrier signals to produce the ST states. The insertion of ST using the modified I-PD modulation method is shown in Fig. 9. As shown in Fig. 9, the UST line is compared to the carrier signal (V_{carr+}) and the inverter enters into the UST state; the LST line is compared to the carrier signal (V_{carr-}) and the inverter operates in the LST state. During these switching states, the control signal for a single-phase leg is 1110 for UST and 0111 for LST state.

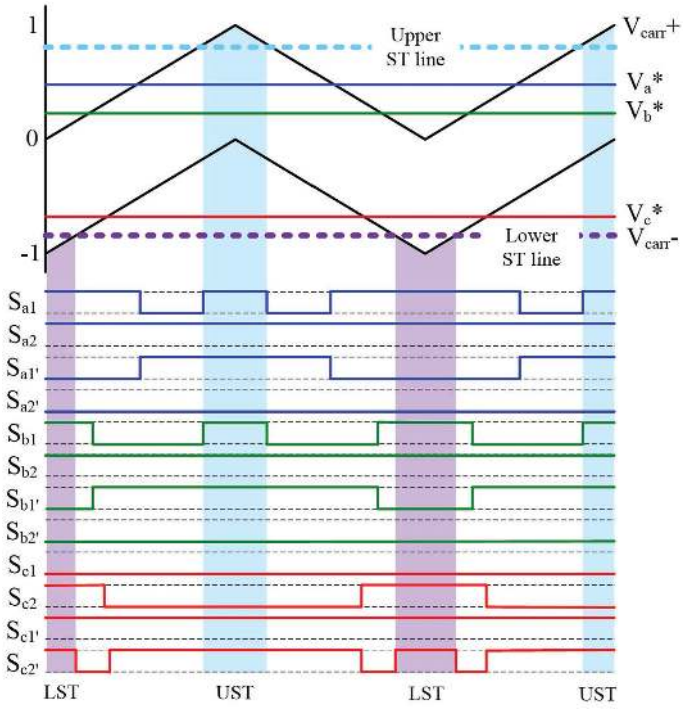

Fig. 9. I-PD LSPWM switching sequence for three-level Z-Source NPC. I-PD LSPWM, in-phase disposition level shifted pulse width modulation; NPC, neutral point clamped.

In addition, it can be noted from Fig. 9 that the FST state due to the gating 'on' of all switches in the three-phase leg does not occur during the carrier comparison. Hence, the voltage boosting using FST states is not possible. In order to use the I-PD LSPWM method for ZSI, the only option to insert the ST state is by a combination of the UST and LST states. The switches and diodes in operation during these UST and LST are tabulated in Table 2.

Insertion of ST states for voltage boosting using I-PD LSPWM does not involve FST states. Therefore, the normalized volt-sec average across the externally connected load remains unchanged, thereby reproducing the desired three-phase sinusoidal voltage output (Gao et al., 2010). Furthermore, less commutation per switching

cycle can be achieved using I-PD LSPWM when compared to POD LSPWM. However, care should be taken to ensure a balanced insertion of ST in the zero states to obtain undistorted voltage boosting.

4.2.3. Reference disposition modulation method

This modulation method, which is proposed in Roomi et al. (2017), uses two reference signals and one carrier signal, in contrary to the aforementioned carrier-based techniques. The two reference signals are level shifted with respect to each other, which when compared to the single carrier signal, provide switching sequence for the N-ST of the inverter. The ST states are introduced using two modified signals that are incorporated using the MCBC method. These modified signals along with reference disposition technique provide switching signals to the inverter. Similar to I-PD LSPWM, the boosting of the voltage in this method is attained by using the N-ST and the combination of LST and UST. Fig. 10 depicts the switching pattern of RD LSPWM for the three-level ZSI. The pattern comprises eight modulation signals: two sets of three reference signals V_{a1}, V_{b1}, V_{c1} & V_{a2}, V_{b2}, V_{c2}, upper modified ST line and a lower modified ST line. The reference signals (V_{a1}, V_{b1}, V_{c1}) trigger the switches S_{x1} and $S_{x1'}$ where x = a, b, c and the other reference signals (V_{a2}, V_{b2}, V_{c2}) are compared to trigger the switches S_{x2} and $S_{x2'}$ where x= a, b, c. The circuit enters into the UST state when the upper modified signal (which is equal to or greater than the peak value of the first set of reference signals) is lower than the carrier signal. Similarly, the circuit enters into the LST state when the lower modified signal (which is equal to the lower peak value of the second set of reference signals) is greater than the carrier signal. As discussed earlier, during the N-ST states, switching follows a pattern identical to that of the traditional carrier-based PWM, with the exception that the two reference signals and the carrier signal are compared. The analysis of ideal and nonideal condition of the circuits using RD LSPWM is presented in Roomi, 2017; Roomi et al. (2017).

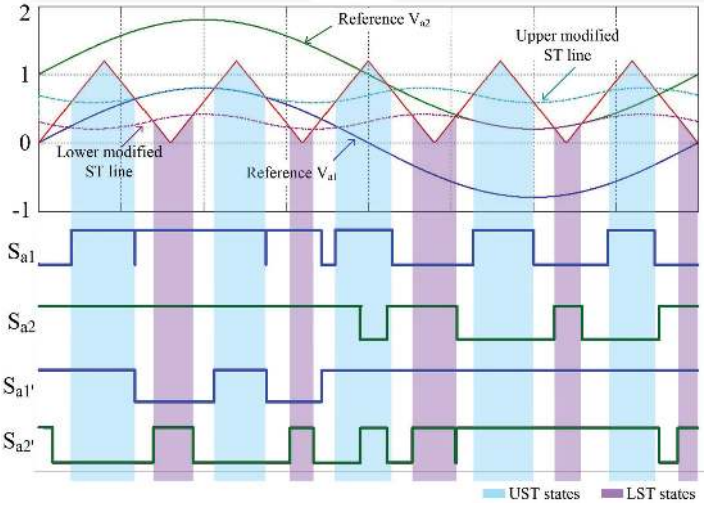

Fig. 10. RD LSPWM switching sequence for three-level Z-Source NPC. NPC, neutral point clamped; RD LSPWM, reference disposition level shifted pulse width modulation.

As shown in Fig. 10, it can be surmised that during the ST states, at least one of the switches in a single-phase leg remains 'off' during all the period. This proves that the voltage boosting by RD LSPWM is achieved by a combination of UST and LST. As the FST states are avoided by this technique, this concludes that the RD LSPWM results in less commutation per switching cycle when compared to POD LSPWM. However, the ST duty ratio is not constant, and this may introduce additional voltage stress on the switching devices.

Therefore, based on this analysis, the ST state in two-level and FST, UST and LST states in three-level ZSIs ensure the output voltage boosting of the ZSI. Although FST can be used for boost operation, gating 'on' all inverter switches leads to 'volt-sec error' (Gao et al., 2010) in the inverter output. Therefore, this state should be avoided. POD LSPWM uses FST states solely, whereas the other two techniques use a combination of UST and LST to perform the inverter operation. Hence, the latter two multi-carrier-based techniques may be considered for the three-level ZSI. A summary of the carrier-based modulation methods for the two-level and multilevel ZSI are tabulated in Table 3.

Table 3. Summary of the carrier modulation method for ZSI.

	Modulation method	Reference signals	Carrier signals	ST lines	ST state
Two-level ZSI	SBC PWM	3	1	–	FST
	MBC PWM	3	1	2 (straight) (+ve and –ve)	FST
	MCBC PWM	3	1	2 (modified) (+ve and –ve)	FST
Three-level ZSI	POD LSPWM	3	2	2 (modified) (+ve and –ve)	FST
	I-PD LSPWM	3	2	2 (modified) (+ve and –ve)	UST and LST
	RD LSPWM	6	1	2 (modified) (+ve)	UST and LST

–ve, negative; +ve, positive.
FST, full shoot through; I-PD LSPWM, in-phase disposition level shifted pulse width modulation; LST, lower shoot through; MBC, maximum boost control; MCBC, maximum constant boost control; POD LSPWM, phase opposition disposition level shifted pulse width modulation; PWM, pulse width modulation; RD LSPWM, reference disposition level shifted pulse width modulation; SBC, simple boost control; UST, upper shoot through; ZSI, Z-source inverter.

In addition to the SPWM techniques, Space Vector PWM (SVPWM) techniques are introduced for the two-level (Ali and Kamaraj, 2011; Ellabban et al., 2011; Jung and Keyhani, 2007; Liu et al., 2014) and three-level (Gao et al., 2007; Loh et al., 2009; Muniz et al., 2011) ZSIs. The ST states for the voltage boosting are introduced in the null states of the traditional inverter. Similar to SPWM, the insertion of ST states in any switching cycle remains crucial and needs proper attention. This is to ensure minimum commutation of the switches and the corresponding switching losses. As the focus of the article is the carrier-based comparison methods, further discussion of SVPWM falls beyond the scope of this article. However, the reviews provided in Loh et al. (2007) and Siwakoti et al. (2015) may be helpful for the readers to gain a further understanding of the SVPWM techniques for the three-level ZSI.

5. Conclusions

This article presented a review on the existing topologies and the carrier comparison-based modulation methods for the impedance source inverter for power conversion. It was discussed that even though MLIs are the primary choice for medium and high-power applications, these inverters cannot perform voltage–boost operation. To incorporate the boost capability into the inverter operation, the MLIs should be integrated with a dc–dc converter. The demand for single-stage converters over two-stage converters was addressed, and the possibilities of integrating NPC inverter and Z-Source buck–boost topology were determined. Moreover, the different topological configurations of the integration were explained.

The unique feature of the ZSI is the ST state; the insertion of which damages the circuit in traditional VSI. The limitations in traditional VSI can be overcome by configurational changes. Some of the proposed topologies were discussed in this article. Furthermore, different carrier-based modulation methods for inserting the ST state solely during the zero state for the two-level and three-level ZSIs were presented. Among the three modulation methods for the two-level operation, the MCBC method appears to be a promising technique due to its ability in achieving maximum voltage gain while maintaining a constant ST duty ratio. Similarly, with more switches in the three-level inverters, the ST states are classified into FST, UST and LST.

According to the modulation techniques discussed in this review for the three-level ZSI, it can be clearly concluded that implementing a modulation method that incorporates POD can introduce FST in the inverter switching. This state may cause volt-sec error, and hence, voltage boosting through this state should be avoided. Therefore, based on the comparative analysis that was performed, the techniques of in-phase disposition of carrier signals or reference signals can be considered as the preferred modulation methods for the three-level ZSI.

Declarations of interest

The authors have no declarations of interest to report.

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