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An Overview of High Frequency Switching Patterns of Cascaded Multilevel Inverters Suitable for PV Applications and Proposing a Modified Method

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Abstract

In this paper different high frequency switching methods for multilevel inverters which has been proposed for PV applications is analyzed; furthermore, the output harmonics content of phase shifted PWM (PSPWM) and in phase disposition PWM (IPDPWM) switching methods are comprised. This simulation results show that total harmonics content in IPDPWM is less than PSPWM method; besides, modified switching method of IPDPWM which solves the unequal power sharing problem of it is also proposed. This switching method is applied to a 7 levels inverter which is fed by three PV array DC sources and supply an AC load. These PV arrays deliver maximum power via DC-DC converter and perturb and observe algorithm. Simulation results show effectiveness of this method in sharing equal powers among different cells of the multilevel inverter which are supposed to be PV arrays; furthermore, results show that DC voltage ripples which cause inter harmonics are less than previous similar switching method; Hence for allowable DC voltage ripple, smaller capacitor is required. Simulation is implemented by MATLAB/SIMULINK software.

Keywords: Multilevel Inverter, Photovoltaic System, Power Conditioning

1. Introduction

In recent years using the multilevel inverters have been increased in different application such as Flexible AC Transmission System (FACTS), electrical machine drive and the interface of renewable energy[1]. Due to advantage such as low stress of switches, higher voltage capability and sine similar voltages[2]. Although different topologies of multilevel inverters have been proposed in recent years, the most popular of one are diode clamped, flying capacitors and cascade H-bridge[3,4]. In comparison to other configuration, cascaded H-bridge inverters which are built by connecting string of H-bridge inverters in series form because of the following reasons attracts more trend in power conditioning application. As aforementioned, H-bridge inverters are connected in series to form a CHB,; hence the structure has modular characteristic and independent Maximum Power Point Tracking (MPPT) are obtained in PV and wind turbine as cells of the Inverters. In this application, balance power sharing between different cells of CMI is critical challenge. Different Switching patterns which have been proposed by authors in multilevel inverters are categorized in low and high frequency groups. Selective harmonics elimination pulse width modulation (SHEPWM)[7–9] and Optimized Harmonic Stepped Waveform (OHSW)[10] are popular switching techniques in low switching frequency category. Space vector PWM and Sinusoidal PWM (SPWM) are also common High

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frequency switching patterns[11]. SPWM is also categorized into two groups of: Single Carrier SPWM (SCPWM) and sub-Harmonics PWM[12]. In Phase Disposition Pulse Width Modulation (IDPPWM) which is one of SCPWM category has lower Total Harmonics Distortion (THD). In this switching pattern, since, active periods of different cells is different, diverse powers are delivered by different CMI's cells. In[13], a modification of this switching pattern is proposed for solving these unbalanced powers sharing a method has been proposed for PV application. In this paper this switching method is also modified. This paper is organized as follow, at first, simulation of PV and MPPT algorithm is presented. The effectiveness of the MPPT algorithm is verified in this section. Then, IPDPWM method is applied to 7 level inverters which fed by constant DC sources and fast Fourier transformation harmonic spectrum of the output voltage of CHB is measured; furthermore, the result is compared with ''Phase shifted PWM" which is a high frequency switching pattern is used for case study. These results show that IPDPWM switching pattern has lower THD than PSPWM. Furthermore the switching pattern proposed in[13] is applied to 7-level inverters which fed by three photovoltaic system with independent MPPT. Simulations are done by MATLAB/SIMULINK. These results verify the effectiveness of the switching method decreasing dc link voltage ripples. Dc voltage ripple results 2M-1 inter harmonics in an M level inverter; hence, in allowable voltage ripples, smaller capacitors are needed. Using smaller capacitors reduces cost and weight of the system and increases the durability and reliability of the whole system.

2. PV Simulation

Sunlight energy is converted to the electrical energy by photovoltaic effect of photovoltaic cells. Figure 1 shows equivalent circuit of a photovoltaic cell. In this Figure I_{ph} and R_s represents cell photocurrent and internal resistance of the cell respectively. A parallel diode show the characteristic of semiconductor material which is used in photovoltaic cell. The leakage current of the cell which has been neglected by many authors is represented by shunt resistance (R_p)[6].

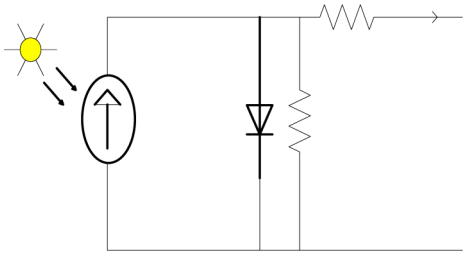

Figure 1. Electrical equivalent circuit of a PV cell.

Photovoltaic cell is described by Equation 1 neglecting the shunt resister[5].

$$I = I_{ph} - I_0(\exp(q(V + IR_s)/kTm - 1) \quad (1)$$

where k, m, T and q represent Boltzmann's constant, the ideality factor of the diode, absolute temperature of the cell and electron charge, respectively. The darkness saturation current of the cell is also represented by I_0. The photocurrent is depended to sun irradiance and temperature of photovoltaic cell. The relation is described by Equation 2:

$$I=(I_{SC}+\alpha(T_c-T_{ref}).G \quad (2)$$

In the recent equation, α and G represent the temperature coefficient and solar irradiance level of short circuit current of photovoltaic cell, respectively. Since each photovoltaic cell generates low power in small output voltage and small current; hence, the connection of the cells in series and parallel form is mandatory. The combination of the cells forms a module. The current of a module is written as Equation 3.

$$I = N_P I_{ph} - N_P I_0(\exp(q(V/N_S + IR_s/N_P)/kTm - 1) \quad (3)$$

where, N_p and N_s represent the number of parallel and the number of series photovoltaic cells which are connected to form a module. The simulation is based on the parameters of a Siemens sp75 module (Table 1).

In this paper ten PV modules are connected in series to form a PV array. *P-V* characteristic of the simulated PV array is depicted in Figure 2 in different solar irradiance (1000w/m^2 and 800w/m^2) conditions.

2.1 Maximum Power Point Tracking (MPPT)

As mentioned before, the output power which is delivered by the PV array is varied in different temperature and

Table 1. Parameters of the simulated PV module

Voc	21.7 V
V_{MPPT}	17 V
I_{SC}	4.8 A
I_{MPPT}	4.4 A
N_S	36

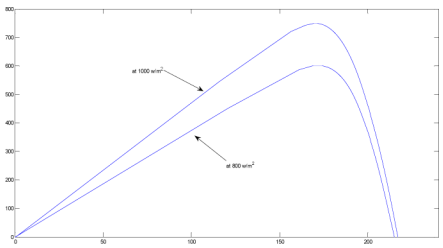

Figure 2. P-V characteristic of the simulated PV array.

solar irradiance condition; hence, the PV system should be able to track maximum power point. Perturb and Observe (P&O) pattern is a common maximum power point teaching method due to simply implementation of this pattern. This MPPT pattern is obtained via a DC/DC inverter which is chosen a boost converter in this paper and the flowchart is depicted in Figure 3. According the algorithm, a small perturb is applied in duty cycle of the boost converter and then the output power is measured and the algorithm is implemented[5].

Figure 4 shows the implementation of the simulation of PV and MPPT using MATLAB/SIMULINK software. As aforementioned a DC/DC boost converter is used; furthermore a 100Ωresistant as a load is considered. The effectiveness of the MPPT algorithm is tested by changing the irradiance in t=.8s from 800w/m^2 to 1000w/m^2. The irradiance is reduced in t=1.5s to 800w/m^2 from 1000w/m^2. The delivered power to resistant is depicted in Figure 4.

2.2 Cascaded Multilevel Inverters

As mentioned before, different topologies have been proposed for multilevel inverters and cascaded multilevel inverters are a suitable choice as interface of renewable resources such as PV to grid. The configuration of a seven level cascaded inverter is depicted in Figure 6. This figure shows that increasing the number of level will be resulted by adding H - bridge inverters. The number of multilevel phase voltage level can be written a follow:

$$L = 2M + 1 \tag{4}$$

where, M and L represent the number of DC sources and the number of multilevel phase voltage level. The output voltage of each cell is given

$$V_{Hi} = (P_{1i} - P_{2i}).V_{DC} \tag{5}$$

where, P_{1i} and P_{2i} are have discrete values of 1 and 0, so the values of V_{Hi} will be $-V_{DC}$, 0 and $+V_{DC}$ according to

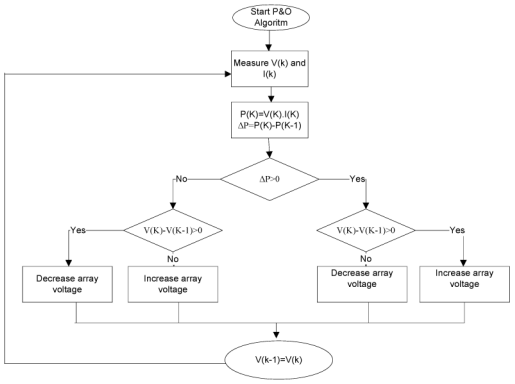

Figure 3. Flowchart of perturb and observe pattern.

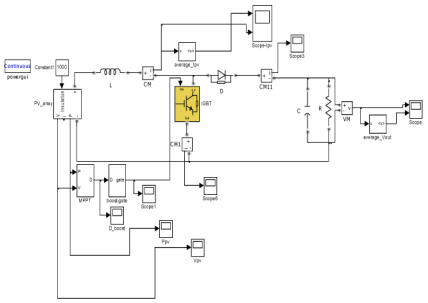

Figure 4. Simulation of PV and MPPT.

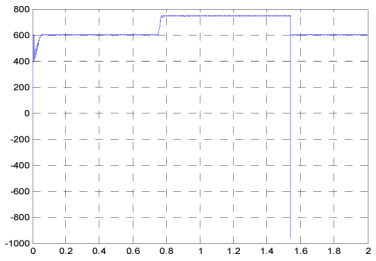

Figure 5. Output power of the PV system.

Equ.5 the number of the phase output voltage level will be increased by increasing the number of H-Bridge inverters which are connected in series form.

3. In Phase Disposition SPWM (IPDSPWM) Switching Pattern

The THD of output voltage is lower than other switching pattern in IPDSPWM[13]. In this switching pattern, the phase and amplitude of different cell's carrier waves which are compared with desired sinusoidal wave are the same but there is a different in dc level of them. In m-level CHB inverters, the amplitude of carrier waves is 2/ (m-1); hence in 7-level CHB inverter the amplitudes of these are 1/3. Figure 7 is depicted the carrier waves of seven level CHB

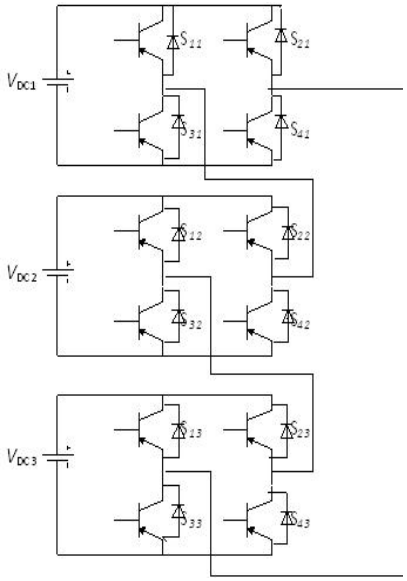

Figure 6. The equivalent circuit of 7-level cascaded multilevel inverter (CHB).

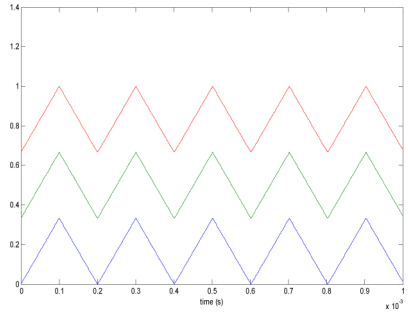

Figure 7. Carrier wave of In Phase Disposition PWM method.

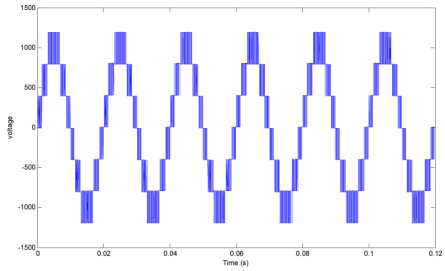

Figure 8. Output phase voltage of CHB inverter in In Phase Disposition SPWM switching pattern.

inverter considering 5kH switching frequency. Since, the DC levels of carrier waves are different; the active period of different cells will be different, so different powers are delivered by different dc sources. This switching pattern is applied to a 7-level inverter with equal dc sources which are shown in Figure 6.

By comparing the carrier wave as shown in Figure 7 by desire reference sinusoid wave, active period of upper cells will be less and active period of lower cells will be more. In high switching application another method named Phased Shifted PWM is used for power balancing between different cells of multilevel inverter. In this method, amplitudes of these carrier waves are the same but phases of them are different as shown in Figure 9. This method is also applied to pervious simulated system while all parameter such as equal DC voltages and switching frequency are the same except these carrier waves. For THD comparison, in "Phase Disposition SPWM" and ''Phase Shifted PWM" are compared and harmonic content of these methods are depicted in Figure 10 and Figure 11. As shown in Figure 10 and Figure 11 the THD of ''In Phase Disposition PWM" is less (i.e. about 12%) than THD of

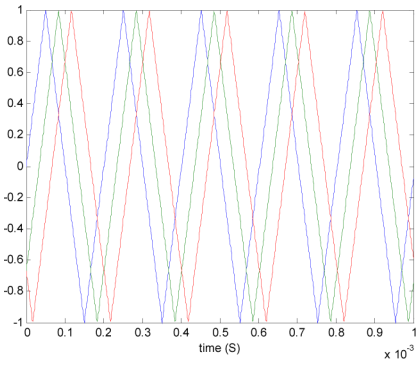

Figure 9. Carrier wave of Phase shifted PWM switching pattern.

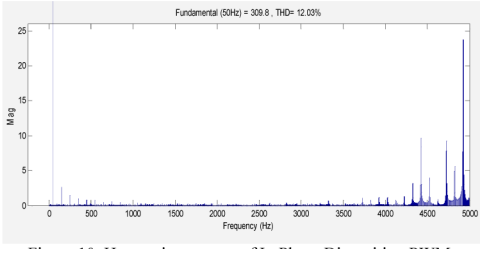

Figure 10. Harmonics content of In Phase Disposition PWM.

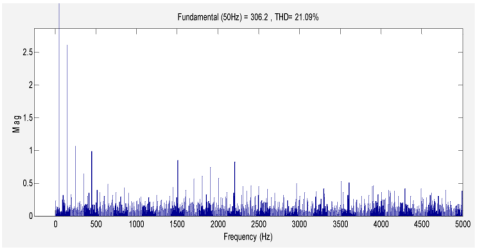

Figure 11. Harmonics content of Phase shifted PWM.

''Phase Shifted PWM" (i.e. about 21%). These results are performed in 5kH switching frequency and 0.8 modulation index. By balancing the power delivered by different cells in '' In Phase disposition PWM '' and without changing in output voltage of multilevel inverter, it will be a suitable switching pattern in power conditioning application. The low THD inverter can inject current with higher power quality, so filtering is more economical.

4. Investigated Method[13]

As mentioned in recent section, unbalance power sharing of different cells of multilevel inverter is caused, because of the difference between DC values of carrier waves; hence equal powers between cells is obtained while the average DC level of carrier waves of different cells are the same. In[13], a modification of IPDSPWM is proposed that DC level of carrier wave is shifted at each quarter of fundamental frequency (i.e. 50Hz or 60 Hz), so the average DC level of different cell will be the same and equal power sharing is obtained.

Figure 12 depicts the simulated carrier waves of 7-level inverter in proposed method. In this figure, the red color demonstrates the upper cell's switching carrier waves that show that the dc level of it is swapped after quarter of fundamental frequency (in this paper 50HZ).

5. Proposed Method

In the switching pattern which is proposed in this paper, the swapping of DC levels of different cells is taken place at each switching period (period of switching frequency) rather than after quarter of fundamental frequency which is in propose method in[13]. Since the average DC level of different cells are the same, equal power sharing between cells is obtained. In comparison to proposed switching pattern in[13], since swapping DC level of each cell is happen after each switching period, DC link capacitor are charged and discharged with more symmetric; hence, the voltage ripple across DC link capacitor will be less than switching pattern discussed in pervious section. These simulated carrier waves are shown in Figure 13 considering the switching frequency equal to 5kH.

As shown in this figure, the carrier wave which is depicted by red color is the carrier wave of the upper cell, it can be conceived from this figure that the dc level of it is swapped after one switching frequency period with the DC level of carrier wave of another cell.

6. Comparison of method in[13] and proposed method in this paper in application of PV connected

In this section, the proposed switching pattern and switching method proposed in 13 which are the modification of IPDSPWM switching pattern are applied in 7 multilevel inverter fed by three PV system. This simulated system is depicted in Figure 14.

In this figure, PV arrays which are shown with rectangular boxes are supplied 7-multilevel. The amount of DC link capacitors are chosen 1 mF and the impedance of AC load is considered as follow:

$$z = 100 + 2 * \Pi * 50 * .5 = 100 + 157\Omega$$

The simulation is implemented with the consideration that solar irradiance during the simulation is kept constant at 800w/m^2; furthermore, the simulated PV which is described in section II is used in this simulation. The switching frequency in this simulation is considered 5 kH.

In the first step of the simulation, the proposed switching pattern in[13] is used in switching of multilevel inverter which is fed three PV sources. The power delivered by different PV sources is depicted in Figure 15. This figure confirmed the effectiveness of the switching

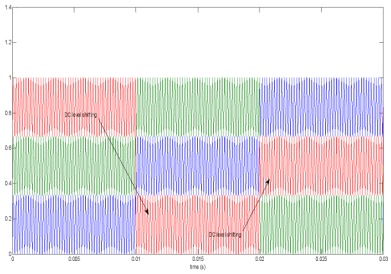

Figure 12. Simulated carrier wave of investigated method[13].

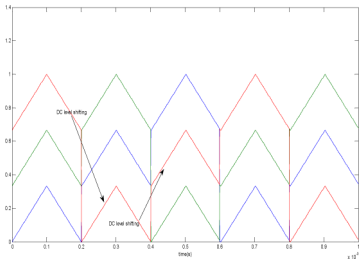

Figure 13. Carrier waves in proposed switching pattern considering 5 KH switching frequency.

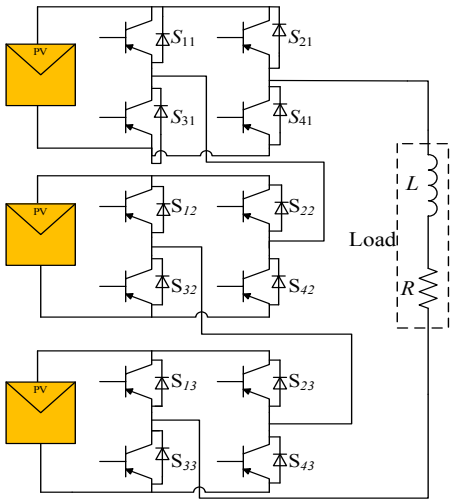

Figure 14. 7-level inverter fed by three PV arrays and suuplly a stand alone load.

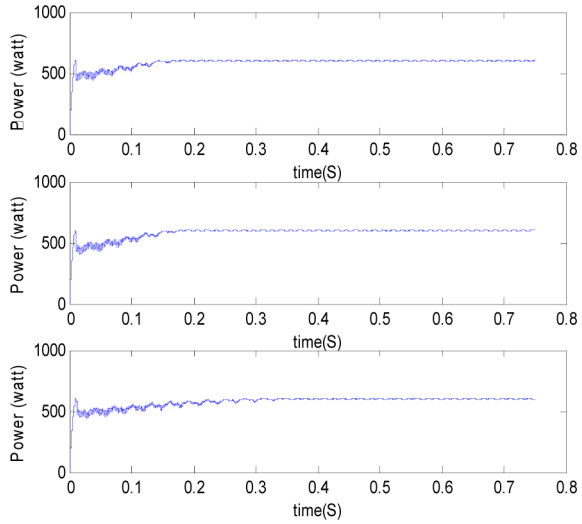

Figure 15. Delivered power of different cells of 7-level inverter by applying proposed switching pattern in[13].

pattern in improving power sharing between different PV arrays which supply the 7-level inverter; beside that, this figure shows that PV array operate in maximum power point (600 Watt).

Different capacitor dc link voltages and output voltages of different cells of the 7-level inverter are depicted in Figures 16 and 17, respectively. As shown in this figure the output voltage of each cell which shows the on or off state of switches in each cell, is not symmetric after one cycle of fundamental frequency (0.02 s). This shows that the time interval that each cell output voltage is negative is not equal to the time interval that each cell voltage

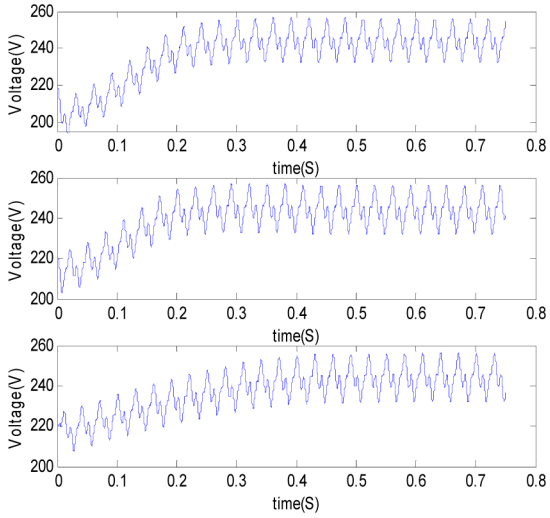

Figure 16. Three DC link capacitor voltages of 7-level inverter cells by using proposed switching pattern in[13].

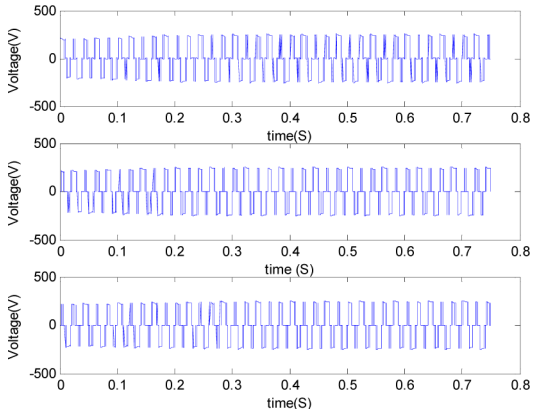

Figure 17. Three output voltage of inverter cells by applying proposed switching pattern in[13].

is positive. The results show the power sharing between different cells is obtained, but there is an inter-cycle difference between delivered powers of different cells of a CMI. This unbalance inters cycle different causes voltage ripples in DC link capacitors which cause inter harmonics in output voltage of inverters, hence decreasing the voltage ripples require larger capacitor which will increase the total cost and volume of the system, beside that it decrease reliability and lifetime of total PV connected multilevel inverters. The measured DC voltage ripple is about 12 % by using C=1 mF =1000 uF capacitor.

In the second step of the simulation, proposed switching pattern in this paper is applied to the 7-level inverter which is fed by three PVs. The carrier waves which are shown in Figure 13 are used; furthermore all parameter of the simulation is the same as first step. The power

delivered by different cells is shown in Figure 18. This figure shows that each PV array deliver their maximum power (i.e. 600 watt at 800w/m^2 solar irrational).

Figure 19 shows voltages across dc link capacitor and Figure 20 depict output voltages of different cells of multilevel inverter. Figure 20 shows that in comparison to pervious step of simulation, because of swapping the DC level of carrier waves of different cells after one switching period, output voltages are more symmetric at each fundamental frequency; hence the charge interval and discharge interval of dc link capacitors will be the same after one period of fundamental frequency; beside that, in the method not the power sharing between different cells is improved but also the inter-cycle difference of power problem is solved, since DC level of different cell's carrier waves are swapped after each period of switching frequency (i.e. at 5kH switching frequency, the cycle is 0.00004s) rather than quarter of fundamental frequency in proposed method in[13]. The measured voltage ripples in this simulation is 3% that is less than switching method

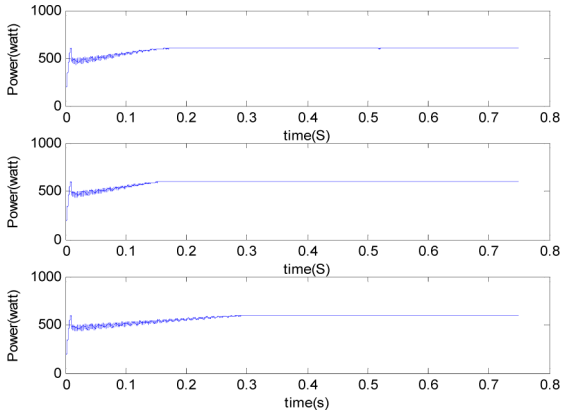

Figure 18. Power delivered by different PV arrays applying proposed switching pattern.

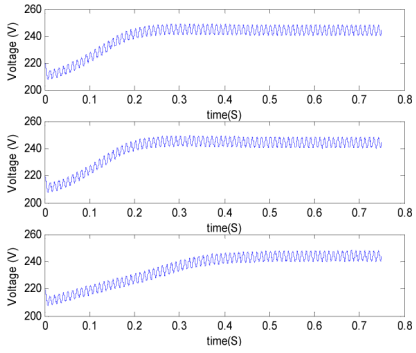

Figure 19. Voltages across DC link capacitor of inverter cells by applying proposed method.

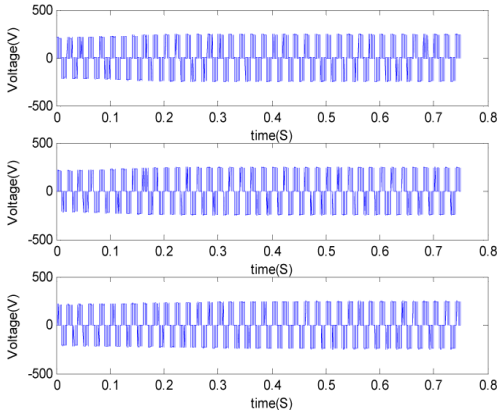

Figure 20. Output voltage of inverter cells by applying proposed switching method.

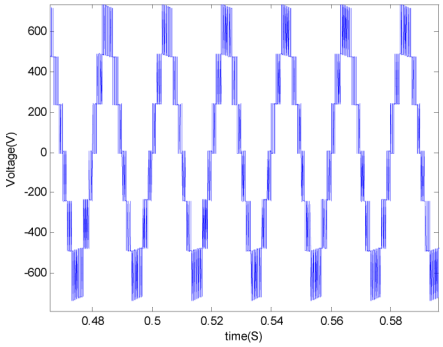

Figure 21. Output voltage of 7-level inverter supplied by PV using this proposed switching pattern.

proposed in[13]; hence, a smaller capacitor is required in this switching pattern in comparison to proposed switching pattern in[13].

Figure 21 depicts the output voltage of 7-level inverter which is feed by three PV arrays in the second step of simulation.

7. Conclusion

In this paper harmonics content of PSPWM and IPDPWM switching pattern that are two frequently used one in multilevel inverters is compared. The simulation results show that IPDPWM have much better harmonics content while this pattern is not suitable for power conditioning application due to unequal power sharing problem between different cells of CMI. A novel switching pattern which modifies the ''In Phase Disposition" and switching method where discussed in[13] is proposed in this paper. This method applied to 7-level multilevel inverter feed by 3 photovoltaic arrays which are operated at their

maximum power point and the proposed method not only solves unequal power sharing problem between different cells of multilevel inverters in "In Phase Disposition" but also in comparison with proposed method in[13], smaller amount of DC link capacitors are needed due to seduction of DC voltages ripples that causes inter harmonics. In proposed method, Reliability and lifetime of total system are increased and the cost and volume of it are decreased by using these smaller DC link capacitors.

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