An SEU Hardening Approach for High-Speed SiGe HBT Digital Logic

Ramkumar Krithivasan, *Student Member, IEEE*, Guofu Niu, *Senior Member, IEEE*, John D. Cressler, *Fellow, IEEE*, Steve M. Currie, Karl E. Fritz, Robert A. Reed, *Member, IEEE*, Paul W. Marshall, *Member, IEEE*, Pamela A. Riggs, Barbara A. Randall, and Barry Gilbert

***Abstract*—A new circuit-level single-event upset (SEU) hardening approach for high-speed SiGe HBT current-steering digital logic is introduced and analyzed using both device and circuit simulations. The workhorse D-type flip-flop circuit architecture is modified in order to significantly improve its SEU immunity. Partial elimination of the effect of cross-coupling at the transistor level in the storage cell of this new circuit decreases its vulnerability to SEU. The SEU response of this new circuit is quantitatively compared with three other D flip-flop architectures, including the unhardened circuit, a conventional NAND gate based circuit, and a current-sharing hardened (CSH) circuit, at both variable data rate and switching current. The new circuit shows substantial improvement in SEU response over the unhardened version, with little increase in layout complexity and power consumption. While the NAND gate based circuit still shows better SEU response than the other circuits, its high power consumption will preclude its use in space applications. Our results suggest that this new circuit architecture exhibits sufficient SEU tolerance, low layout complexity, and modest power consumption, and thus should prove suitable for many space applications requiring very high-speed digital logic.**

***Index Terms*—Charge collection, circuit modeling, current-steering logic, HBT, SiGe, single-event effects (SEE).**

I. Introduction

SiGe HBT technology has recently emerged as a contender for high-speed digital, analog, RF, and microwave applications, due to its higher intrinsic performance than Si technology at similar processing complexity, and better cost-performance than III-V technology. SiGe HBTs have proven to be robust to various types of total dose ionizing radiation, as fabricated, in terms of both dc and ac electrical characteristics, making them potentially attractive for space applications. Recently, however, high-speed SiGe HBT digital logic circuits were found to be potentially vulnerable to single-event upset (SEU), and have been examined through both ion-beam testing and charge collection modeling. SEU sensitivity in SiGe HBT digital logic, as it is for any bipolar logic, depends on the circuit implementation, and hence one can in principle alter the circuit configuration in order to minimize SEU sensitivity. Previously, a comparison of SEU response in multiple SiGe HBT digital logic circuits indicated that cross-coupling at the transistor level in the storage cell negates any moderate SEU immunity achieved through circuit-level hardening using the current-shared hardening (CSH) [1] technique [2]. In this work, we propose an implementation of D flip-flop digital logic with a new circuit architecture featuring limited transistor-level decoupling in the storage cell and compare its predicted SEU response with three other circuit architectures. While maintaining the basic functionality of the storage cell of the D flip-flop, the new circuit achieves considerable SEU immunity over the CSH version and the unhardened version of the D flip-flop [3] with little power or real estate overhead.

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R. Krithivasan and J. D. Cressler are with Electrical and Computer Engineering Department, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: ramkumar@ece.gatech.edu).

G. Niu is with the Electrical and Computer Engineering Department, Auburn University, Auburn, AL 36849 USA.

S. M. Currie, K. E. Fritz, P. A. Riggs, B. A. Randall, and B. Gilbert are with the Mayo Foundation, Rochester, MN 55905 USA.

R. A. Reed and P. M. Marshall are with NASA-GSFC, Greenbelt, MD 20771 USA.

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II. Device Technology

A schematic cross-section of a SiGe HBT used in the device and circuit simulations is shown in Fig. 1 The SiGe HBT, fabricated by IBM (SiGe 5HP), has a planar, self-aligned structure with a conventional polysilicon emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. The p-type substrate and the n-p-n layers of the intrinsic transistor form a n-p-n-p multilayer structure, complicating the charge collection process during ion strikes. This SiGe HBT technology features a peak f_T of 50 GHz and a peak $f_{\max}$ of 70 GHz [4]. The p-type substrate is biased at the lowest potential (-5.2 V and -3.3 V in this case) for isolation.

III. Device Simulations and Circuit Modeling

MEDICI [5] was used for quasi 3-D device simulations of the charge collection mechanisms, which involved using MEDICI in cylindrical symmetric mode [6]. The SiGe HBT doping profile and Ge profile in the base were constructed using measured SIMS data and calibrated to measured dc and ac electrical characteristics. The ion charge track was generated over a period of 10 picoseconds using a Gaussian waveform. The Gaussian has a $1/\mathrm{e}$ characteristic time scale of 2 picoseconds, a $1/\mathrm{e}$ characteristic radius of 0.2 μm, and the peak of the Gaussian occurs at 4 picoseconds. The depth of the charge track is assumed to be 10 μm, and as substrate doping of $5 \times 10^{15}/\mathrm{cm}^3$ was used. A uniform LET of 0.5 pC/μm was used along the charge track in this work. (An LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm in silicon.) In order to ensure that our simu-

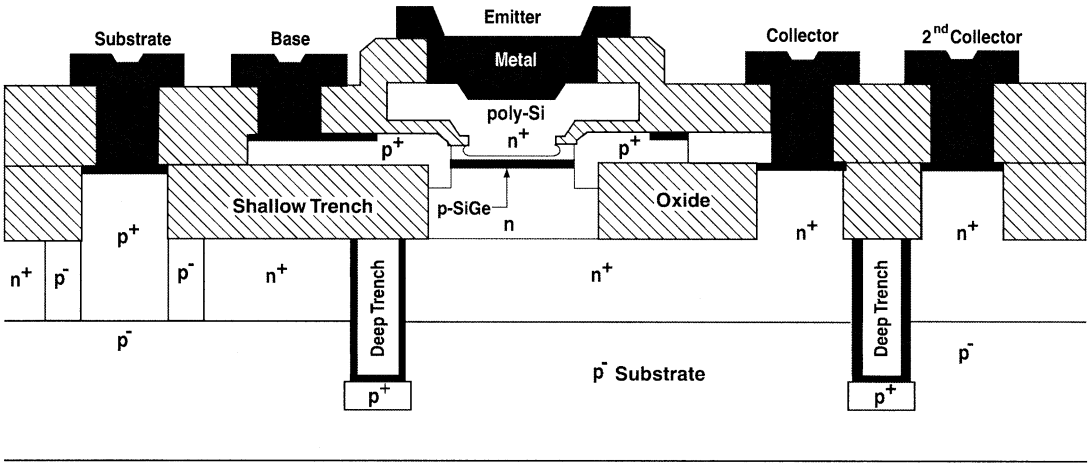

Fig. 1. The schematic cross-section of the SiGe HBT used in the simulations.

lated charge profiles were reasonable, we have compared simulations to actual microbeam data for a 36 MeV oxygen ion. We used the SRIM program to estimate the actual LET profile inside the device. As the spatial distribution of this LET profile was nonuniform, it is difficult to compare the net LET to the uniform LET used in our device simulations. However, the total collector-collected charge via device simulation was approximately 800 fC in this case, which is close to the value of 700 fC obtained for the peak charge collected in the collector for an actual 36 MeV oxygen ion in the microbeam experiment [7]. This agreement between the simulated collector-collected charge and that from actual microbeam data establishes the predictive capability of our model and hence lends credence to the circuit results presented.

The SEU response of the circuits was determined by integrating the SEE-induced transient terminal currents obtained from device simulation into a circuit simulation tool via an equivalent circuit model, as shown in Fig. 2 [8]. The current sources in the equivalent circuit model represent the transient terminal currents. The SEE-induced transient currents at the emitter and collector are denoted as i_{en} and i_{cn}, where the subscript n indicates "electron collection," while those at the base and substrate are denoted as i_{bp}, and i_{sp}, where p indicates "hole collection." As the sum of all of the terminal currents is always zero, we only need to include any three of the four currents, and the other current is automatically accounted for. Therefore, SEE-induced collector current, i_{cn}, is given by

$$i_{cn} = -(i_{bp} + i_{sp} + i_{en}). \tag{1}$$

Thus, this equivalent circuit model allows us to perform quasi mixed mode SEU simulation in a robust manner.

IV. Circuit Descriptions

A new D flip-flop circuit (denoted here as circuit C) was implemented by incorporating duplicate pass and storage cells to effectively produce decoupling of the differential inputs and outputs in the storage cell. The SEU response of circuit C was compared with that of three other D flip-flop circuits, including two unhardened circuits (denoted as circuits A and D), and a CSH-hardened version of circuit A (denoted as circuit B). All of the four circuits have the identical logical functionality of a rising edge-triggered D flip-flop under normal operating conditions (i.e., without SEU).

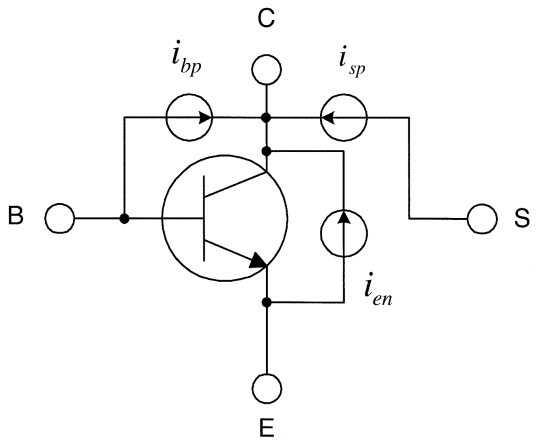

Fig. 2. An equivalent circuit model for including the ion-induced terminal currents in the circuit simulations.

A. Circuit A, B, and D

Detailed circuit descriptions of circuits A, B, and D along with their merits and demerits with respect to SEU can be found in [3]. Circuit A is the unhardened version of the D flip-flop used in the shift registers tested in [2]. The transistor level circuit is shown in Fig. 3.

Circuit D is a standard NAND gate based implementation of the conventional rising edge-triggered flip-flop logic Fig. 4. Circuit A uses a fewer number of transistors than circuit D.

Circuit B is the CSH-hardened version of circuit A. This circuit was used as a basic building block of the 32 stage shift-register tested in [2]. Each transistor element in Fig. 3 was implemented with a five path CSH scheme (Fig. 5). These five current paths remain separate through the clocking stage and through the storage and pass cells until the load. The transistors in the storage and pass cells, however, eventually share the same load.

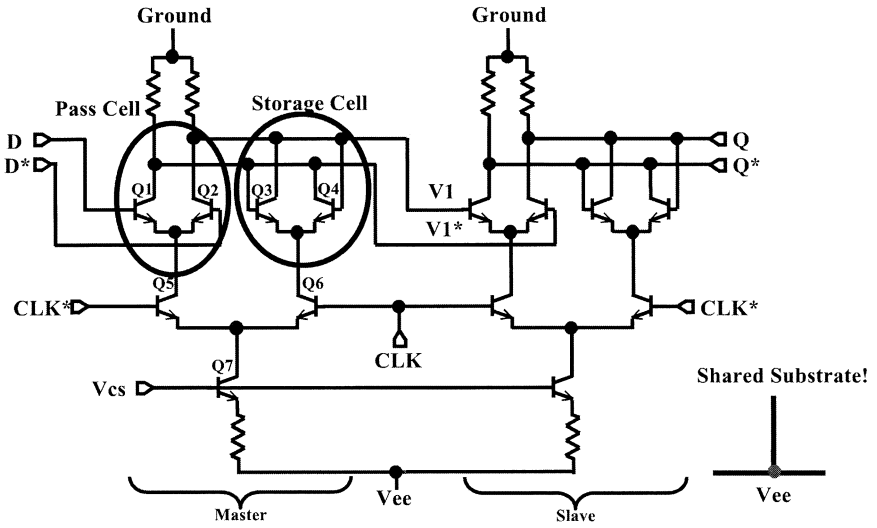

Fig. 3. Schematic of circuit A—the unhardened version of the D flip-flop used in the shift registers tested in [2].

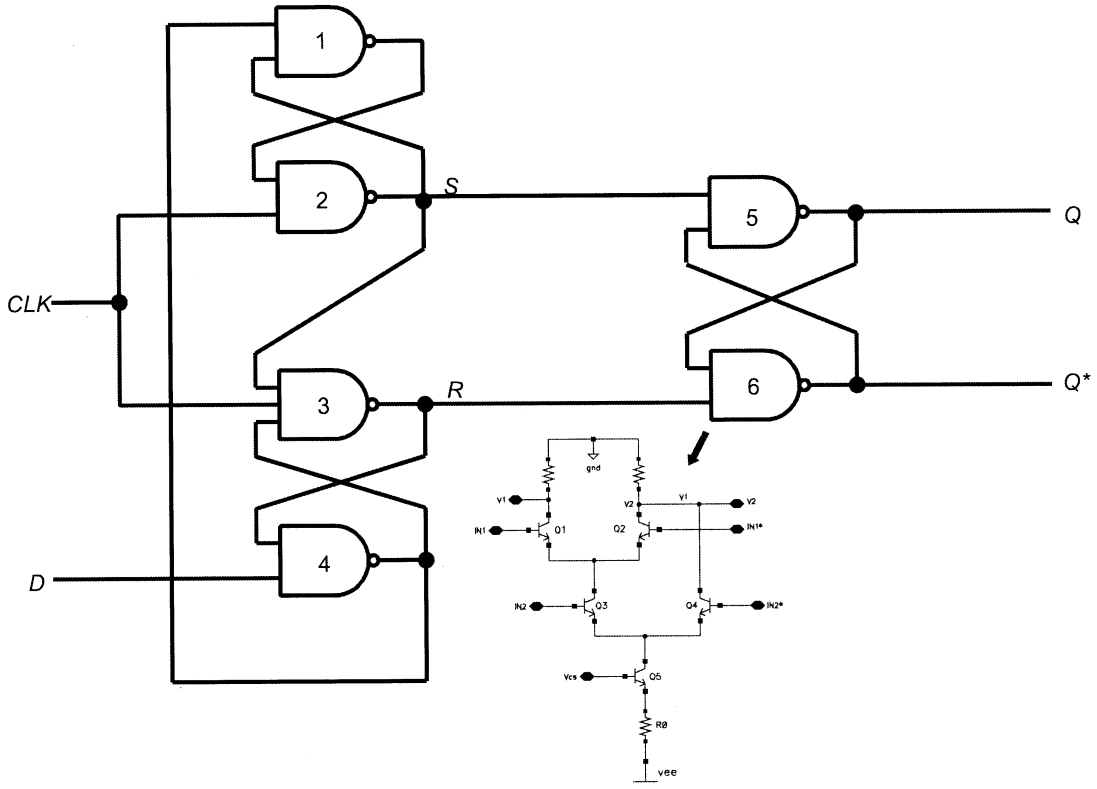

Fig. 4. Schematic of circuit D—Logic diagram of a standard rising edge-triggered D flip-flop with ECL implementation of a two-input NAND gate in the inset.

B. Circuit C

Circuit C, the new circuit proposed in this work, implements limited decoupling of the storage cell transistor inputs (base) and outputs (collector) in the master and the slave stages of the flip-flop, as shown in Fig. 6. This circuit is very similar to circuit A, except for the presence of a duplicate cell for each cell in circuit A. Although circuit C may appear to simply be two unhardened D flip-flop circuits (circuit A) wired in parallel, a careful examination of the connections in the storage cell shows that this is not the case. While the collectors of Q5 and Q6 are connected to the collectors of Q3 and Q4, the bases are connected to the collectors of Q1 and Q2, respectively. In the case of two D flip-flops wired in parallel, however, one would expect the collectors and bases of Q5 and Q6 to be connected to the collectors and bases of Q1 and Q2 in Fig. 3, and likewise for Q7 and Q8.

This new configuration maintains the basic functionality of the storage cell of storing data when the clock goes high. Effective decoupling is achieved by not connecting the base and the collector of the transistors in the storage cell to the same differential pair in the pass cell. For example, the base of Q5 is connected to the collector of Q1, whereas the collector of Q5 is con-

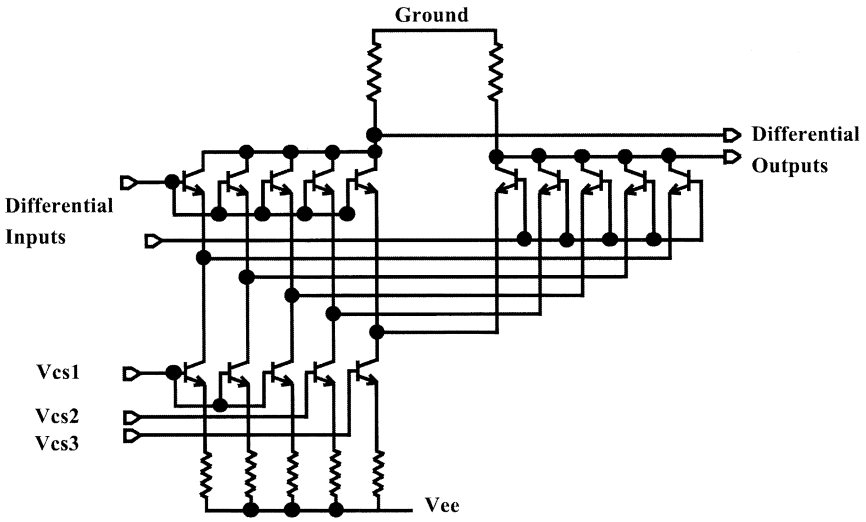

Fig. 5. Illustration of current-sharing hardening (CSH) concept using a basic ECL gate. Five parallel (sub)transistor elements are used to maintain separate current paths.

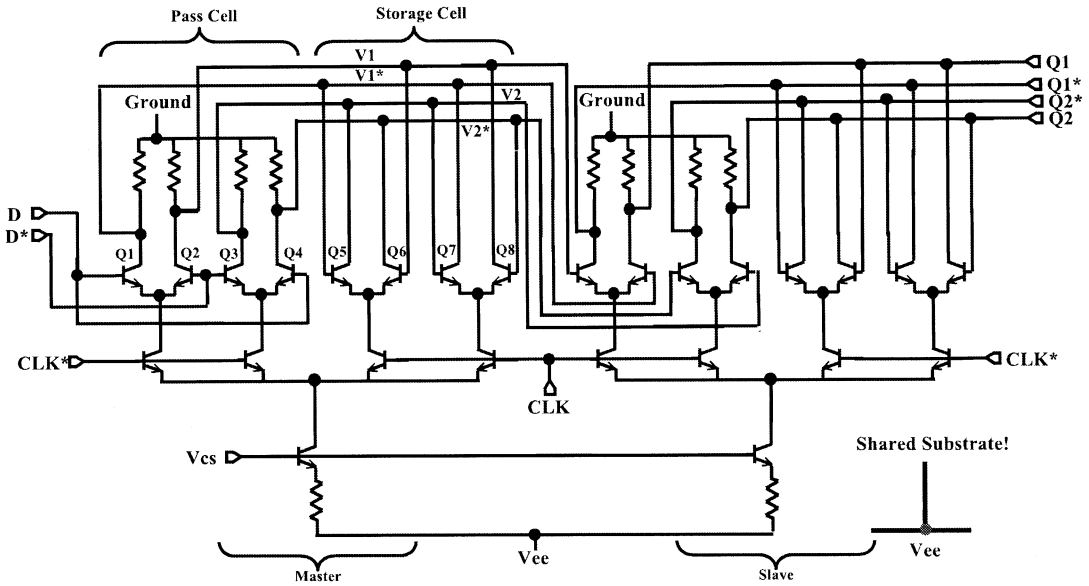

Fig. 6. Schematic of circuit C—the new D flip-flop with minimal cross-coupling in the storage cell.

nected to the collector of Q3 (note that the base and collector of each transistor in the storage cell are connected to complementary outputs from the pass cell, which is essential for storage cell functionality). Thus, if SEU transient current flows through the collector of the transistor Q5, the base is unaffected by this current flow. The voltage drop due to this transient flow does affect the base Q7, however, which might indirectly affect the base of Q5, potentially leading to upset.

TABLE I
POWER CONSUMPTION AND NUMBER OF TRANSISTORS IN THE CIRCUITS

Topology	Power Consumption		Number of transistors
	Switching Current=1.5mA	Switching Current=0.5mA	
Circuit A	3P	P	14
Circuit B	3P	P	70
Circuit C	6P	2P	26
Circuit D	12P	4P	56

V. CIRCUIT SIMULATIONS

Circuit transient response simulations were performed using the Spectre simulator in Cadence, using calibrated VBIC compact models for the SiGe HBT in the SiGe BiCMOS design kit from IBM. The transistor being subjected to an ion-strike is replaced with the equivalent circuit model (Fig. 2) and the SEE-induced transient terminal currents are turned on during the course of the transient simulation.

Simulations were performed at three different data rates (2, 4, and 6 Gbit/s). The simulations for the various circuits were made at a constant switching current of 1.5 mA. In order to study the effect of variable switching current on SEU response,

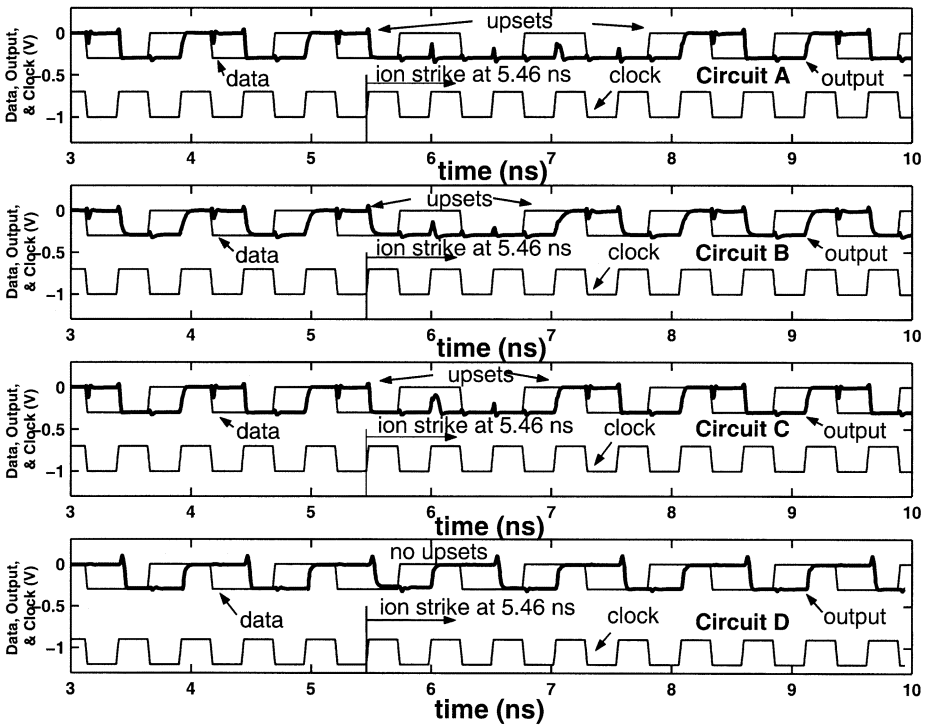

Fig. 7. Data, output, and clock waveforms of circuits A to D (top-to-bottom) at a data rate of 2 Gbit/s (LET $= 0.5$ pC/μm and switch current is 1.5 mA).

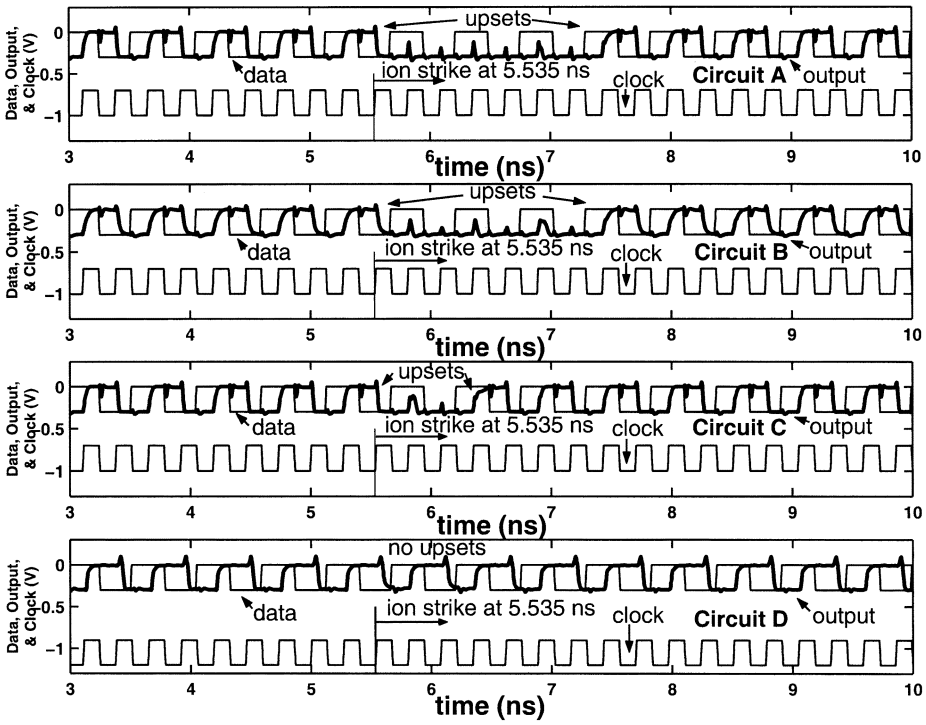

Fig. 8. Data, output, and clock waveforms of circuits A to D (top-to-bottom) at a data rate of 4 Gbit/s (LET $= 0.5$ pC/μm and switch current is 1.5 mA).

simulations were also performed at a 0.5 mA fixing the data rate at 2 Gbit/s. The input data was an alternating train of '1' and '0' bits, and the voltage swing was maintained at 300 mV (swinging between -300 mV and 0 V) in all the circuits, irrespective of the switching current or the data rate.

The upset-sensitive transistors in each D flip-flop circuit were identified (as described in [3]) and SEE-induced transient currents were activated on these transistors. In each circuit, the transient currents were triggered just before the rising clock edge, when the data is still '0', since this condition was determined to

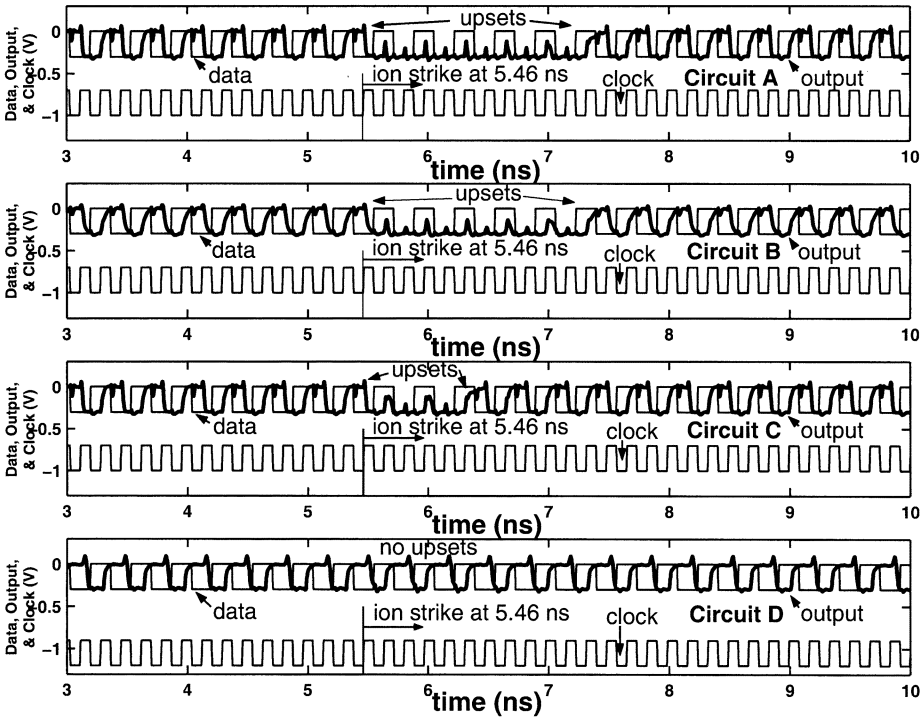

Fig. 9. Data, output, and clock waveforms of circuits A to D (top-to-bottom) at a data rate of 6 Gbit/s (LET $= 0.5$ pC/μm and switch current is 1.5 mA).

be worst case. Such conditions occur at 5.460 ns after the start of the simulation for data rates of 2 and 6 Gbit/s for 1.5 mA switch current, and at 5.535 ns for 4 Gbit/s at 1.5 mA switching current.

VI. Results and Discussion

A. Performance Analysis

Table I shows the trade-off between power consumption and the number of transistors required to implement the various circuits. The power consumption of all the circuits are computed relative to the power consumption of circuit A (Fig. 3) at a switching current of 0.5 mA (designated as P).

We compared the SEU response of each circuit at three different data rates for a fixed switching current of 1.5 mA. Figs. 7–9 show the simulated SEU responses for circuits A, B, C, and D at three data rates simulated here. The SEU response is measured in terms of bit error rate (BER) (or alternatively, recovery time).

Circuit A, as expected, shows the maximum number of upset bits across all data rates. Although circuit B shows slightly better SEU response at 2, 4, and 6 Gbit/s, it has a performance similar to circuit A. Circuit D shows the best performance compared to all the circuits, with no upsets at any data rate. It is clear from the SEU response at higher data rates, however, that with just half the power consumption of circuit D and with many fewer transistors, we can achieve significant improvement in SEU response (BER or recovery time) using the new circuit C architecture.

The circuits were also operated at a switching current of 0.5 mA with the data rate maintained at 2 Gbit/s, as shown in Fig. 10. We see that in general the SEU performance has degraded significantly in all of the circuits, with circuit D (which showed no upsets for any data rate at 1.5 mA switching current) now showing upsets.

Fig. 11 summarizes the SEU results of the four circuit architectures using as a metric the number of upset bits/unit power consumption as a function of data rate.

B. Understanding the Results

In any current-steering logic, the input signal to one of the transistors of the differential pair is compared with either a static reference voltage (single-ended input) or the complementary input signal (differential input) at the input of the other transistor. All the circuits investigated in this work operate with a differential input signal. In the storage cell of circuit A (and B), the input (base) of the transistor Q3 is connected to the output (collector) of the transistor Q4 (and Q1) (Fig. 3). Similarly, the input to transistor Q4 is connected to the output of the transistor Q3 (and Q2). This cross-coupling of the inputs and outputs of the differential pair in circuits A and B, which is essential for latching, presents a strong positive feedback, as previously pointed out [3]. As a result, an upset occurring at the output of any of the transistors in the storage cell influences the other transistor to an equal and opposite extent, reinforcing the upset in the differential output. This explains the poor SEU tolerance in circuits A and B at both switching currents and at all data rates. In circuit B, although the current paths are maintained as separate through the clocking stage, and pass and storage cells, the loads are shared (as in circuit A), effectively making this circuit equally vulnerable to SEU.

In circuit D, however, where this transistor-level cross-coupling within a differential pair is entirely absent, we do not

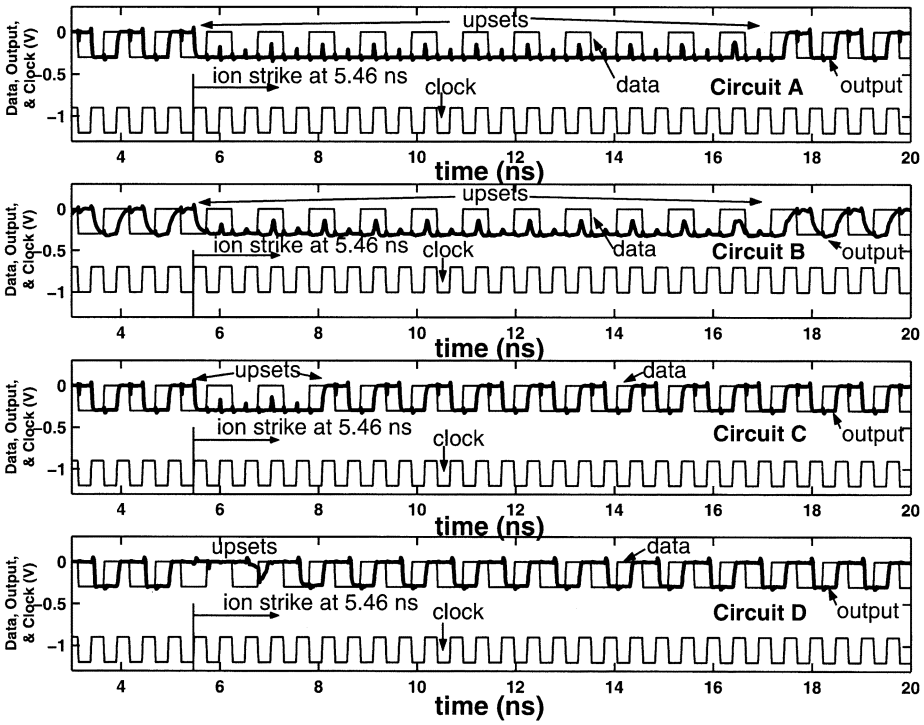

Fig. 10. Data, output, and clock waveforms of circuits A to D (top-to-bottom) at a data rate of 2 Gbit/s ($\mathrm{LET} = 0.5$ pC/μm and switch current is 0.5 mA).

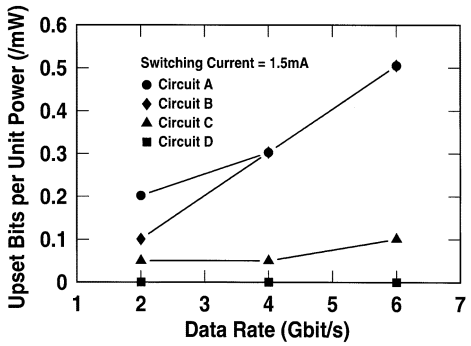

Fig. 11. Summary comparison of the four circuit architectures using as a metric, the number of upset bits/unit power consumption as a function of data rate.

see any significant upset at the output due to SEU transient currents. The differential outputs are independent of each other, and therefore upsets occurring in one of the outputs does not affect the complement output. As long as the differential output is above the cell switching threshold, the output remains unaffected, and no SEU upset occurs. However, it is worth pointing out that the storage cells in this type of D flip-flop still incorporate cross-coupling between gates required for latching, but there is no cross-coupling within a differential pair as such.

The analysis of the SEU response in circuits A, B, and D indicate that if one of the inputs to the storage cell differential pair is unaffected by SEU, we see no significant SEU at the differential output. In circuit D this condition is always satisfied, while in circuits A and B, it is always violated. The very high power consumption of circuit D (Table I), however, might preclude its use in space applications. In circuit C, the above-mentioned condition for SEU tolerance is partially satisfied due to the use of duplicate pass and storage cells (Fig. 6). The use of duplicate pass cells present independent loads to the input and output of transistors in the storage cell. In order to maintain the basic functionality of the storage cell, however, we still need a positive feedback, and therefore, cross-coupling between transistors having same logic level but from different storage cells (as explained above). Hence, upsets, although significantly fewer than in circuits A and B, can still be seen at the output.

Figs. 12–14 show the differential output of the storage cell at 0.5 mA switching current. It is clear from these figures that both the outputs are affected to an equal and opposite extent in circuit A. In circuits C and D, however, only one of the outputs is affected. In circuit C (Fig. 13), soon after triggering the SEU transient currents, when the clock goes high and when there is upset in one of the terminals, we also see upset in the opposite terminal (for example, observe the change in V1 slightly after 6 ns). This upset occurs due to pass cell of the slave stage turning ON as a result of the clock going high, and since V1* is high (due to upset), V1 goes low.

The degradation of the overall SEU response at low switching current is due to large load resistance needed to maintain the voltage swing, and hence due to a lower switching threshold. The same SEU transient current now flows through this larger load resistance, leading to a more pronounced upset. In circuits C (D), however, the differential output of one of the storage cells, V1 and V1* (V2 and V1 in circuit D), are not affected to

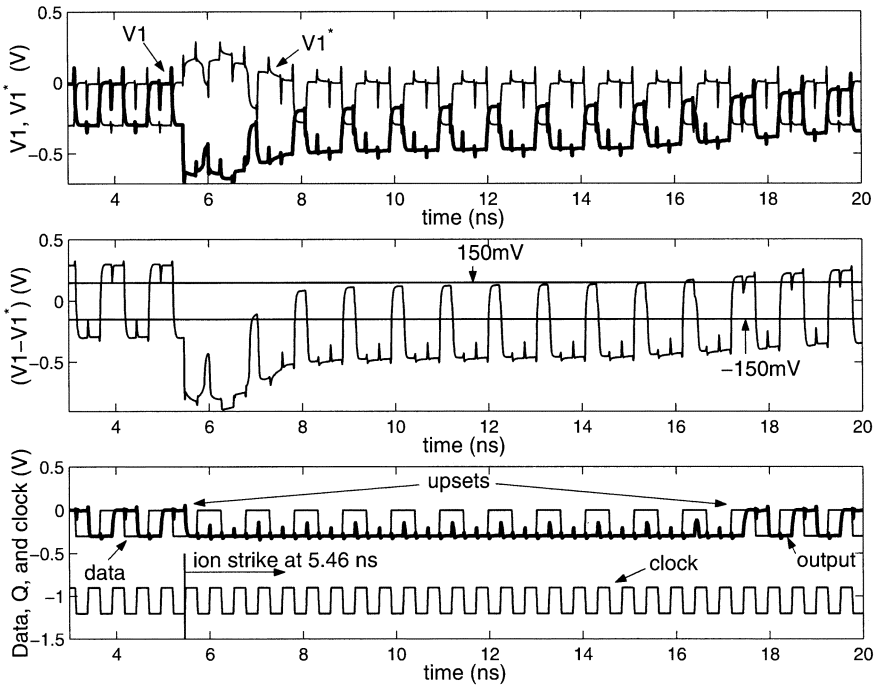

Fig. 12. Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in circuit A (switch current is 0.5 mA).

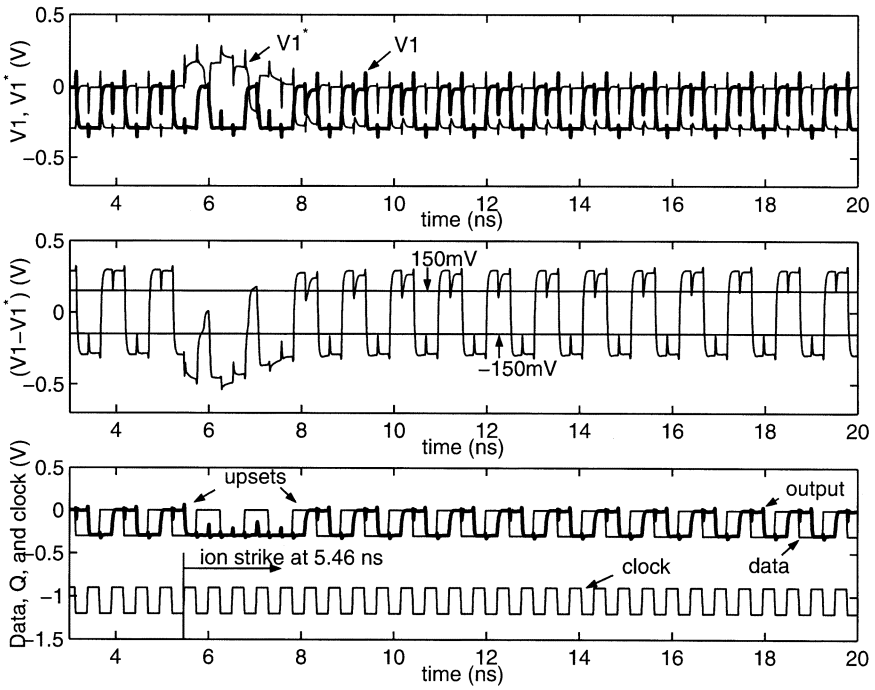

Fig. 13. Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in circuit C (switch current is 0.5 mA).

the extent to which they are affected in circuits A and B. Therefore, fewer upsets occur in circuits C and D at low switching current.

VII. Summary

A new circuit architecture for high-speed SiGe HBT digital logic having moderate SEU tolerance is implemented by partial decoupling of the differential output. The SEU response of this circuit architecture is compared with the response of three SiGe HBT D flip-flop architectures, including one previously tested CSH-hardened circuit, and two unhardened circuits. The performance of this new circuit is comparable to the NAND-based D flip-flop circuit that has no transistor level cross-coupling, but at much lower power consumption and fewer transistor count. The significant improvement in SEU response

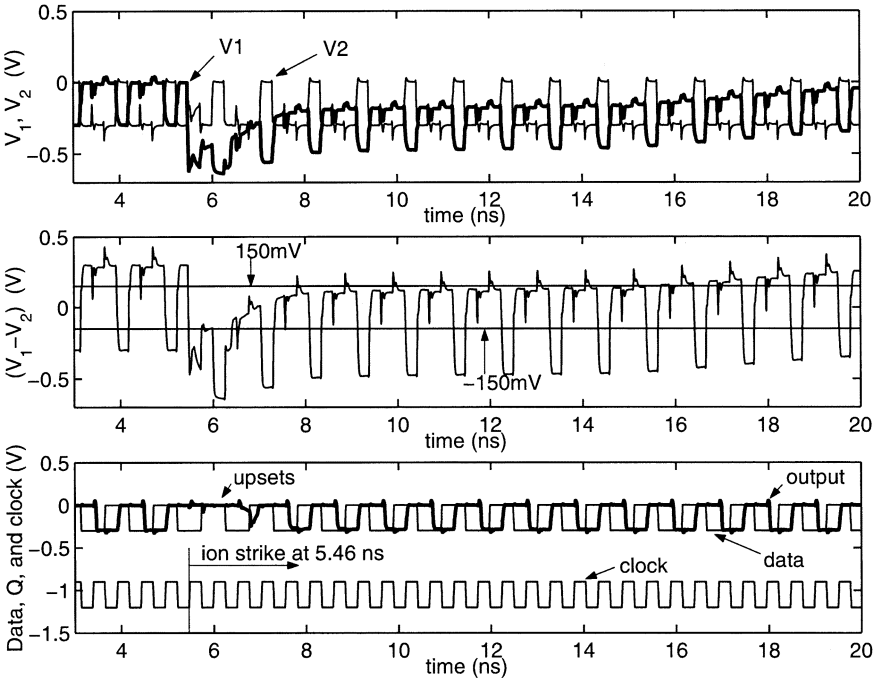

Fig. 14. Single-ended and differential output voltages for the NAND gate struck by heavy ion in circuit D (switch current is 0.5 mA).

seen in the new circuit, which is obtained by guidelines laid out in [3], further validates these earlier conclusions. Together, these results suggest a potential path for achieving sufficient SEU tolerance in high-speed SiGe HBT digital logic for many space applications. We plan to do a microbeam study on the circuits discussed in this paper in near future for experimental validation of the results.

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