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8.1 An Ultra-Low-Energy/Frame Multi-Standard JPEG Co-Processor in 65nm CMOS with Sub/Near-Threshold Power Supply

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Many digital ICs can benefit from sub/near threshold operations that provide ultra-low-energy/operation for long battery lifetime. In addition, sub/near threshold operation largely mitigates the transient current hence lowering the ground bounce noise. This also helps to improve the performance of sensitive analog circuits on the chip, such as delay-lock loops (DLL), which is crucial for the functioning of large digital circuits. However, aggressive voltage scaling causes throughput and reliability degradation. This paper presents SubJPEG, a state of the art multi-standard 65nm CMOS JPEG encoding co-processor that enables ultra-wide V_{DD} scaling. With a 0.45V power supply, it delivers 15fps 640×480 VGA application with only 1.3pJ/operation energy consumption per DCT and quantization computation. This co-processor is very suitable for applications such as digital cameras, portable wireless and medical imaging. To the best of our knowledge, this is the largest sub-threshold processor so far.

The architecture of SubJPEG is shown in Fig. 8.1.1. The design is fully compliant with the JPEG encoder baseline standard [1]. Asynchronous FIFOs (AFIFOs) are located at the front-end of the data-path to enable an flexible interface to standard bus interfaces such as PCI/PCI-X/PCI-Express. For each frame, the external main CPU issues a command to the configuration register file of the JPEG processor. The command includes the source data start address/length, destination data start address, YUV sampling ratio, programmable quantization table coefficients, etc. SubJPEG accommodates two command slots in the configuration register file so as to minimize the inter-frame configuration latency. The JPEG data-path has three main stages: (1) 2D-DCT transformation, (2) Quantization, and (3) Huffman encoding. A pair of DCT and Quantization modules is denoted as an "engine". SubJPEG has 4 engines in parallel in order to mitigate throughput degradation. It exploits 2 supply voltage domains and 3 frequency domains. The configuration and interface operate with *bus* clock and V_{DDH}, the Huffman encoder functions with *fast* clock and V_{DDH}, while the engines function with *slow* clock and V_{DDL}. However, to reduce the I/O pads of this DMA processor, logic has been added to multiplex certain I/O signals, so an additional V_{MUX} domain working under a *shift* clock is implemented. Signals across different clock domains utilize handshaking to increase robustness.

The V_T variation is the dominant component for sub-threshold current variation due to its exponential correlation to the current [2]. A novel configurable V_T balancer which uses only one bulk line to balance the V_T of PMOS and NMOS transistors has been shown in Fig 8.1.2. An off-chip capacitor is needed to mitigate ripple. Each engine has a deep N-well island and a dedicated V_T balancer located at its corner. When the engines are set in super-threshold mode, the tri-state buffer is configured to be in high impedance state. The bulk of the PMOS transistors is then configured to be connected to V_{DD}, and the bulk of the NMOS transistors is configured to be connected to G_{ND}. When the engines are configured to be in the sub/near threshold mode, the tri-state buffer starts to function. Any fluctuation of the signal V_{out}, which is generated from a process-corner V_T imbalance detector, is thus detected and amplified by the tri-state buffer. In this mode, the power switches are configured so that the buffer's output voltage directly supplies the bulk of all the logic gates of the engine. This output is also fed back to the bulk of the V_T balancing detector to force PMOS/NMOS V_T balancing. As the bulk controlling line is never higher than $|V_T|$, so the p-n junction diodes are prevented from turning on. The

power switch transistors S_0, S_1 and S_2 are designed with NMOS transistors with their gate control voltage boosted to 1.2V, which is the VDDIO for pads, so the driving capability is increased. The Monte-Carlo transient time simulation for a critical path at V_{DD}=0.4V shows that the standard deviation σ is reduced by 4.7× and the σ/μ is reduced by 3.6× when the configurable V_T balancer is used.

Our previous research has revealed that, V_T mismatch of paired transistors working in sub-threshold can be worse by a factor of two as compared to transistors working in the super-threshold region [3]. While V_T mismatch is always thought as notorious, an interesting observation is that the V_T mismatch between parallel transistors can be utilized to increase the sub/near threshold current drivability, as shown in Fig. 8.1.3. Therefore, wide sub-threshold power switches, such as S_5 and S_6 in the V_T balancer, are therefore preferably divided into narrow transistors. This is realized by utilizing a multiple-finger structured transistor. As a result, the drivability of power switches is significantly increased without increasing layout area.

A sub-threshold standard cell library has been developed to synthesize the engines. Compared to existing super-threshold libraries, in the sub-threshold library the standard cells are resized so as to pass Monte-Carlo simulation with high confidence. Besides, certain circuit structures are strictly prohibited, as illustrated in Fig. 8.1.4; cells with more than three parallel-transistors or more than three stacked transistors are avoided (only PMOS transistors are drawn for clarity). Also avoided are ratioed logic cells.

Also shown in Fig. 8.1.4 is the 2-stage level shift scheme used in subJPEG. The 1st stage level shifting is performed through simple buffers which are capable of pulling up signals from sub-threshold V_{DDL} to V_{DDH} (~ V_{DDL}+300mV). The 2nd stage level shifting is performed through feedback structured level-shifters from V_{DDH} to 1.2V I/O pad.

The chip is fabricated in a 65nm 7-layer standard V_T CMOS process. A micrograph of the chip is shown in Fig. 8.1.7. The core area is 1.4×1.4mm² without pads. Fig. 8.1.5 shows the waveforms of some control signals from the logic analyzer. Also shown is the measurement result for the V_T balancer. Measurements of energy and speed performance are summarized in Fig. 8.1.6.

References:
[1] Gregory K. Wallace, "The JPEG Still Picture Compression Standard," *IEEE Trans. Consumer Electronics*, vol. 38, issue 1, pp. xviii–xxxiv, February, 1992.
[2] Yu Pu, José Pineda de Gyvez, Henk Corporaal and Yajun Ha, "V_T Balancing and Device Sizing Towards High Yield of Sub-threshold Static Logic Gates," *IEEE International Symp. Low Power Electronics and Design (ISLPED)*, pp. 355-358, Aug. 2007.
[3] José Pineda de Gyvez ,and Hans P.Tuinhout, "Threshold Voltage Mismatch and Intra-Die Leakage Current in Digital CMOS Circuits," *IEEE J. Solid-State Circuits*, Vol. 39, No.1, pp. 157–168, Jan. 2004.
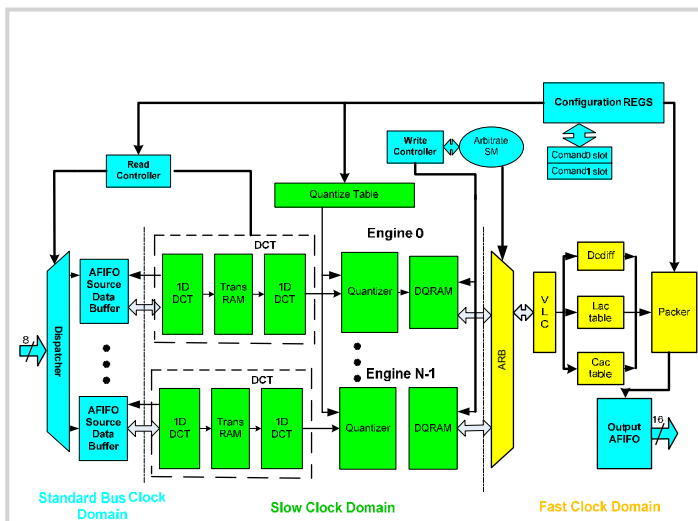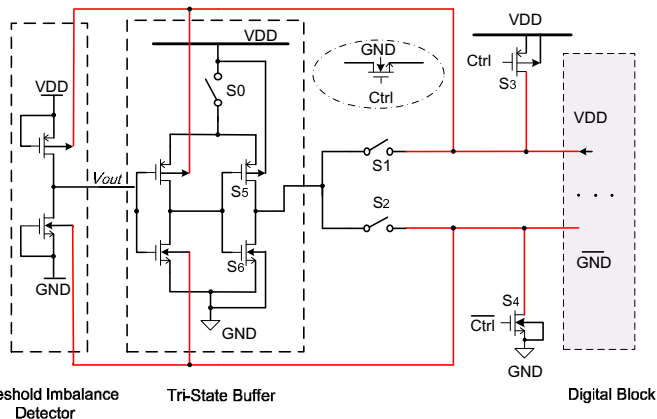
Figure 8.1.1: SubJPEG system block diagram.

Figure 8.1.2: Configurable V_T Balancer.

$$\sigma V_T = \frac{A_{\Delta V_T}}{\sqrt{WL}} \qquad \sigma V_{Tx} = \frac{\sqrt{N}\, A_{\Delta V_T}}{\sqrt{WL}}$$

$$\mu_{\text{Ieff}} = I_{0n} e^{\frac{(V_{GS}-\mu V_T + \eta V_{DS} - \gamma V_{SB})}{nU} + \frac{\sigma V_T^2}{2}} (1 - e^{\frac{V_{DS}}{U}}) \qquad \mu_{\text{Ieff}}' = \sum_{i=1}^{N} I_{\text{eff}\_i}$$

$$= I_{0n} e^{\frac{(V_{GS}-\mu V_T + \eta V_{DS} - \gamma V_{SB})}{nU} + \frac{\sigma V_{Tx}^2}{2}} (1 - e^{\frac{V_{DS}}{U}})$$

$$\sigma V_{Tx} > \sigma V_T \quad \Rightarrow \quad \mu_{\text{Ieff}}' > \mu_{\text{Ieff}}$$
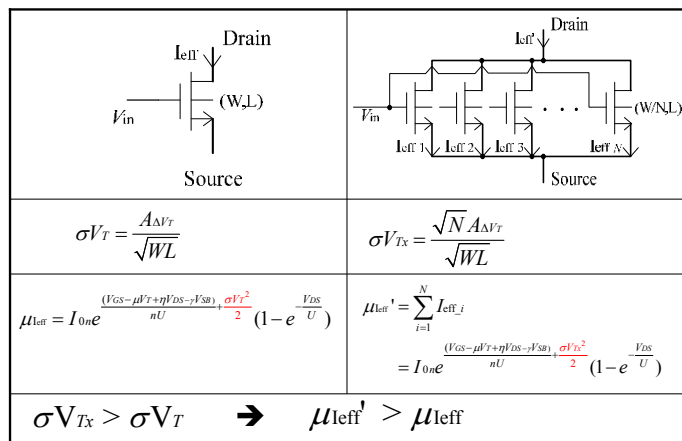
Figure 8.1.3: Improving sub-threshold drivability by exploiting V_T mismatch between parallel transistors.
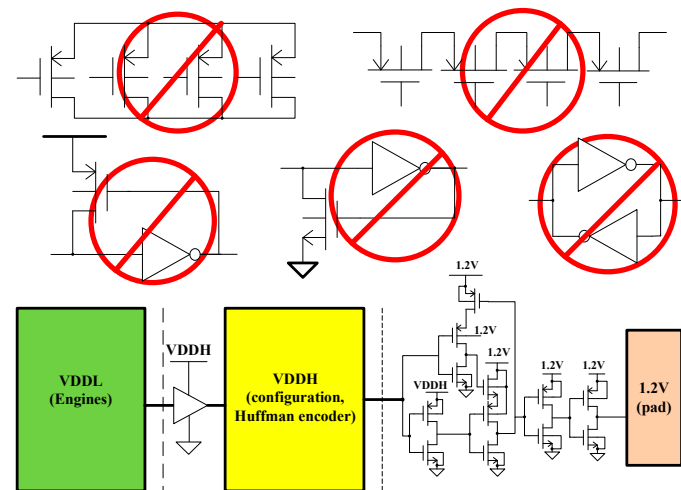

Figure 8.1.4: Illustration of prohibited structures in sub-threshold library and 2-stage level shift scheme.
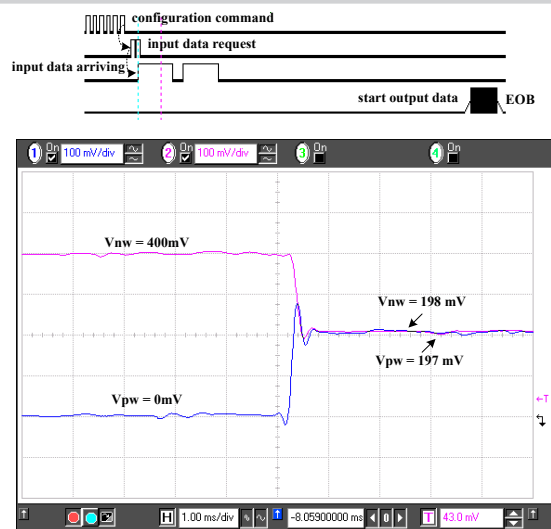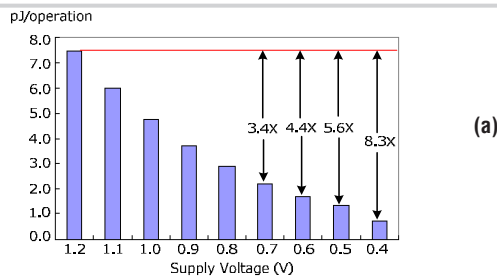

Figure 8.1.5: Waveforms from logic analyzer and V_T balancer measurements from oscilloscope.

Engine Mode	VDDL (V)	VDDH (V)	Throughput (MB)	Possible Applications
Sub-threshold	0.4	0.6	10 (2.5MHz clock)	digital still image
Near-threshold	0.45	0.7	18 (4.5MHz clock)	VGA (640×480,15fps)
	0.5	0.8	40 (10MHz clock)	VGA (640×480, 30fps)
Super-threshold	0.6	0.9	100 (25MHz clock)	SXGA(1280×1024,15fps)
	0.7	1.0	160 (40MHz clock)	UXGA(1600×1200, 15fps) QXGA(2048×1536, 15fps)

Figure 8.1.6: (a) Energy/operation for each engine, (b) Throughput for 4 engines and possible real-time image applications.
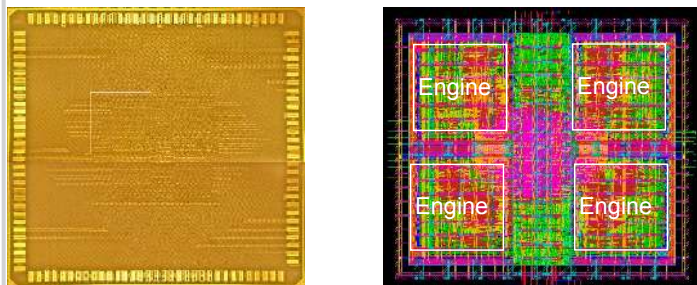
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Figure 8.1.7: Die micrograph and core layout of SubJPEG test chip in 65nm CMOS.