

# An Ultra-Low Phase Noise Class-F<sub>2</sub> CMOS Oscillator With 191 dBc/Hz FoM and Long-Term Reliability

Masoud Babaie, *Student Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

**Abstract**—In this paper, we propose a new class of operation of an RF oscillator that minimizes its phase noise. The main idea is to enforce a clipped voltage waveform around the LC tank by increasing the second-harmonic of fundamental oscillation voltage through an additional impedance peak, thus giving rise to a class-F<sub>2</sub> operation. As a result, the noise contribution of the tail current transistor on the total phase noise can be significantly decreased without sacrificing the oscillator's voltage and current efficiencies. Furthermore, its special impulse sensitivity function (ISF) reduces the phase sensitivity to thermal circuit noise. The prototype of the class-F<sub>2</sub> oscillator is implemented in standard TSMC 65 nm CMOS occupying 0.2 mm<sup>2</sup>. It draws 32–38 mA from 1.3 V supply. Its tuning range is 19% covering 7.2–8.8 GHz. It exhibits phase noise of –139 dBc/Hz at 3 MHz offset from 8.7 GHz carrier, translated to an average figure-of-merit of 191 dBc/Hz with less than 2 dB variation across the tuning range. The long term reliability is also investigated with estimated >10 year lifetime.

**Index Terms**—Class-F<sub>2</sub> oscillator, differential/common mode resonant frequencies, digitally controlled oscillator, impulse sensitivity function, oscillator reliability, phase noise, transformer, VCO.

## I. INTRODUCTION

SPECTRAL purity of RF LC-tank oscillators is typically addressed by improving a quality factor (Q) of its tank, lowering its noise factor (NF), and increasing its power consumption. Even though technology scaling increases the effective capacitance ratio,  $C_{\max}/C_{\min}$ , of switchable tuning capacitors and, consequently, the oscillator tuning range, it does not improve the oscillator's spectral purity parameters, such as tank Q-factor and oscillator NF. In fact, the tank Q-factor is slightly degraded in more advanced technologies mainly due to closer separation between the top-metal and lossy substrate as well as thinner lower-level metals that are used in metal-oxide-metal (MoM) capacitors. On the other hand, transistor excess noise factor,  $\gamma$ , thus oscillator NF, keeps on degrading, thus penalizing the oscillator phase noise (PN). Consequently, the oscil-

lators of excellent spectral purity and power efficiency are becoming more and more challenging as compared to other RF circuitry that is actually gaining from the technology scaling. This has motivated an intensive research leading to recently introduced new oscillator topologies [1]–[9].

In this paper, we specifically address the ultra-low phase noise design space while maintaining high power efficiency. We propose a soft-clipping class-F<sub>2</sub> oscillator topology based on enforcing a clipped voltage waveform around the LC tank by increasing the 2nd-harmonic of the fundamental oscillation voltage through an additional impedance peak [9]. This structure shifts the oscillation voltage level so that it provides enough headroom for the tail current without compromising the oscillating amplitude. Consequently, the phase noise contribution of the tail current transistor is effectively reduced while maintaining the oscillator voltage efficiency. Furthermore, the class-F<sub>2</sub> operation clips the oscillation waveform for almost half of the period, thus benefiting from the lower circuit-to-phase noise conversion during this time span.

The paper is organized as follows. The tradeoffs between the RF oscillator PN and power consumption are investigated in Section II. Section III establishes the environment to introduce the class-F<sub>2</sub> operation, its benefits, and constraints. The circuit-to-PN conversion mechanisms are studied in Section IV. Section V presents extensive experimental results. The oscillator longterm reliability is studied and quantified in Section VI.

## II. CHALLENGES IN ULTRA-LOW PHASE NOISE OSCILLATORS

The phase noise (PN) of the traditional oscillator (i.e., class-B) with an ideal current source at an offset frequency  $\Delta\omega$  from its fundamental frequency  $\omega_0$  could be expressed as

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left( \frac{KT}{2 Q_t^2 P_{DC}} \frac{1}{\alpha_I \alpha_V} (1 + \gamma) \left( \frac{\omega_0}{\Delta\omega} \right)^2 \right) \quad (1)$$

where  $Q_t$  is the tank quality factor,  $\alpha_I$  is the current efficiency, defined as the ratio of the fundamental current harmonic  $I_{\omega_0}$  over the oscillator DC current  $I_{DC}$ , and  $\alpha_V$  is the voltage efficiency, defined as the ratio of the oscillation amplitude  $V_{osc}$  (single-ended) over the supply voltage  $V_{DD}$ . The oscillator power consumption is

$$P_{DC} = \frac{V_{osc}^2}{\alpha_I \cdot \alpha_V \cdot R_{in}} \quad (2)$$

where  $R_{in}$  is an equivalent input parallel resistance of the tank modeling its losses. Equation (1) clearly demonstrates a tradeoff between power consumption and PN. To improve the oscillator PN, one must increase  $P_{DC}$  by scaling down  $R_{in}$ . This

Manuscript received March 12, 2014; revised September 27, 2014; accepted November 21, 2014. This paper was approved by Associate Editor Jacques Christophe Rudell. This work was supported in part by the European ERC Starting Grant 307624 TDRFSP.

M. Babaie is with Delft University of Technology, 2628 CD, Delft, The Netherlands (e-mail: m.masoud.babaie@ieee.org).

R. B. Staszewski was with Delft University of Technology, 2628 CD, Delft, The Netherlands. He is now with University College Dublin, Belfield, Dublin 4, Ireland (e-mail: bogdans@ieee.org).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2014.2379265

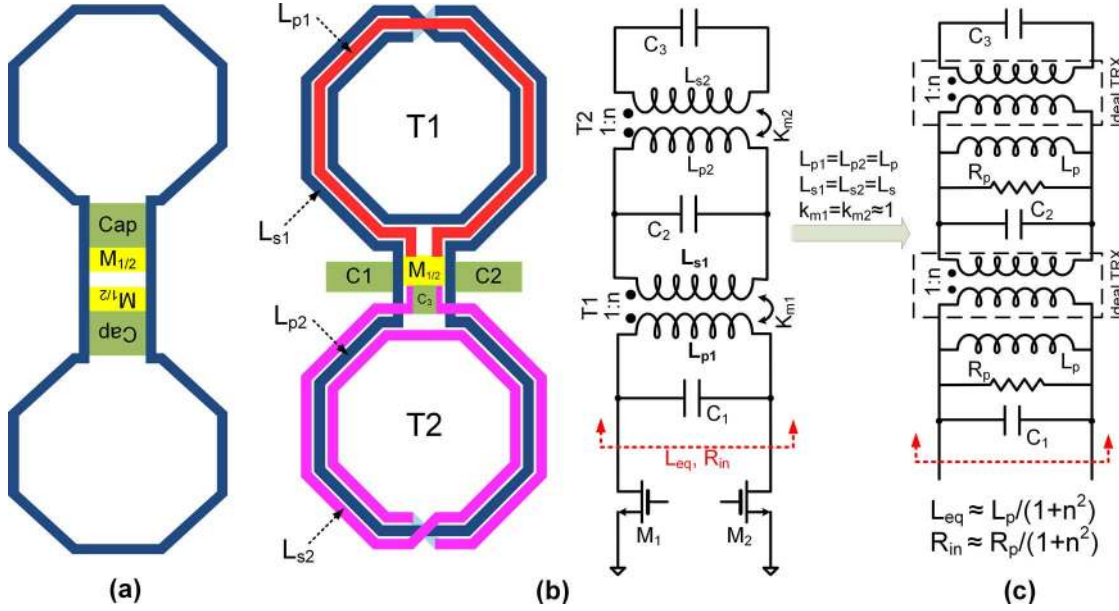


Fig. 1. Phase noise reduction techniques without sacrificing tank's  $Q$ -factor: (a) coupled oscillators, (b) connecting two step-up transformers back-to-back, and (c) its equivalent circuit model.

could be done by lowering the tank inductance while maintaining the optimal  $Q_t$ . For example, by continuing to reduce the inductance by half,  $R_{in}$  could theoretically decrease by half at the constant  $Q_t$ , which would improve phase noise by 3 dB with twice the power consumption at the same FoM.<sup>1</sup> However, at some point, the resistance of the tank's interconnections will start dominating the resonator losses and, consequently, the equivalent tank's  $Q$  will start decreasing. Hence, the PN-versus-power tradeoff will no longer be beneficial since the FoM will drop dramatically due to the  $Q$ -factor degradation.

Coupling  $N$  oscillators is an alternative way of trading off the power for PN since it avoids scaling the inductance down to impractically small values. It can theoretically improve PN by a factor of  $N$  compared with a single oscillator [10], [11]. Unfortunately, the oscillator size increases linearly, i.e.,  $4\times$  larger area for just 6 dB of PN improvement.

In this paper, we improve the phase noise by utilizing two  $1:n$  transformers that are connected back-to-back [9], as shown in Fig. 1(b) and (c). The equivalent  $R_{in}$  and, thus, the oscillator PN are scaled down by a factor of  $\sim(1+n^2)$  without sacrificing tank's  $Q$ -factor. Hence, PN improvement can potentially be much better than with the coupled oscillators [e.g., Fig. 1(a)] at the same die area. In addition, the  $C_2$  and  $C_3$  tuning capacitors, which are not directly connected to the primary of the first transformer, appear at the input of the transformer network via the scaling factor of  $n^2$  and  $n^4$  as can be realized from Fig. 1(c). This impedance transformation results in a significant reduction in the required value of all the capacitors (i.e.,  $\sum_i C_i$ ), which reduces the routing parasitics (both inductive and capacitive), and improves the tuning range and PN of the oscillator. Even though by increasing the transformer's turns ratio the tank input impedance will be reduced, the transformer  $Q$ -factor will not stay at the optimum level and will start dropping at some point

[12]. It turns out that the turns ratio of  $n = 2$  can satisfy the aforementioned constraints altogether.

To sustain the oscillation of this differential tank, two transistors shall be added. Fig. 2 illustrates the *preliminary* schematic and waveforms. Unfortunately, as gathered from Fig. 3, this structure suffers the same issues as the traditional class-B oscillator when the ideal current source is replaced with a tail bias transistor,  $M_T$ . The PN is ideally improved by 20 dB/dec through increasing the oscillation amplitude, provided the gm-devices  $M_{1,2}$  operate in saturation over the entire period. However, the slope of PN improvement deviates from the ideal case when  $M_{1,2}$  enter the triode region for a part of the oscillation period [2]. This problem is intensified especially when the oscillator operates at higher frequencies and larger  $I_{DC}$  (i.e.,  $\geq 10$  mA) is needed to satisfy the stringent spectral purity of the GSM standard [6]. Actually, the combination of the parasitic drain capacitance of the large-size  $M_T$  with the entering the triode region by  $M_{1,2}$ , will cyclically short-circuit the tank, thus degrading its equivalent  $Q$ -factor and oscillator PN [13].

Furthermore, the oscillation voltage should provide minimum  $V_{DSAT}$  across  $M_T$  throughout the entire period to keep it in saturation. Consequently,  $\alpha_V$  becomes substantially less than 1, which translates to a significant PN penalty as clearly seen from (1). Larger  $M_T$  needs lower  $V_{DSAT}$ , which would increase  $\alpha_V$ . However, the tail transistor's effective thermal noise will increase significantly for the same  $I_{DC}$  [14]. As a consequence, the contribution of  $M_T$  to the PN could be larger than that of gm-devices, which translates to a significant increase of the oscillator NF and thus its PN [6]. In addition, the  $M_T$  parasitic capacitance  $C_T$  will also increase with the side effect of a stronger tank loading. On the other hand, the combination of the sinusoidal drain voltage, large  $C_T$ , and the entering of triode region by  $M_{1,2}$  will result in a dimple in the squarish shape of active device drain current (see Fig. 2) with a 10%–20% reduction in

<sup>1</sup>FoM =  $|PN| + 20 \log_{10}(\omega_0/\Delta\omega) - 10 \log_{10}(P_{DC}/1 \text{ mW})$

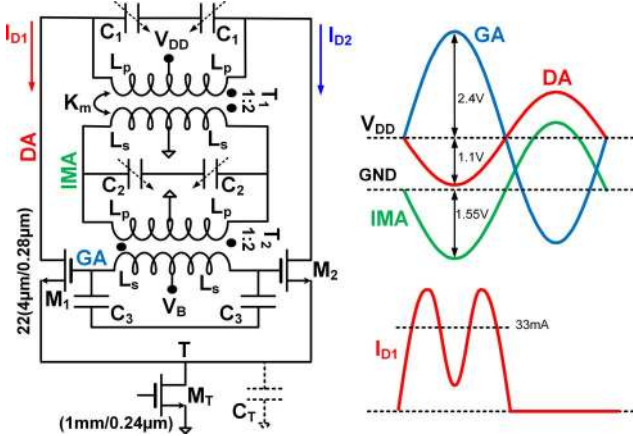


Fig. 2. Preliminary oscillator schematic and its simulated voltage and estimated current waveforms at  $f_0 = 8$  GHz,  $V_{DD} = 1.2$  V,  $I_{DC} = 33$  mA,  $L_{eq} = 80$  pH, and  $C_{eq} = 4.95$  pF.

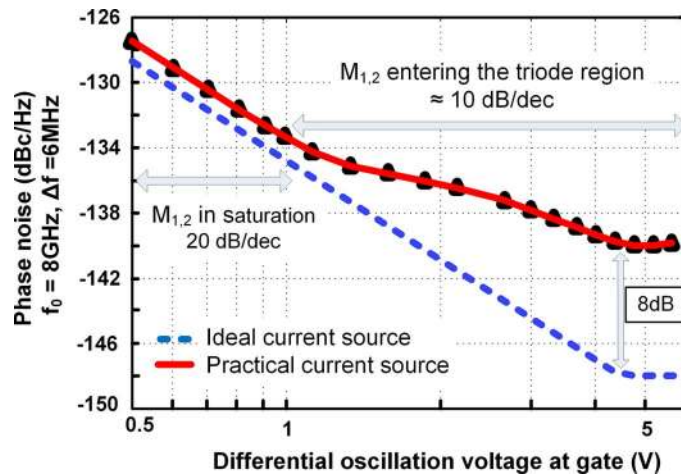


Fig. 3. Simulated phase noise performance of the preliminary oscillator of Fig. 2 versus gate differential oscillation voltage for the ideal and real current sources.

$\alpha_I$ , and thus FoM of the oscillator [1], [6]. All of the above reasons contribute to reducing the rate of PN improvement versus  $V_{osc}$  to about 10 dB/dec when  $M_{1,2}$  enter the triode region for a part of the oscillation period. Hence, a huge 8 dB PN difference in Fig. 3 is observed between the ideal and real operation of the oscillator. Consequently, the proposed oscillator must not be sensitive to the excess gm-device noise in the triode intervals. It should also break the tradeoff between  $\alpha_V$  and NF.

### III. EVOLUTION TOWARDS CLASS-F<sub>2</sub> OPERATION

Before introducing our proposed PN reduction technique, let us take a closer look at the harmonic component of the drain current  $I_D$  of the  $M_1$  and  $M_2$  gm-devices in Fig. 2. Ideally,  $I_D$  is a square wave containing fundamental and odd harmonics. The odd harmonics through  $M_1$  and  $M_2$  are 180° mutually out-of-phase and appear as differential-mode (DM) input signals for the tank. The  $I_D$  also contains even harmonics due to the large oscillation voltage, non-linearity of  $M_{1,2}$  and large parasitic capacitance of  $M_T$ . However, the even harmonics through  $M_1$  and  $M_2$  are mutually in-phase with  $\pm 90^\circ$  phase shift to their related odd

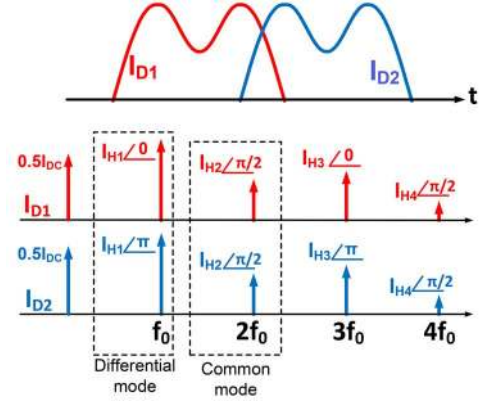


Fig. 4. Drain current of  $M_{1,2}$  devices of Fig. 2 in time and frequency domains.

harmonics, as shown in Fig. 4. Consequently, these even harmonics appear as a common-mode (CM) input for the tank. The conventional tank input impedance has only one peak at the fundamental frequency  $\omega_0$ . Therefore, the tank filters out the drain current harmonics and ultimately a sinusoidal voltage is seen across the tank. Now, suppose the tank offers an additional CM input impedance peak around the second harmonic (see Fig. 5). Then, the second harmonic of  $I_D$  is multiplied by the tank's CM input impedance to produce a sinusoidal voltage at  $2\omega_0$  that is in quadrature to the fundamental oscillation voltage produced by the tank's DM impedance at  $\omega_0$ . The combination of both waveforms creates the desired oscillation voltage around the tank, as shown in Fig. 5, thus justifying the class-F<sub>2</sub> designation

$$V_{DA} = V_{DD} - V_{H1} \sin(\omega_0 t) - V_{H2} \sin\left(2\omega_0 t + \frac{\pi}{2}\right). \quad (3)$$

$\zeta_V$  is defined as the ratio of the second-to-first harmonic components of the oscillation voltage

$$\zeta_V = \frac{V_{H2}}{V_{H1}} = \left(\frac{R_{CM}}{R_{in}}\right) \left(\frac{I_{H2}}{I_{H1}}\right) \quad (4)$$

where  $R_{in}$  and  $R_{CM}$  are, respectively, the tank DM and CM impedance magnitude at  $\omega_0$  and  $2\omega_0$ . Fig. 6 illustrates the oscillation voltage and its related impulse sensitivity function (ISF) based on [15, eq. (38)] for different  $\zeta_V$  values. Clearly,  $\zeta_V$  should be 0.3 to have the widest flat span in the tank's oscillation voltage. The  $\Gamma_{rms}^2$  is 0.35 for  $\zeta_V = 0.3$  compared with 0.5 for the traditional oscillator, which leads to a 1.5 dB PN and FoM improvements. Furthermore, ISF is negligible when the gm-devices work in the triode region and inject the most thermal noise into the tank. Consequently, the oscillator FoM improvement should be larger than that predicted by just the ISF<sub>rms</sub> reduction. More benefits of the class-F<sub>2</sub> operation will be revealed in the following sections.

The argument related to Fig. 5 suggests the creation of an additional CM input impedance peak at the second harmonic of main differential resonance. Incidentally, the proposed step-up 1:2 transformer acts differently to the CM and DM input signals. Fig. 7(a) illustrates the induced current at the transformer's secondary when the primary winding is excited by a differential signal. All induced currents circulate in the same direction at the transformer's secondary to satisfy Lenz's Law. Consequently, the induced currents add constructively, which leads



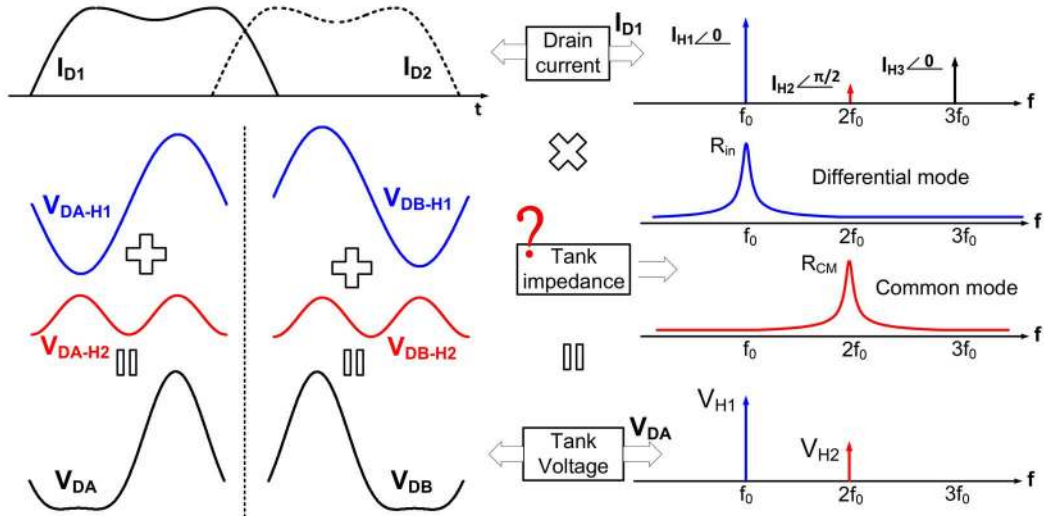


Fig. 5. Proposed oscillator waveforms in time and frequency domains.

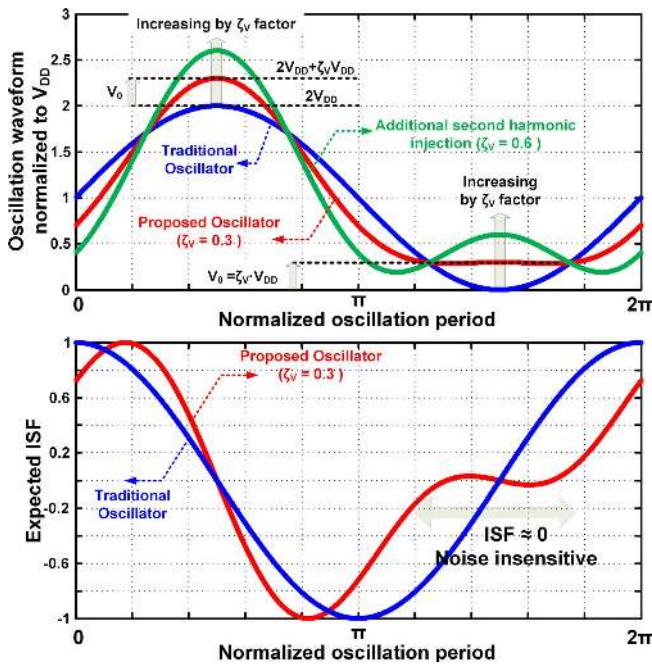


Fig. 6. Top: effect of adding second harmonic in the oscillation voltage waveform. Bottom: its expected ISF based on [15, eq. (38)].

to a strong inter-winding coupling factor ( $k_m \geq 0.7$ ). However, when the transformer's primary is excited by a CM signal [Fig. 7(b)], the induced currents at the right-hand and left-hand halves of the transformer's secondary winding circulate in opposite directions thus largely canceling each other. The residual current results in a very small  $k_m \leq 0.2$  for the CM excitation. Consequently, the concept of using two modes of a transformer for waveform shaping (proposed in [16] for a power amplifier) will be adopted here to realize the special tank input impedance of Fig. 5. Note that an equivalent lumped-element model in [12], [17] cannot simultaneously cover both CM and DM types of behavior and would produce wrong results. Hence, we suggest to utilize the transformer's  $S$ -parameters and PSS analysis to simulate the proposed class- $F_2$  oscillator.

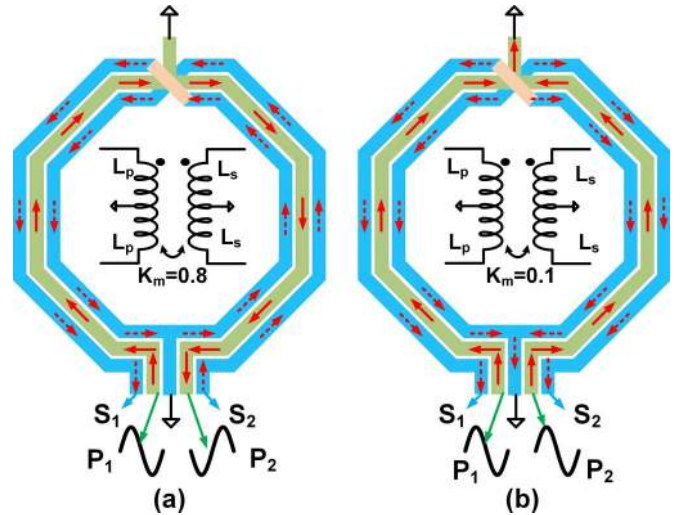


Fig. 7. Transformer behavior in (a) differential-mode and (b) common-mode excitations.

Fig. 8 shows the proposed tank of a class- $F_2$  oscillator. The  $C_{1d}$  and  $C_3$  are intentionally chosen as fixed capacitors while the DM and CM resonant frequencies are tuned by  $C_{1c}$  (fine) and  $C_2$  (coarse). The DM main resonant frequency is

$$f_{1d} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \approx \frac{1}{2\pi\sqrt{\left(\frac{L_p}{1+n^2}\right)(C_{1c} + C_{1d} + C_2n^2 + C_3n^4)}}. \quad (5)$$

The inductance reduction and capacitance multiplication factors of the dual-transformer tank are directly contained in (5). The CM input signal can neither see the second transformer nor  $C_2$  &  $C_3$  due to negligible  $k_{m(CM)}$ . In addition, differential capacitors also act as open circuit for the CM signals. Consequently, the tank's CM resonant frequency is

$$f_{1c} = \frac{1}{2\pi\sqrt{L_{cm}C_{1c}}} \approx \frac{1}{2\pi\sqrt{(L_p + 2L_{par})C_{1c}}}. \quad (6)$$

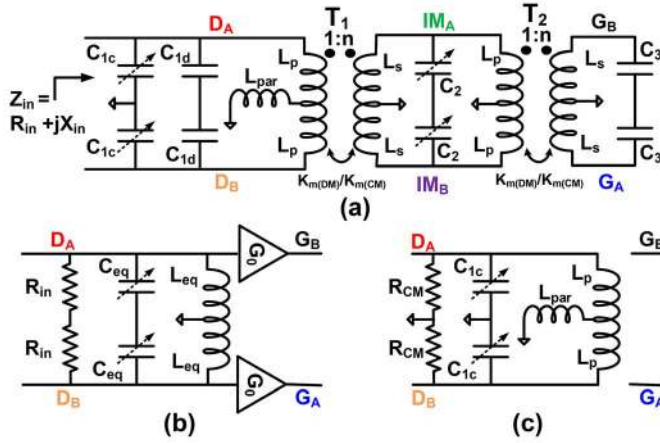


Fig. 8. Proposed transformer-based resonator: (a) schematic, (b) its simplified equivalent differential-mode circuit ( $k_{m(DM)} \approx 1$ ), (c) simplified tank schematic for common-mode input signals ( $k_{m(CM)} \approx 0$ ).

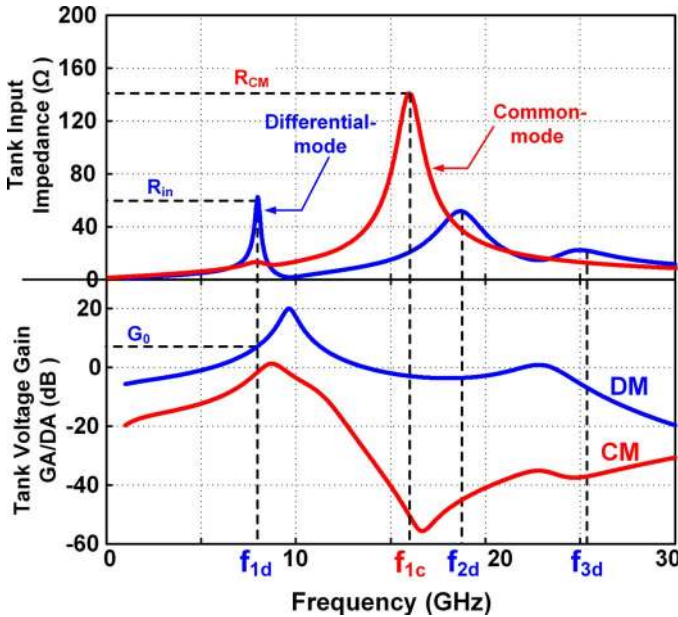


Fig. 9. Simulated characteristics of the transformer-based tank of Fig. 8. Top: magnitude of input impedance  $Z_{in}$ . Bottom: tank voltage gain between gate and drain of core devices.

There is no tank impedance scaling for the CM excitation. Hence, the CM input impedance peak should be higher than the DM peak, as clearly seen from Fig. 9 (top). To operate properly, CM-to-DM resonance ratio must be adjusted to 2 as follows:

$$\begin{aligned} \zeta_f &= \frac{f_{1c}}{f_{1d}} \\ &= \sqrt{\frac{L_p}{L_p + 2L_{par}} \cdot \frac{C_{1c} + C_{1d} + C_2 n^2 + C_3 n^4}{C_{1c} (1 + n^2)}} \\ &= 2. \end{aligned} \quad (7)$$

As a consequence, the frequency tuning requires a bit different consideration than in the class-B oscillators. Both  $C_{1c}$  and  $C_2$  must, at least at the coarse level, be changed simultaneously to satisfy (7) such that  $f_{1c}$  coincides with  $2f_{1d}$ . This

adjustment is entirely a function of the ratio of the tuning capacitors, which is precise thus making  $\zeta_f$  largely independent from process, voltage and temperature (PVT) variations.

Let us now consider the required accuracy of this ratio  $\zeta_f$ . The transformer and switching capacitors are designed based on maximum Q-factor at the operating frequency  $f_{1d}$ . The tank Q-factor drops at least  $3 \times$  at  $f_{1c} = 2f_{1d}$ . Consequently, the tank CM impedance bandwidth is very wide, as seen in Fig. 9. Therefore, the oscillator is less sensitive to the position of  $f_{1c}$  and thus the tuning capacitance ratio. A realistic 5% error in  $\zeta_f$  has no significant adverse effects on the oscillator waveform and thus its PN.

The schematic and waveforms of the proposed oscillator are shown in Figs. 10 and 11. Even though the second-harmonic injection reduces the drain oscillation voltage by  $V_0$  during the clipping interval, it increases its positive peak by  $V_0$  [see Fig. 6(a)]. It means the drain oscillation span is shifted from 0-to- $2V_{DD}$  in the traditional oscillator to  $V_0$ -to- $(-2V_{DD} + V_0)$  in the proposed class-F<sub>2</sub> operation. Hence, the larger current source voltage headroom and lower noise factor are achieved without compromising the oscillation amplitude. Furthermore, the  $V_0$  headroom also reduces the dimple in the core-device drain current (compare Figs. 2 and 11), which helps the class-F<sub>2</sub> current efficiency to be closer to the ideal value of  $2/\pi$ .

Fig. 9 illustrates the tank CM/DM input impedance and passive voltage gain between the gate and drain of  $M_{1,2}$  versus frequency. Unfortunately, the tank exhibits two other undesired DM resonant frequencies ( $f_{2d}$ ,  $f_{3d}$ ) due to imperfect  $k_m$  of the two transformers that create two leakage inductances [12]. Consequently, the circuit loop must guarantee the oscillation only at the desired DM resonance,  $f_{1d}$ . Although CM demonstrates much larger input impedance peak, the two transformers effectively reject (attenuate by  $> 40$  dB) the CM signals. The root-locus plot in Fig. 12 illustrates the DM pole movements toward zeros for different oscillator loop trans-conductance gains  $G_M$ . The first and third frequency conjugate pole pairs ( $\omega_{1d}$ ,  $\omega_{3d}$ ) move into the right-hand plane with increasing the absolute value of  $G_M$ , while the second conjugate pole  $\omega_{2d}$  is pushed far away from the imaginary axis. This guarantees that the oscillation will not happen at  $\omega_{2d}$ . Furthermore, it can be shown that  $\omega_{3d}$  poles move to much higher frequencies with much lower input impedance peak and tank voltage gain if enough differential capacitance is located at  $T_1$  primary windings. It justifies the existence of the non-switchable differential capacitor  $C_{1d}$ . Consequently, the loop gain will not be enough to satisfy the Barkhausen criterion for  $\omega_{3d}$ .

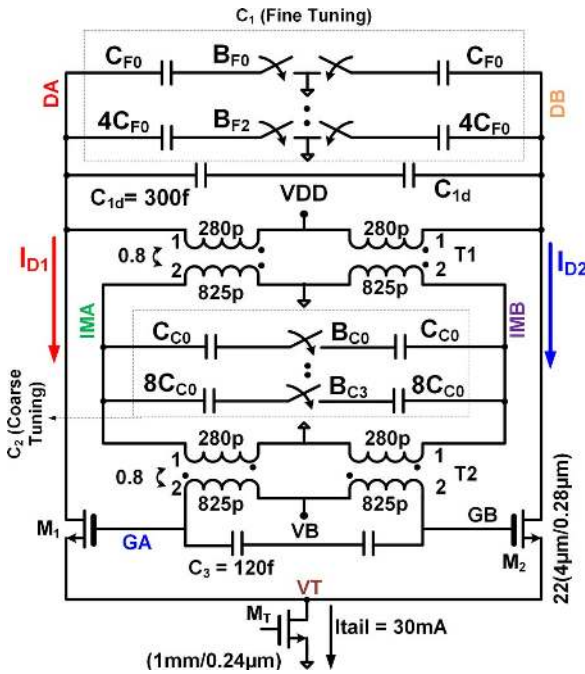
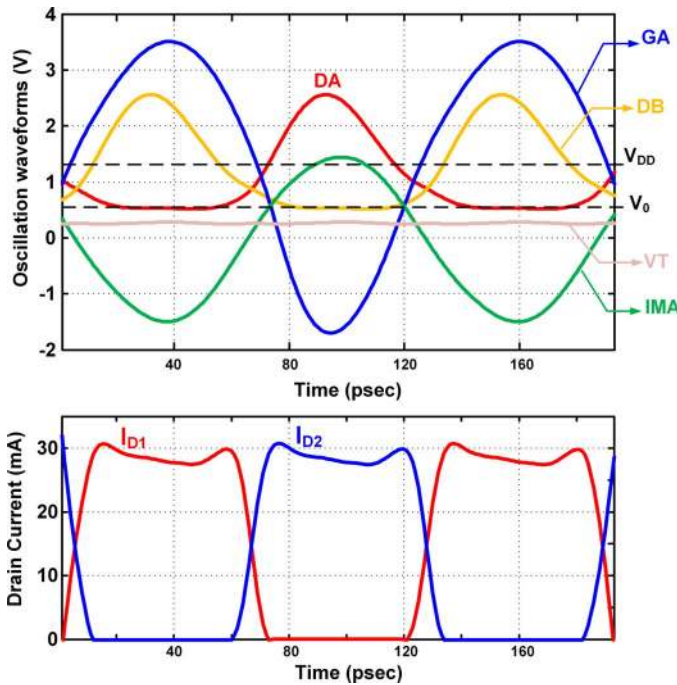
#### IV. PHASE NOISE MECHANISM IN CLASS-F<sub>2</sub> OSCILLATOR

According to the linear time-variant (LTV) model [15], the phase noise of an oscillator at an angular offset frequency  $\Delta\omega$  from its fundamental frequency  $\omega_0$  is expressed as

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left( \frac{\sum_i N_{L,i}}{2 q_{max}^2 (\Delta\omega)^2} \right) \quad (8)$$

where  $q_{max} = C_{eq} \cdot V_{osc}$  is the maximum charge displacement across the tuning capacitors and  $V_{osc} = \alpha_I \cdot R_{in} \cdot I_{DC}$  is the single-ended oscillation amplitude at the drain of gm-devices.

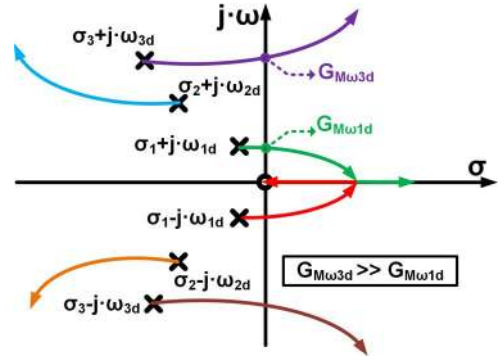



 Fig. 10. Proposed transformer-based class- $F_2$  oscillator schematic.

 Fig. 11. Simulated oscillation waveforms of the class- $F_2$  oscillator at  $V_{DD} = 1.2$  V and  $I_{DC} = 29$  mA. Top: oscillation voltage of different circuit nodes. Bottom: core transistors drain current.

The  $N_{L,i}$  in (8) is the effective noise power produced by the  $i$ th device given by

$$N_{L,i} = \frac{1}{2\pi} \int_0^{2\pi} \Gamma_i^2(\omega_0 t) \overline{i_{n,i}^2(\omega_0 t)} d(\omega_0 t) \quad (9)$$

where  $\overline{i_{n,i}^2}$  is the white noise current density of the  $i$ th noise source,  $\Gamma_i$  is its corresponding ISF function. Obtaining the ISF


 Fig. 12. Root-locus plot of the class- $F_2$  oscillator.

of various oscillator nodes is the first step in calculating the oscillator's PN. The ISF functions are simulated by injecting a 20 femto-coulomb charge ( $\Delta q$ ) throughout the oscillation period and measuring the resulting time shifts  $\Delta t_i$ , yielding

$$\Gamma_i = \omega_0 \cdot \Delta t_i \cdot \frac{q_{\max}}{\Delta q}. \quad (10)$$

Fig. 13(a) illustrates the ISF of various tank nodes. The soft clipping reduces by 30% the effect of losses on the oscillator PN due to single-ended switchable  $C_{1c}^2$  and  $T_1$  primary windings. However, ISF functions of the  $T_1$  secondary and  $T_2$  primary/secondary winding noise sources (including  $C_2$  and  $C_3$ ) are not improved due to the sinusoidal (i.e., conventional) waveforms at  $IM_{A,B}$  and  $GA,B$  nodes. Fig. 13(a) indicates that  $G_{A,B}$  are the most sensitive nodes. Hence,  $C_3$  is constructed as a fixed MoM capacitor and the transformer was designed with a goal of maximizing Q-factor of the secondary winding.

To calculate a closed-form PN equation, the proposed oscillator model is simplified in Fig. 14. The  $G_{DS1,2}(t)$  represent the channel conductance of  $M_{1,2}$ . The  $G_{M1,2}(t)$  and  $G_{MT}(t)$  model the transconductance gain of  $M_{1,2}$  and  $M_T$ , respectively. The original tank is pruned to a parallel  $L_{eq}$ ,  $C_{eq}$ ,  $R_{in}$  with noiseless voltage gain of  $G_0$  (see Fig. 8(b)). The simplified tank's equivalent ISF can be roughly estimated by an average of the tank's contributing ISF functions of Fig. 13(a) and is shown in Fig. 13(b) as green curve. The effective noise power of the tank is illustrated in Fig. 13(c) as green curve and its average power is approximated by

$$N_{\text{Tank}} = \frac{1}{\pi} \int_0^{2\pi} \frac{4KT}{R_{in}} \Gamma_{\text{tank}}^2(\omega_0 t) d(\omega_0 t) \approx 0.8 \frac{KT}{R_{in}}. \quad (11)$$

Consequently, the soft clipping reduces  $N_{\text{Tank}}$  by 20% compared to the traditional oscillator.

The effects of noise on the oscillator PN due to channel conductance ( $G_{DS}$ ) and transconductance gain ( $G_M$ ) of  $M_{1,2}$  transistors are separately investigated. Fig. 13(d) illustrates various operational regions of  $M_{1,2}$  across the oscillation period. When  $M_{1,2}$  are not turned off, they work mainly in the deep triode region where they exhibit a few ohms of channel resistance, as indicated in Fig. 13(e). Consequently, the combination of the

<sup>2</sup>The single-ended switchable capacitor is used to adjust the CM resonant frequency. However, its Q-factor is almost half that of the differential structure for the same  $C_{\max}/C_{\min}$ . The soft clipping largely compensates the effect of additional losses due to its lower  $\Gamma_{\text{rms}}$  value.

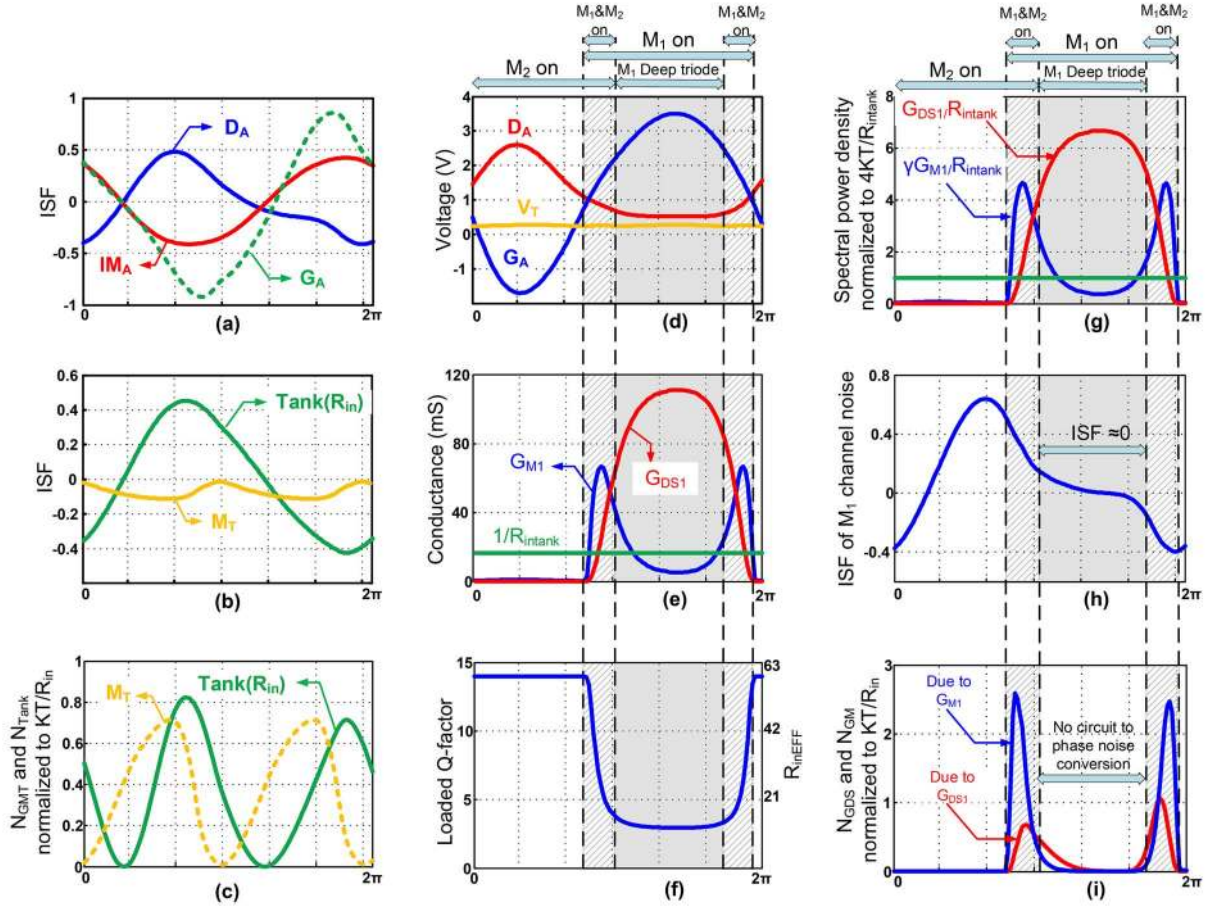


Fig. 13. Mechanisms of circuit-to-phase noise conversion across the oscillation period in the class-F<sub>2</sub> oscillator. (a) Simulated ISF of different tank nodes. (b) Equivalent ISF in the simplified oscillator schematic of Fig. 14. (c) Simulated effective power spectral density of the oscillator's noise sources normalized to  $KT/R_{in}$ . (d) Oscillation waveforms and operation region of  $M_{1,2}$ . (e) Transconductance and channel conductance of  $M_1$ . (f) Loaded Q-factor and effective parallel input resistance of the tank. (g) Power spectral density of  $M_1$  noise sources normalized to  $4KT/R_{intank}$ . (h) Simulated ISF function of  $M_1$  channel noise. (i) Simulated effective power spectral density of different noise sources of  $M_1$  normalized to  $KT/R_{in}$ .

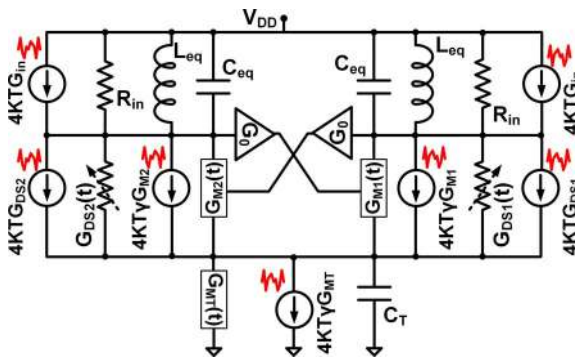


Fig. 14. Simplified noise source model of the class-F<sub>2</sub> oscillator.

large parasitic capacitance of  $M_T$  with low channel resistance of  $M_{1,2}$  in this deep triode region makes a low impedance path between the tank and ground. The literature interprets this as the tank loading event and defines implicit parameters such as *effective* tank Q-factor ( $Q_{eff}$ ) and input parallel resistance ( $R_{ineff}$ ) to justify the oscillator phase noise degradation due to this phenomenon. As shown in Fig. 13(f), the tank  $Q_{eff}$  and  $R_{ineff}$  drop 4–5 $\times$  when  $M_{1,2}$  operate in the deep triode. These “effective”

parameters merely indicate that more noise is injected then into the tank. However, they do not ordain how much of that circuit noise converts to phase noise, especially when the drain oscillation wave is not conventionally sinusoidal.

The proper approach should be based on the channel conductance noise power *and* its related ISF. If we had an ideal current source,  $M_{1,2}$  noise would be injected to the tank only during the commuting time (hachure areas in Fig. 13(e-g)). At the remaining part of oscillation period, one transistor is off and other one is degenerated by the ideal current source and thus noiseless. However, the output impedance of a practical current source is low for such a high  $I_{DC} = 30$  mA and  $f_0 = 8$  GHz. Consequently,  $M_{1,2}$  can inject significant amount of noise to the tank when they operate in deep triode region outside the commuting time (i.e., gray area in Fig. 13(g)). Note that gm-devices generate  $\sim 7\times$  higher amount of noise compared to the tank loss in the gray area, which can potentially increase the phase noise of the oscillator. However, the ISF of channel noise of  $M_{1,2}$  is very small in that time span as shown in Fig. 13(h). Hence, the excessive transistor channel noise (or excessive loaded tank noise of the conventional approach) cannot convert to phase noise. Consequently, the effective noise power of the gm-device

TABLE I  
COMPARISON BETWEEN THE RESULTS OF SPECTRERF PSS, PNOISE SIMULATION AND THEORETICAL EQUATIONS AT 8 GHz CARRIER FOR  $V_{DD} = 1.2$  V,  
 $R_{in} = 60 \Omega$ ,  $L_{eq} = 80$  pH,  $\gamma_{MT} = 1.3$  AND  $\gamma_{M1,2} = 1$

	Theoretical equations		SpectreRF simulation	
	Value	Share	Value	Share
$N_{Tank}$	$5.50 \cdot 10^{-23}$ V <sup>2</sup> /Hz	31%	$4.71 \cdot 10^{-23}$ V <sup>2</sup> /Hz	28.4%
$N_{M1,2} = N_{GDS} + N_{GMT}$	$8.63 \cdot 10^{-23}$ V <sup>2</sup> /Hz	48.8%	$8.78 \cdot 10^{-23}$ V <sup>2</sup> /Hz	53%
$N_{MT}$	$3.59 \cdot 10^{-23}$ V <sup>2</sup> /Hz	20.2%	$3.08 \cdot 10^{-23}$ V <sup>2</sup> /Hz	18.6%
$N_{Total} = N_{Tank} + N_{M1,2} + N_{MT}$	$17.72 \cdot 10^{-23}$ V <sup>2</sup> /Hz	100%	$16.57 \cdot 10^{-23}$ V <sup>2</sup> /Hz	100%
$q_{max}$ (coulombs)	$5.34 \cdot 10^{-12}$		$5.34 \cdot 10^{-12}$	
Phase noise @10MHz	-151dBc/Hz		-151.33dBc/Hz	

channel conductance is negligible, as illustrated in Fig. 13(i), and its average power is approximated by

$$N_{GDS} = \frac{1}{\pi} \int_0^{2\pi} 4KT G_{DS1}(\omega_0 t) \cdot \Gamma_{M1}^2(\omega_0 t) \cdot d(\omega_0 t) \approx \frac{KT}{R_{in}} \cdot (0.25). \quad (12)$$

Note that  $N_{GDS}$  is at least  $4 \times$  larger for the traditional oscillator, especially when a large  $\alpha_V$  is needed [18].

Fig. 13(e) shows  $M_1$  transconductance gain  $G_{M1}$  across the oscillation period. To sustain the oscillation, the combination of the transformers' passive voltage gain ( $G_0$ ) and effective negative transconductance of the gm-devices needs to overcome the tank and  $M_{1,2}$  channel resistance losses. Consequently

$$G_{M1EF} = \frac{1}{G_0} \cdot \left( \frac{1}{R_{in}} + G_{DS1EF} \right) \quad (13)$$

where  $G_{DS1EF}$  describes the effective value of the instantaneous conductance  $G_{DS1}(t)$  of  $M_{1,2}$  [18]. It can be shown that  $G_{DS1EF}$  could be as large as  $1/R_{in}$  when the oscillator is biased near the voltage limited region [1]. Therefore, the effective noise due to  $G_M$  of core transistors can be calculated by

$$N_{GM} = \frac{1}{\pi} \int_0^{2\pi} 4KT \gamma_{M1} G_{M1}(\omega_0 t) \cdot \Gamma_{M1}^2(\omega_0 t) \cdot d(\omega_0 t) \approx \frac{KT}{R_{in}} \frac{\gamma_{M1}}{G_0} \cdot (1 + R_{in} \cdot G_{DS1EF}) \approx \frac{KT}{R_{in}} \cdot \left( \frac{2\gamma_{M1}}{G_0} \right). \quad (14)$$

Equation (14) indicates that the second-harmonic injection (i.e., class-F<sub>2</sub> operation) demonstrates no benefit for  $N_{GM}$  but the transformers' voltage gain still offers significant benefits.

To estimate the PN contribution of  $M_T$ , its transconductance should be calculated first.

$$G_{MT} = \frac{2I_{DC}}{V_{gs(M_T)} - V_{th}} \approx \frac{2I_{DC}}{V_T} \quad (15)$$

where  $V_T$  is the overdrive voltage of  $M_T$  equal to the drain-source voltage. The clipping voltage level is

$$V_0 = V_{DD} [1 - \alpha_V (1 - \zeta_V)]. \quad (16)$$

By dedicating a half of  $V_0$  headroom to  $M_T$ , we obtain

$$G_{MT} = \frac{4I_{DC}}{V_0} \approx \frac{4I_{DC}}{V_{DD} (1 - \alpha_V (1 - \zeta_V))}. \quad (17)$$

By substituting  $I_{DC}$  with  $V_{osc}/(\alpha_I R_{in})$  in (17), we obtain

$$G_{MT} = \frac{4}{(1 - \alpha_V (1 - \zeta_V)) R_{in} \alpha_I} \left( \frac{V_{osc}}{V_{DD}} \right) = \frac{1}{R_{in}} \frac{4\alpha_V}{(1 - \alpha_V (1 - \zeta_V)) \alpha_I}. \quad (18)$$

As discussed earlier,  $\alpha_I$  and  $\alpha_V$  could be as large as 0.6 and 0.9 in the proposed oscillator, and optimum  $\zeta_V$  is about 0.3. Hence, (18) is simplified to  $G_{MT} \approx 15/R_{in}$ . As revealed by Fig. 13(b, orange),  $\Gamma_{MT,rms}$  is only 0.08 due to relatively large  $V_T$  of the class-F<sub>2</sub> operation. Consequently

$$N_{MT} = \frac{1}{2\pi} \int_0^{2\pi} 4KT \gamma_{MT} G_{MT}(\omega_0 t) \cdot \Gamma_{MT}^2(\omega_0 t) \cdot d(\omega_0 t) \approx \frac{KT}{R_{in}} \cdot (0.4\gamma_{MT}). \quad (19)$$

The contribution of  $M_T$  to the PN is less than that of the tank and is about 20% of the total. This share could easily be higher than 50% for the traditional oscillator at the same  $\alpha_V$  and  $I_{DC}$  as discussed in [6] and [13]. Finally, the total oscillator effective noise power ( $N_T$ ) and noise factor ( $NF_{Total}$ ) are given by

$$N_T \approx \frac{KT}{R_{in}} \cdot NF_{Total}, \quad NF_{Total} \approx \left( 1.05 + \frac{2\gamma_{M1}}{G_0} + 0.4\gamma_{MT} \right). \quad (20)$$

Equation (20) indicates the effective noise factor of the proposed class-F<sub>2</sub> oscillator is very close to the ideal value of  $(1 + \gamma)$  despite the aforementioned practical issues. The phase noise can easily be calculated by replacing (20) in (8). The oscillator FoM normalizes the PN performance to  $\omega_0$  and  $P_{DC}$ , yielding

$$FoM = -10 \log_{10} \left( \frac{10^3 \cdot KT}{2Q_t^2 \alpha_I \alpha_V} \cdot NF_{Total} \right). \quad (21)$$

Table I verifies the solidity of the presented phase noise analysis by comparing the results of SpectreRF PSS, Pnoise simulations with the derived theoretical equations. The expressions estimate the oscillator PN and share of different noise sources with an acceptable accuracy.

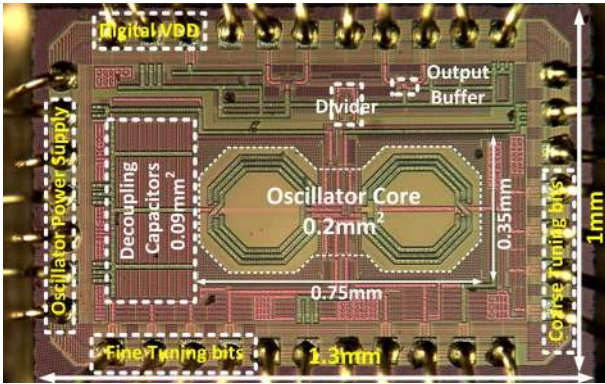
It is also instructive to compare in Table II the benefits and drawbacks of the two flavors of class-F operation. Intuitively, the third-harmonic injection in class-F<sub>3</sub> [1] demonstrates a pseudo-square waveform with smaller ISF<sub>rms</sub> value and shorter commutating time. Consequently, it offers lower  $NF_{Tank}$  and  $NF_{GM}$ . On the other hand, class-F<sub>2</sub> operation provides larger voltage overhead for the gm-devices and tail current transistor without sacrificing the oscillator  $\alpha_V$ . Hence, it exhibits better



TABLE II

COMPARISON BETWEEN TWO FLAVORS OF CLASS-F OSCILLATOR FOR THE SAME Carrier Frequency = 8 GHz,  $V_{DD} = 1.2$  V, TANK Q-factor = 14,  $\Delta f = 10$  MHz AND  $R_p = 240 \Omega$ 

	Expression	Class-F <sub>3</sub> [1]	Class-F <sub>2</sub>
$\alpha_I$	$I_{\omega_0}/I_{DC}$	0.6	0.6
$\alpha_V$	$V_{osc}/V_{DD}$	0.8	0.9 (✓)
$NF_{Tank}$	$N_{Tank}/(KT/R_{in})$	0.7 (✓)	0.8
$NF_{GDS}$	$N_{GDS}/(KT/R_{in})$	0.3	0.25 (✓)
$NF_{GM}$	$N_{GM}/(KT/R_{in})$	$\approx 0.7\gamma_{M1}$ (✓)	$\approx \gamma_{M1}$
$NF_{GMT}$	$N_{GMT}/(KT/R_{in})$	$\approx 0.5\gamma_{MT}$	$\approx 0.4\gamma_{MT}$ (✓)
$NF_{Total}$		3.7dB (✓)	4.1dB
FoM	$\approx -10 \log_{10} \left( \frac{KT}{2Q_I^2} \frac{1}{\alpha_I \alpha_V} NF \right)$	192.9dB (✓)	192.9dB (✓)
$R_{in}$		$\approx R_p = 240\Omega$	$\approx R_p/(1+\eta^2) = 60\Omega$ (✓)
$P_{DC}$	$\left( \frac{V_{DD}^2}{R_{in}} \frac{\alpha_V}{\alpha_I} \right)$	8mW	36mW
Phase noise	$\approx 10 \log_{10} \left( \frac{KT}{2Q_I^2} \frac{1}{P_{DC}} \frac{1}{\alpha_I \alpha_V} NF \left( \frac{\omega_0}{\Delta\omega} \right)^2 \right)$	-144 dBc/Hz	-150.5 dBc/Hz (✓)

Fig. 15. Die photograph of the class-F<sub>2</sub> oscillator.

$NF_{MT}$ ,  $NF_{GDS}$  and  $\alpha_V$ . As expected, the effective noise factor and FoM of both topologies turns out to be identical. However, this implementation of class-F<sub>2</sub> automatically scales down the tank input parallel resistance and thus offers lower PN at price of larger area and slightly lower Q-factor due to the inter-connection of the two transformers.

## V. EXPERIMENTAL RESULTS

This oscillator work targets GSM-900 MHz and DSC-1800 MHz base-station PN requirements. Electromagnetic (EM) simulations reveal that the tank Q-factor would be slightly (i.e.,  $\sim 10\%$ ) better at 8 GHz as compared with 4 GHz for the same  $R_{in}$  and tuning range. However, the  $1/f$  noise up-conversion would be more severe at 8 GHz due to a larger share of the non-linear  $C_{gs}$  of gm-devices to the total tank's capacitance. Furthermore, the output impedance of the current source is lower at higher frequencies, which would lead to higher PN penalty due to the tank loading. Consequently, there seems to be altogether no clear performance advantage of the 8 GHz over 4 GHz operation. Considering the fact that the proposed oscillator has two transformers, the 8 GHz center frequency was chosen mainly to save die area.

The proposed class-F<sub>2</sub> oscillator, whose schematic is shown in Fig. 10, was realized in TSMC 1P7M 65 nm CMOS process technology. The die photograph is shown in Fig. 15. The oscillator core die area is  $0.2 \text{ mm}^2$ . The differential transistors are thick-oxide devices of  $22 (4 \mu\text{m}/0.28 \mu\text{m})$  dimension.

However, the tail current source  $M_T$  is implemented as a standard  $1 \text{ mm}/0.24 \mu\text{m}$  thin-oxide ( $t_{ox} = 2.6 \text{ nm}$ ) device. Note that the thin oxide device produces lower  $1/f$  noise corner than the thick one at the same area [19]. The aluminum capping layer ( $1.45 \mu\text{m}$ ), which is intended to cover bond-pads, is strapped to the ultra-thick top copper layer ( $3.4 \mu\text{m}$ ) to form the windings and improve the transformer's primary and secondary Q-factor to 14 and 20, respectively, at 8 GHz. The transformer's primary and secondary differential self-inductance is 560 pH and 1650 pH, respectively, with the DM and CM magnetic coupling factors of 0.8 and 0.15, respectively.

Four differential switched MOM capacitors  $B_{C0}-B_{C3}$  with the resolution of 40 fF placed across  $T_1$  secondary realize coarse tuning bits ( $C_2$ ), while the fine control bits  $B_{F0}-B_{F2}$  with LSB of 20 fF adjust  $\omega_c$  to near  $2\omega_{1d}$  to satisfy (7) and thus the class-F<sub>2</sub> operation. The effective  $C_{max}/C_{min}$  of the switched capacitor structures is determined by the strong tradeoff between the oscillator tuning range (TR) and tank Q-factor degradation due to the switch series resistance. The switched-capacitor's Q-factor is about 45 for 25% TR at 8 GHz. Furthermore, the interconnections of the two transformers also increase the tank losses by 10%, resulting in an average Q-factor of 14 for the entire tank.

The supply voltage connects to the center tap of  $T_1$  primary along with a 100 pF on-chip decoupling capacitor. The center tap of  $T_2$  secondary is connected to the bias voltage  $V_B$ , which is fixed at  $V_{DD}$  to minimize the number of supply domains and to guarantee safe oscillator start-up. The oscillator is very sensitive to noise at the  $M_{1,2}$  gates [see Fig. 13(a)]. Fortunately, no DC current is drawn from  $V_B$  so an RC filter of slow time constant is placed between  $V_{DD}$  and  $V_B$  to further reduce the bias voltage noise. Both  $T_1$  secondary and  $T_2$  primary windings center taps are connected to ground to avoid any floating nodes and make a return path for the negligible second harmonic current to improve the waveform symmetry.

The measured and simulated PN at 4.35 GHz (after the on-chip  $\div 2$  divider) at 1.3 V and 32 mA current consumption are shown Fig. 16. The PN of  $-145 \text{ dBc/Hz}$  at 3 MHz offset lies on the 20 dB/dec region, which extrapolates to  $-174.7 \text{ dBc/Hz}$  at 20 MHz offset (normalized to 915 MHz) and meets the GSM TX mobile station (MS) requirements with a very wide 13 dB margin. The GSM/DCS "micro" base-station (BTS) and DCS

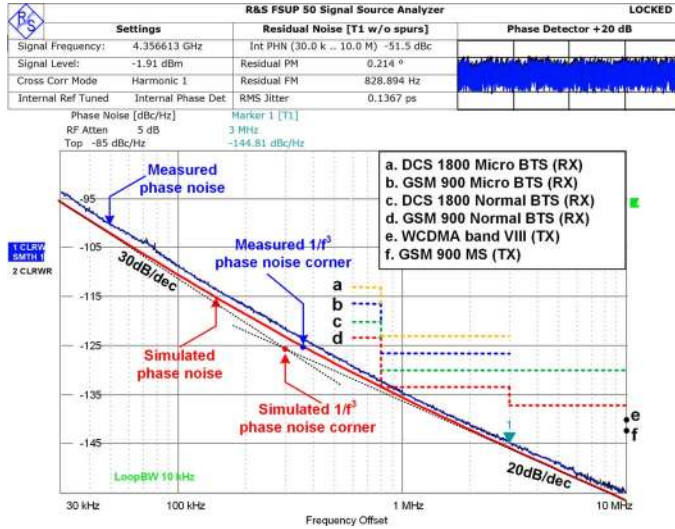


Fig. 16. Measured (blue) and simulated (red) phase noise plots at 4.35 GHz,  $V_{DD} = 1.3$  V and  $P_{DC} = 41$  mW. Specifications (MS: mobile station, BTS: basestation) are normalized to the carrier frequency.

“normal” BTS specs are met with a few dB of margin. These PN numbers are the *best ever* published at low  $V_{DD}$  (i.e.,  $\leq 1.5$  V). However, the toughest GSM base-station “normal” specifications at 800 to 900 kHz offset are within 1 dB of reach. The measured PN is just 1 dB higher than simulation in the 20 dB/dec region due to the power supply noise and additional tank loss caused by the routing of the tuning capacitors and dummy fill metals around the transformer.

The measured  $1/f^3$  PN corner shows less than 100 kHz increase over the simulation and is  $\sim 350$  kHz and  $\sim 250$  kHz at the highest and lowest side of the tuning range, respectively. This excellent  $1/f^3$  performance is achieved thanks to the following reasons. First, the  $1/f$  noise of the tail current source can appear as a CM signal at  $T_1$  primary and modulate the oscillation voltage. However, the  $T_1$  transformer will effectively filter out this CM AM signal, thus preventing any AM-to-PM conversion at the  $C_2$  switched capacitors and nonlinear  $C_{gs}$  of gm-devices. Second, the class- $F_2$  tank has two impedance peaks at the fundamental oscillation frequency and its 2nd harmonic. Hence, the 2nd harmonic of the drain current flows into a resistance of the tank instead of its capacitive part. It effectively reduces the  $1/f$  noise upconversion to the  $1/f^3$  phase noise due to Groszkowski phenomenon [20]. Third, the soft clipping effectively reduces the voltage variation of  $V_T$ , as shown in Fig. 11. Intuitively, it could reduce the DC and even-order coefficients of ISF at this node and thus alleviate the  $1/f$  noise conversion of the tail current transistor.

The PN noise beyond the 10 MHz offset is dominated by thermal noise floor from the divider and buffers set at  $-162$  dBc/Hz. The oscillator has a 19% tuning range from 7.2 to 8.7 GHz. Fig. 17 shows the phase noise and FoM of the oscillator at 3 MHz offset across the tuning range (after the  $\div 2$  divider). The average FoM is as high as 191 dBc/Hz and varies less than 2 dB. The oscillator also reveals a very low frequency pushing of 42 and 22 MHz/V at the highest and lowest frequencies, respectively.

Fig. 18 shows the PN performance versus its current consumption. The circuit cannot satisfy Barkhausen oscillation cri-

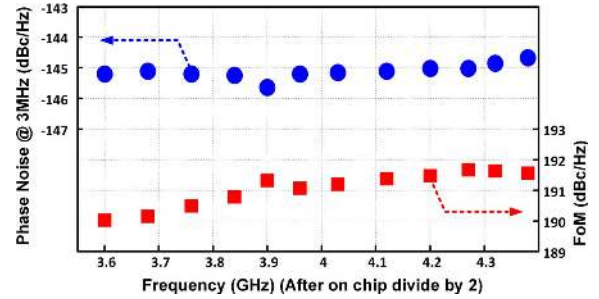


Fig. 17. Measured phase noise and FoM at 3 MHz offset versus carrier frequency.

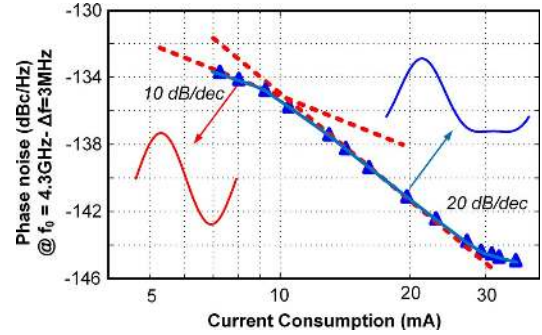


Fig. 18. Measured phase noise at 3 MHz offset frequency from 4.3 GHz carrier versus the oscillator current consumption.

terion at  $I_{DC} < 7$  mA. The oscillator phase noise is improved only by 10 dB/dec between 7 to 12 mA due to the drop in the oscillator current efficiency  $\alpha_I$  and loading of the tank's Q-factor by the gm-devices entering the linear region. Note that even though the tank has an additional impedance at  $2\omega_0$ , the second harmonic of the drain current is negligible and, consequently, the drain oscillation resembles a sinusoid. However, by further increasing the drain current, the soft clipping phenomenon appears where the tank loading and tail transistor noise effects are reduced significantly due to the class- $F_2$  operation. Consequently, PN improves by almost 20 dB/dec, which demonstrates a few dB of improvement compared to the traditional class-B operation (compare Figs. 3 and 18). Fig. 18 also indicates that the circuit can sustain the oscillation even with  $4\times$  lower  $I_{DC}$  and thus  $G_{MEF}$ , which translates into sufficient margin for the oscillator start-up over PVT variations.

Table III summarizes the performance of the proposed class- $F_2$  oscillator and compares it with the best spectral purity state-of-the-art oscillators. Note that this oscillator demonstrates the best PN with the highest power efficiency at relatively low supply voltage while abiding by the process technology reliability rules. Only the dual-core class-C oscillator [11] offers better PN performance but at the price of  $1.65\times$  larger  $V_{DD}$ ,  $3\times$  higher power consumption and 3 dB lower FoM or power efficiency.

## VI. RELIABILITY OF HIGH-SWING RF OSCILLATORS

RF oscillators are especially vulnerable to device and interconnect failures due to their large voltage and current peaks. The interconnect failure is mainly due to electromigration and can be easily cured by increasing the number of vias and widening high-current metal lines, which fortunately coincide

TABLE III  
COMPARISON OF STATE-OF-THE-ART IN ULTRA-LOW PHASE NOISE OSCILLATORS

	This Work	[11]	[7]	[1]	[13]	[21]	[22]
CMOS technology	65nm	65nm	65nm	65nm	350 $\mu$ m	55nm	BiCMOS 130nm
Supply voltage (V)	1.3	2.15	1.5	1.25	2.5	1.5	3.3
Frequency (GHz)	4.35 <sup>1</sup>	4.07	3.92 <sup>1</sup>	3.7 <sup>1</sup>	1.2	3.35 <sup>1</sup>	1.56
Tuning range (%)	19	19	10.2	25	18	31.4	9.6
Phase noise at 3 MHz (dBc/Hz)	-144.8	-146.7	-147.7	-142.2	-152	-142	-150.4
Norm. phase noise <sup>2</sup> (dBc/Hz)	-158.3	-159.6	-157.2	-154.3	-154.8	-153.3	-155
Power consumption (mW)	41.6	126.8	48	15	9.25	27	290
FoM (dB)	191.8 <sup>3</sup>	188.3	190.1	192.2	195	189	180
FoM <sub>T</sub> <sup>4</sup> (dB)	197.4	193.4	190.3	200.2	200.7	199	179.7
Transformers/inductors count	2	2	2	1	2	1	1
Oscillator structure	Class F <sub>2</sub>	Dual core Class-C	Hard clipping	Class F <sub>3</sub>	Noise Filtering	Class B/C	Colpitts

<sup>1</sup>after on-chip  $\div 2$  divider. <sup>2</sup>at 3 MHz offset frequency normalized to 915 MHz carrier.

<sup>3</sup>FoM drops to 191.5 dB by considering the divider power consumption of 2.6 mW.

<sup>4</sup>FoM<sub>T</sub> =  $|PN| + 20 \log_{10}((f_0/\Delta f) (TR/10)) - 10 \log_{10}(P_{DC}/1mW)$

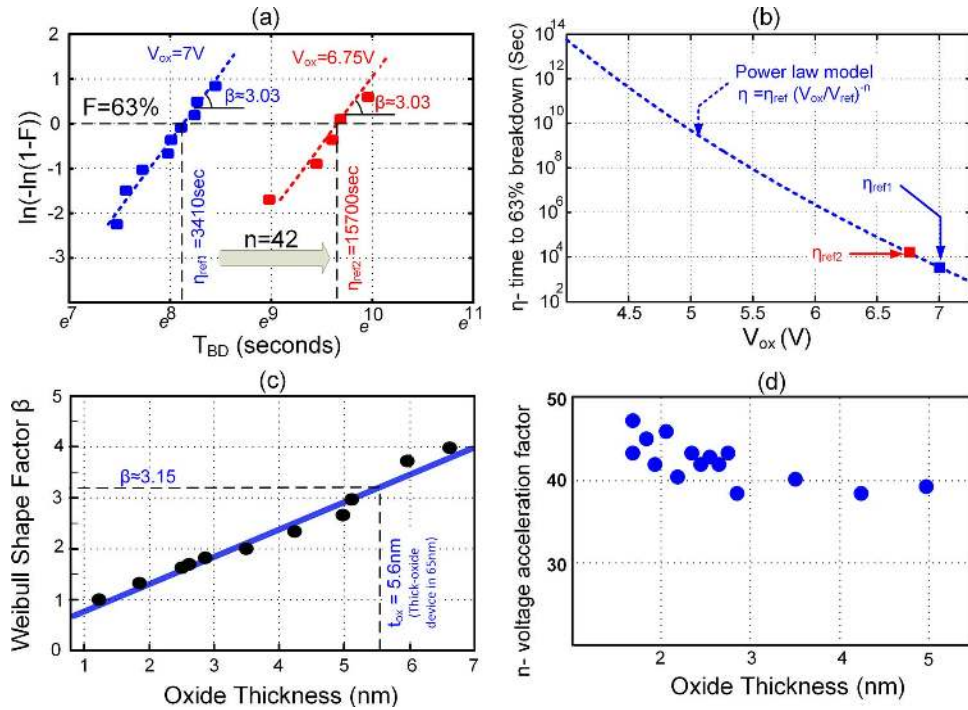


Fig. 19. (a) Measured cumulative failure rate  $F$  versus breakdown time  $T_{BD}$  for 14 samples of a thick-oxide transistor (176  $\mu\text{m}/0.28 \mu\text{m}$ ) at room temperature, (b) the projected  $\eta$  value versus different gate-oxide stress voltage based on the measured  $\eta_{ref}$ , (c) Weibull slope versus gate oxide thickness extracted from measurement results in [25], (d) voltage acceleration versus gate oxide thickness extracted from measurement results in [26].

with efforts to optimize the inductor Q-factor. However, the device failure becomes ever more serious and highly circuit dependent in scaled CMOS. Consequently, circuit designers of high-performance (thus, high-swing) RF oscillators must fully comprehend these reliability issues. Time dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) are considered two main failure mechanisms, which limit the max oscillation amplitude [23].

The HCI degradation would occur when the drain current,  $I_{DS}$ , and drain-source voltage,  $V_{DS}$ , are large at the same time. Thanks to the transformer's voltage gain, the proposed oscillator  $V_{DD}$  is low enough such that  $V_{DS}$  of its gm-devices can be much less than the standard voltage of thick-oxide transistors (2.5 V) when they operate in on-state (see Fig. 11). Consequently, the proposed oscillator is not inherently vulnerable

to HCI. However, the large oscillation swing applies a strong electric field across the gate-oxide of gm-devices ( $V_{DG}$ ,  $V_{GS}$ ), which can potentially reduce the long term reliability of the proposed oscillator due to TDDB [24].

The oxide breakdown stems from defects, such as electron traps, in the oxide structure. The rate of defect generation is almost proportional to the gate-oxide electric field and its leakage current density. This failure is a time-dependent statistically distributed phenomenon and is described by a well-known Weibull distribution

$$F = 1 - e^{-(T_{BD}/\eta)^\beta} \rightarrow \eta = T_{BD} (-\ln(1-F))^{-1/\beta} \quad (22)$$

where  $F$  is a cumulative failure probability and  $T_{BD}$  is a random variable for time-to-breakdown [25]. Both  $\beta$  and  $\eta$  are experimental parameters and defined as a Weibull shape slope and



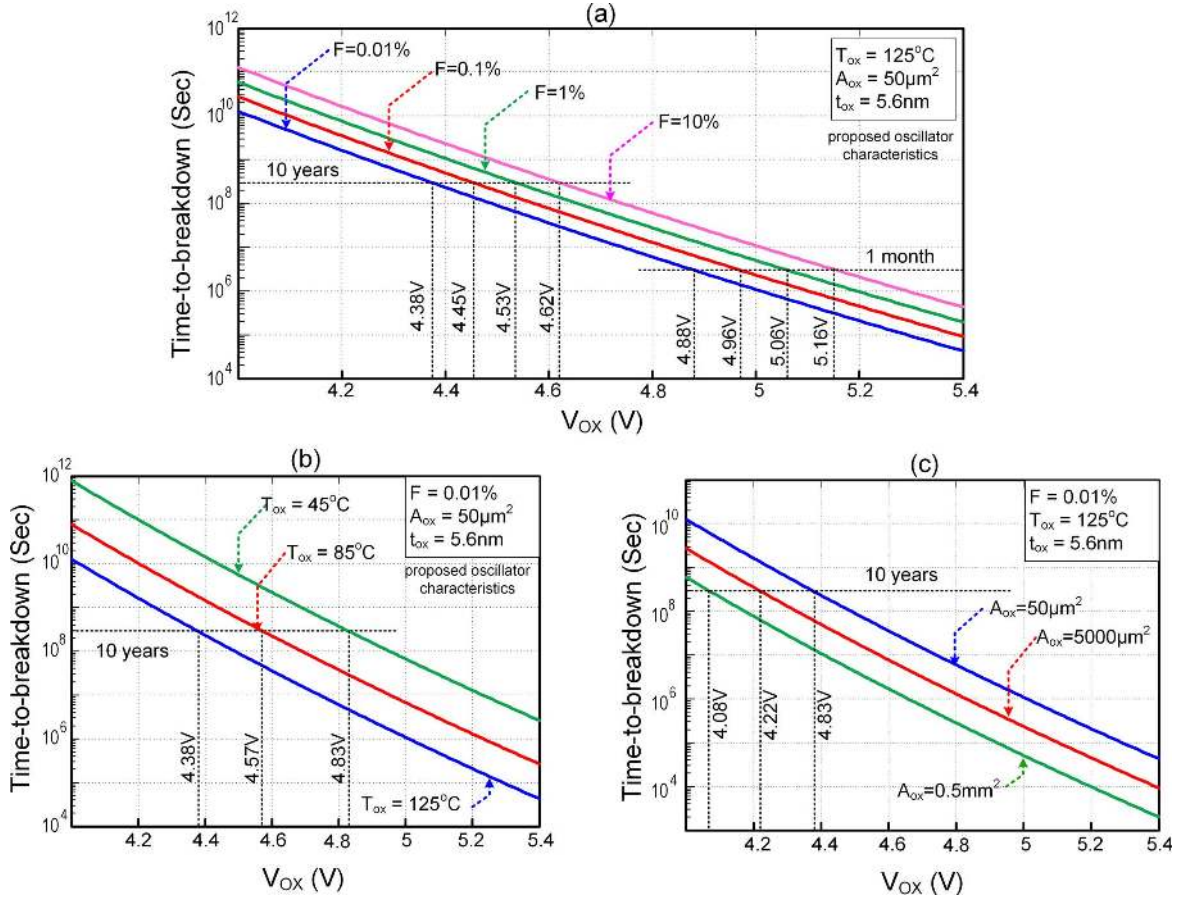


Fig. 20. Estimated time-to-breakdown [based on the measured parameters of Fig. 19(a)] of thick-oxide transistors in 65 nm CMOS versus maximum gate-oxide stress voltage for different (a) cumulative failure rates, (b) temperatures, and (c) gate-oxide areas.

characteristic  $T_{BD}$  at  $F = 63.2\%$ , respectively.  $\eta$  is a strong function of the total gate oxide area ( $A_{ox}$ ), absolute junction temperature ( $T_{ox}$ ) and stress voltage across the gate oxide ( $V_{ox}$ ). The  $\eta$  is usually estimated by means of voltage and temperature acceleration models from results acquired at relatively short measurements to the required product lifetime (e.g., 10 years). It is shown in [25] that  $\eta$  for a given circuit with arbitrary characteristics ( $A_{ox}$ ,  $V_{ox}$  and  $T_{ox}$ ) can be extrapolated from the reference data ( $x_{ref}$ ) by

$$\eta = \eta_{ref} \left( \frac{V_{ox}}{V_{ref}} \right)^{-n} e^{(E_a/K)(1/T_{ox} - 1/T_{ref})} \left( \frac{A_{ox}}{A_{ref}} \right)^{-1/\beta} \quad (23)$$

where  $n$  and  $E_a$  are, respectively, voltage acceleration and thermal activity energy factors.

The above procedure is now applied to our proposed class- $F_2$  oscillator to determine its  $T_{BD}$ . Fig. 19(a) shows the measured  $F$  versus  $T_{BD}$  for 14 samples of the thick-oxide transistor ( $176 \mu\text{m}/0.28 \mu\text{m}$ ) at room temperature when a large voltage (6.75 V and 7 V) is applied across the gate. The data points are easily mapped to a Weibull distribution curve as indicated by the dashed line. The cross-over of these curves at  $F = 63.2\%$  specifies the reference  $\eta$  values ( $\eta_{ref}$ ). The voltage acceleration ratio  $n$  is calculated by applying  $\eta_{ref}$  values and their related  $V_{ox}$  in (23). Furthermore, the slope of the curves determines  $\beta$ . Consequently, the estimated  $n$  and  $\beta$  values are respectively 42 and 3 for the thick-oxide devices ( $t_{ox} = 5.6 \text{ nm}$ ) in 65 nm

CMOS, which are close to extracted measured numbers from literature, as shown in Fig. 19(c) and (d) [25], [26]. The  $E_a$  is  $\sim 0.55 \text{ eV}$  and independent from the oxide thickness and temperature [27]. Consequently, the given oscillator  $\eta$  can be estimated by substituting the measured reference values, technology parameters, and circuit characteristics ( $A_{ox}$ ,  $V_{ox}$ ,  $T_{ox}$ ) in (23). Finally,  $T_{BD}$  is calculated by substituting the estimated  $\eta$  and the desired  $F$  in (22).

The lifetime estimation of our circuit as a function of  $V_{ox}$  is plotted in Fig. 20 for various  $F$ ,  $T_{ox}$  and  $A_{ox}$ . The plots indicate that the maximum voltage across the oxide for  $M_{1,2}$  transistors should be  $< 4.4 \text{ V}$  to ensure  $< 0.01\%$  failure during 10 years at  $125^\circ\text{C}$ . The max  $V_{ox}$  could be increased if higher failure rate or lower max operating temperature are accepted. The maximum dc voltage is thus established across the gate-oxide. However, the actual nature of stress in RF oscillators is not dc but an ac voltage  $V_{ox}(\omega_0 t)$ . Consequently, it is instructive to compare the static max  $V_{ox}$  with the actual operation when  $\eta$  changes over the period of the resonant frequency. Hence, the “effective”  $\eta$  is calculated as

$$\frac{1}{\eta_{eff}} = \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{\eta(V_{ox}(\omega_0 t))} d(\omega_0 t) \quad (24)$$

where  $\eta(V_{ox}(\omega_0 t))$  is given by (23) and can be expediently simplified to  $\eta = B \cdot (V_{ox}(\omega_0 t))^{-n}$ .

Starting with the application's desired operating time (i.e.,  $T_{BD}$ ) at a given failure rate ( $F$ ) in a given technology (i.e.,  $\beta$ ),

the parameter  $\eta_{\text{eff}}$  is first established as per (22) and is identical for dc and ac operations. For a dc operation,  $\eta = B \cdot (V_{\text{dc}})^{-n}$  and (24) results in

$$V_{\text{dc}} = \left( \frac{B}{\eta_{\text{eff}}} \right)^{1/n}. \quad (25)$$

However, for an ac operation,

$$\frac{1}{\eta_{\text{eff}}} = \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{B(0.5V_{\text{ac,max}}(1 + \sin(\omega_0 t)))^{-n}} d(\omega_0 t). \quad (26)$$

Solving this integral for the voltage acceleration factor  $n$  of 42 for the 65 nm CMOS thick-oxide devices,

$$V_{\text{ac,max}} = \left( \frac{11.5 \cdot B}{\eta_{\text{eff}}} \right)^{1/n}. \quad (27)$$

Consequently, the ac to dc maximum tolerable stress voltage ratio ( $V_{\text{ac,max}}/V_{\text{dc}}$ ) will be  $(11.5)^{1/n} \approx 1.06$ . We strongly emphasize that there are no significant differences in max  $V_{\text{ox}}$  at ac-peak and dc conditions due to the sharp slope of  $T_{\text{BD}}-V_{\text{ox}}$  curves in Fig. 20. As shown by integrating the voltage-dependent  $\eta(V_{\text{ox}})$  over the full oscillation cycle, the peak magnitude of the  $V_{\text{ox}}$  sine wave can be just 6% higher than what is determined for a fixed dc  $V_{\text{ox}}$ . Consequently, the slightly lower pessimistic value of  $V_{\text{ox}}$  in the dc condition could be used as an extra margin.

## VII. CONCLUSION

In this paper, we have proposed and analyzed a class-F<sub>2</sub> oscillator where an auxiliary impedance peak is introduced around the second harmonic of the oscillating waveform. The second harmonic of the active device current converts into voltage and, together with the fundamental component, creates a soft clipped oscillation waveform. The class-F<sub>2</sub> operation offers enough headroom for the low noise operation of the tail current transistor without compromising the oscillator current and voltage efficiencies. Furthermore, the special ISF of the soft clipping waveform reduces significantly the circuit-to-phase noise conversion. The additional resonant frequency is realized by exploiting a different transformer behavior in common-mode and differential-mode excitations. In addition, the tank input impedance is also scaled down without sacrificing its Q-factor. Consequently, the proposed structure is able to push the phase noise much lower than practically possible with the traditional LC oscillators while satisfying long-term reliability requirements. The proposed reliability acceleration analysis indicates that the oscillator will function for >10 years with <0.01% failure rate at 125 °C.

## ACKNOWLEDGMENT

The authors would like to thank A. Akhnouk, W. Straver, A. Kaichouhi, M. Alavi, A. Visweswaran, W. Wu, M. Shahmohammadi, A. A. Mehr, M. Tohidian, I. Madadi, Z. Zong, and A. Ximenes for the measurement support and technical discussions.

## REFERENCES

[1] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[2] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[3] M. Babaie and R. B. Staszewski, "Third-harmonic injection technique applied to a 5.87-to-7.56 GHz 65 nm class-F oscillator with 192 dBc/Hz FoM," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 348–349.

[4] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[5] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, Jun. 2012.

[6] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.

[7] A. Visweswaran, R. B. Staszewski, and J. R. Long, "A low phase noise oscillator principled on transformer-coupled hard limiting," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 300–311, Feb. 2014.

[8] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A 36 mW/9 mW power-scalable DCO in 55 nm CMOS for GSM/WCDMA frequency synthesizers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 348–350.

[9] M. Babaie, A. Visweswaran, Z. He, and R. B. Staszewski, "Ultra-low phase noise 7.2–8.7 GHz clip-and-restore oscillator with 191 dBc/Hz FoM," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, 2013, pp. 43–46.

[10] L. Roman, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "5-GHz oscillator array with reduced flicker up-conversion in 0.13- $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2457–2467, Nov. 2006.

[11] M. Tohidian, S. A. R. A. Mehr, and R. B. Staszewski, "Dual-core high-swing class-C oscillator with ultra-low phase noise," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, 2013, pp. 243–246.

[12] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[13] E. Hegazi, H. Sjolund, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[14] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[15] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[16] J. Chen, L. Ye, D. Titz, F. Ganesello, R. Pilard, A. Cathelin, F. Ferrero, C. Luxey, and A. Niknejad, "A digitally modulated mm-Wave cartesian beamforming transmitter with quadrature spatial combining," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 232–233.

[17] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.

[18] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.

[19] C. H. Jan *et al.*, "RF CMOS technology scaling in high-k/metal gate era for RF SoC (system-on-chip) applications," in *Proc. IEEE Int. Electron Devices Meeting*, 2010, pp. 604–607.

[20] J. Rael and A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2000, pp. 569–572.

[21] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2 GHz 55 nm CMOS hybrid class-B/class-C cellular TX VCO," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 354–355.

[22] J. Steinkamp *et al.*, "A Colpitts oscillator design for a GSM base station synthesizer," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, 2007, pp. 405–408.

[23] C.-M. Hung, R. B. Staszewski, N. Barton, M.-C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.

[24] M. Babaie and R. B. Staszewski, "A study of RF oscillator reliability in nanoscale CMOS," in *Proc. 21st IEEE Eur. Conf. Circuit Theory and Design*, 2013, pp. 243–246.

[25] E. Y. Wu *et al.*, "CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics," *IBM J. Res. & Dev.*, vol. 46, no. 2/3, pp. 287–297, Mar./May 2002.

- [26] E. Y. Wu *et al.*, "Voltage-dependent voltage-acceleration of oxide breakdown for ultra-thin oxides," in *Proc. IEEE Int. Electron Devices Meeting*, 2000, pp. 541–544.
- [27] E. Y. Wu *et al.*, "The effect of change of voltage acceleration on temperature activation of oxide breakdown for ultrathin oxides," *IEEE Electron Device Lett.*, vol. 22, no. 12, pp. 603–605, Dec. 2001.



**Masoud Babaie** (S'13) received the B.Sc. degree (with highest honors) from Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2004, and the M.Sc. degree from Sharif University of Technology, Tehran, in 2006, both in electrical engineering. He is currently working toward the Ph.D. degree at the Delft University of Technology, Delft, The Netherlands.

He joined Kavoshcom R&D Group, Tehran, Iran, in 2006, where he was involved in designing tactical communication systems. He was appointed the CTO of the company between 2009 and 2011. His research interests include analog and RF IC design for wireless communications.



**Robert Bogdan Staszewski** (M'97–SM'05–F'09) received the B.S.E.E. (*summa cum laude*), M.S.E.E., and Ph.D. degrees from the University of Texas at Dallas, Dallas, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, TX, USA, working on SONET cross-connect systems for fiber optics communications. He joined Texas Instruments, Dallas, TX, USA, in 1995, where he was elected a Distinguished Member of Technical Staff. Between 1995 and 1999, he was engaged in advanced CMOS read channel development for hard disk drives. In 1999, he co-started a Digital RF Processor (DRP) group within Texas Instruments with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS processes. He was appointed a CTO of the DRP group between 2007 and 2009. In July 2009 he joined Delft University of Technology, Delft, The Netherlands, where he is currently a part-time Full Professor. Since September 2014, he has been a Professor with University College Dublin (UCD), Dublin, Ireland. He has authored and coauthored one book, four book chapters, and 170 journal and conference publications and holds 120 issued U.S. patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters, and receivers.

Prof. Staszewski has been a TPC member of ISSCC, RFIC, ESSCIRC, ISCAS, and RFIT. He was a recipient of the IEEE Circuits and Systems Industrial Pioneer Award.