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An Ultra-Low-Power 2.4 GHz All-Digital Phase-Locked Loop With Injection-Locked Frequency Multiplier and Continuous Frequency Tracking

MUHAMMAD RIAZ UR REHMAN[1], ARASH HEJAZI[1], (Student Member, IEEE), IMRAN ALI[1], MUHAMMAD ASIF[1], (Member, IEEE), SEONGJIN OH[1], (Student Member, IEEE), PERVESH KUMAR[1], YOUNGGUN PU[1,2], SANG-SUN YOO[3], (Member, IEEE), KEUM CHEOL HWANG[1], YOUNGOO YANG[1], YEONJAE JUNG[1,2], HYUNGKI HUH[1,2], SEOKKEE KIM[1,2], JOON-MO YOO[1,2] and KANG-YOON LEE[1,2], (Senior Member, IEEE).

[1]Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, 16419, South Korea.
[2]SKAIChips, Sungkyunkwan University, Suwon, 16419, South Korea
[3]Department of Smart Automobile, Pyeongtaek University, Pyeongtaek 17869, South Korea.

Corresponding author: Kang-Yoon Lee (e-mail: klee@skku.edu)

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ABSTRACT This paper presents a 0.46 mW and 2.4 GHz; All-Digital Phase-Locked Loop (ADPLL) through an Injection-Locked Frequency Multiplier (ILFM) and Continuous Frequency Tracking Loop (CFTL) circuitry for low power Internet-of-Thing (IoT) applications. In the proposed ADPLL architecture to save power, the need for Time-to-Digital Converter (TDC) is eliminated through providing the CFTL circuitry. This feature makes the design compact, low power, and suitable for IoT applications. The proposed design is based on a synthesizable pulse injection and frequency-locked loop along with an ultra-low-power LC Digitally-Controlled Oscillator (LC-DCO). The presented CFTL circuit adjusts the frequency of the DCO continuously and prevents the frequency drift after the reference injection. Inside the designed LC-DCO core, the power consumption is minimized by optimizing the g_m/I_D and adjusting the power supply to 0.5 V. The proposed ILFM based ADPLL is fabricated in 55 nm CMOS technology and covers the operational frequency range of 2.402 GHz to 2.480 GHz with a reference frequency of 32 MHz. The measured phase noise performance of the ADPLL is -111.15 dBc/Hz at 1 MHz offset frequency from the carrier frequency of 2.4 GHz. It consumes only 0.46 mW power with an active area of 0.129 mm^2.

INDEX TERMS ADPLL; Injection Locked Frequency Multiplier; Low Power; Small Area; Internet of Things, Digitally-Controlled Oscillator;

I. INTRODUCTION

Nowadays, a frequency synthesizer is a key building block of a Radio Frequency (RF) transceiver, which provides the Local Oscillator (LO) signal to convert up or down the signal to the desired frequency band. With the advancement in Complementary-Metal-Oxide-Semiconductor (CMOS) technology, the design of a frequency multiplier based PLL is shifting from analog to digital, for low power and low area target applications [1]. The digital design provides significant advantages in terms of low power and low area [2-3]. Due to the benefits of the All-Digital Phase-Locked Loop (ADPLL), it becomes an attractive candidate for low power Internet-of-Things (IoT) applications. Traditional ADPLL design utilizes the Time-to-Digital Converter (TDC) for the phase offset detection [4-6]. But due to the high power consumption and complexity of the TDC, it is not suitable for low power design. Recently the Injection-Locked Frequency Multipliers (ILFM) become attractive options for the design of digital PLLs for a low phase noise performance with low power consumption [7-9]. As compared to analog sampling PLL, injection locked ADPLL offers less complexity, low cost and less area utilization.Through this technique, a very low jitter integer-N sclock multiplier can be implemented by using a ring oscillator (RO) or an LC Digitally Controlled Oscillator (DCO). The RO offers a wider tuning range with a small area but exhibits poor jitter

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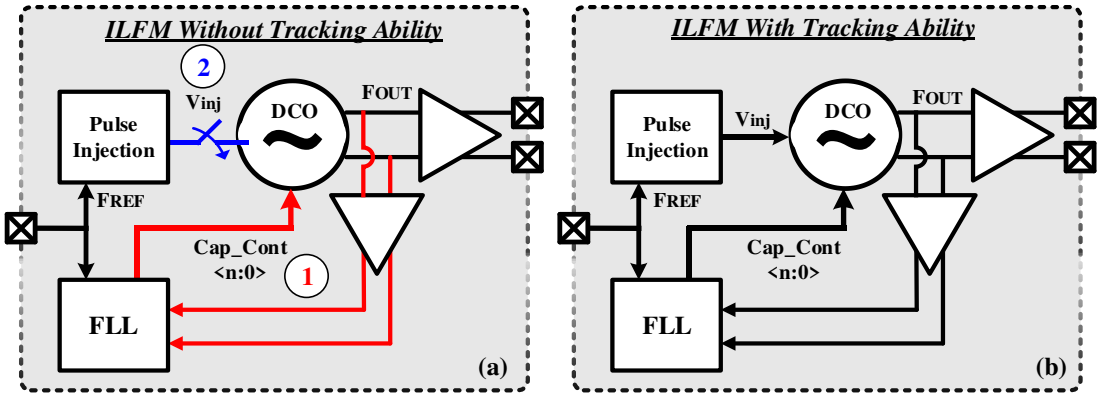

FIGURE 1. **Conventional ILFM (a) Injection only (b) injection with frequency tracking.**

performance [10]. On the other hand, the LC-oscillator based ILFM offers better phase noise performance and outstanding power efficiency [11]. In [18-19] an injection locked rotary traveling- wave oscillator (IL-RTWO) is presented which offers low skew clock generation. We can get multiple phases and its provides similar phase noise performance as LC-VCO.

By taking the benefit of the LC-DCO, a low phase noise and power LC-DCO based ILFM is proposed in this paper. It offers low power consumption and better jitter and phase noise performance as compared to the RO based ADPLL or ILFM design.

The error between the oscillator target frequency and the free-running frequency degrades the performance of the ILFM. On the other hand, the work proposed in [12] does only foreground frequency adjustment. After the injection by the reference clock, the frequency of the oscillator drifts due to PVT variations. This frequency drift would not be detected by the frequency-locked loop, and the structure can suffer from large reference spurs. Besides, without continuous frequency tracking ability the ILFM does not offer excellent jitter performance. To keep the oscillator at the target frequency, a frequency tracking loop is required. To overcome this problem the works [4-17] propose different techniques to keep the frequency error as low as possible. Although it gives better jitter performance but at the cost of high power consumption and design complexity. Figure 1 demonstrates the two approaches, with and without frequency tracking in the implementation of the ILFM. In Figure 1(a), a frequency lock loop (FLL) is used to bring the oscillator frequency near to the target frequency. After that, the FLL is disabled and reference frequency (FREF) is injected directly to the oscillator. In Figure 1 (b), an FLL is running continuously in the background to keep the DCO at the target frequency against PVT variations.

When the frequency tuning of the DCO through the FLL finished, the pulse injection circuit aligns the output phase of the DCO with F_REF and resets the phase error between two clocks. The effect of the reference frequency injection on the DCO output F_OUT is shown in Figure 2.

Figure 3 compares the phase noise performance for free running DCO, ILFM with the only injection, and ILFM with injection and frequency tracking ability. In this paper, an ILFM based ADPLL design is proposed, that offers low complexity and low power consumption. The reference injection controller and FLL controller are designed using HDL, which is fully synthesizable. The major contributions of this paper are as follows:

- Design of low power ILFM based ADPLL, which makes it suitable for low power and low-cost IoT applications.
- Design of FLL and injection controller are fully synthesizable which offers low area and design portability.

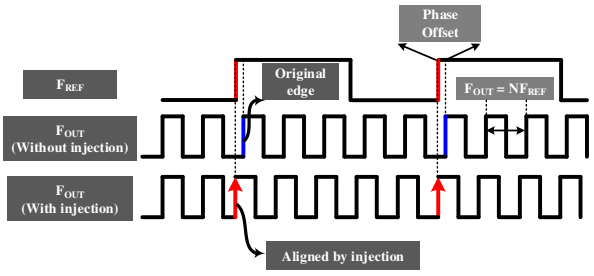

FIGURE 2. **Phase adjustment after injection of the reference frequency**

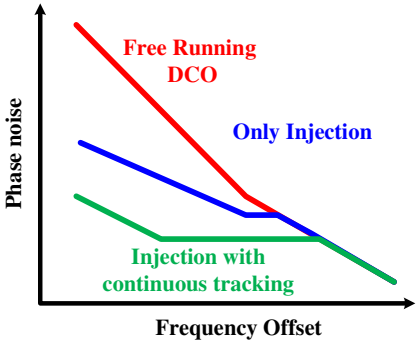

FIGURE 3. **Phase noise trend for RI-based ADPLL when Injection without CFTL and injection with CFTL**

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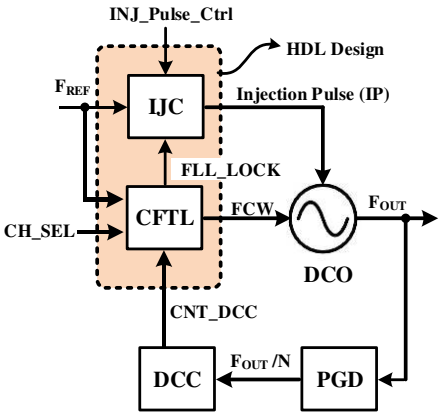

FIGURE 4. Block diagram of the ILFM based ADPLL.

- Design of low phase noise and low power LC-DCO that makes the whole design low power and suitable for the required specifications.

The rest of the paper is structured as follows: In section 2, the proposed architecture of the ILFM based ADPLL is discussed. Experimental results are discussed in section 3. Lastly, the paper is concluded in section 4.

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II. PROPOSED ILFM BASED ADPLL ARCHITECTURE

The block diagram of the proposed architecture of the ILFM based ADPLL is shown in Figure. 4. It consists of Injection Controller (IJC), Continuous Frequency Tracking Loop (CFTL), DCO, Programmable Divider (PGD), and DCO Clock Counter (DCC). The task of the CFTL is to bring the DCO output frequency FOUT to the target center frequency which can be selected by the CH_SEL. The CFTL is operating at the reference frequency of FREF. The Frequency Control Word (FCW) is provided to the DCO by the CFTL to increase or decrease the frequency of the DCO output (FOUT). The FOUT is divided by the PGD and the output of the PGD is fed to the DCC. The output of the DCC is used by the CFTL and it is compared with the target value depending on the channel frequency. The CFTL increase or decrease the output frequency of DCO by adjusting the FCW. Once the CFTL brings the DCO frequency to the target frequency, it sets the FLL_LOCK signal to high and enables the IJC. The IJC adjusts the phase of the DCO by periodically injecting the reference frequency pulse to the DCO. The pulse width of the injection pulse is controlled by the INJ_Pulse_Ctrl, and different injection pulse widths would be made through this block. Narrow pulse width for the injection process is essential for reduction in distortion caused by pulse injection. However lock failure can occur due to excessively narrow pulse width or strong distortion can occur due to wide pulse width. Figure. 5 shows the block diagram of the IJC. It mainly consists of the Flip-Flop (FF), Delay Multiplexer (DM), and buffer delay line. It is designed through HDL to make it fully synthesizable. The data input of the FF is set to high, and it is clocked by FREF. The FREF propagates through the delay line.

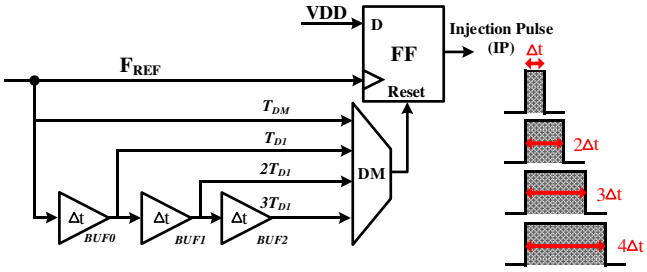

FIGURE 5. Block diagram of the injection controller.

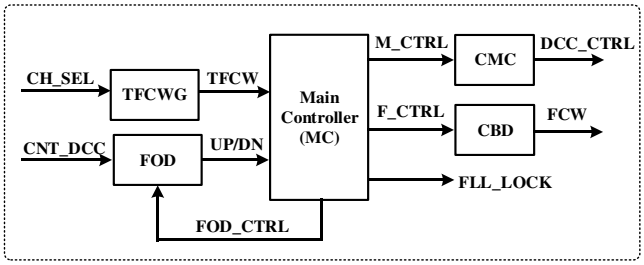

FIGURE 6. Block diagram of CFTL.

The output of each delay cell is connected to the DM input. By controlling the INJ_Pulse_Ctrl, we can get the delayed version of FREF at the output of the DM. The output of DM is used to reset the FF to control the injection pulse width. The timing diagram of the operation of the IJC is shown in Figure. 5. The purpose of the CFTL is to bring the free-running DCO output frequency to the target channel frequency. It uses a binary searching algorithm to bring the DCO frequency to the target frequency. Let's suppose we have 40 channels which can be specified through k where k= 0, 1, 2 … 39. To select a channel among 40 channels, the FLL generates the frequency control word (FCW) for the DCO by the following equation.

$$N_{FCW}(k) = k + N_{CH0}(\frac{M}{D} \times 10^{-6}) \quad (1$$

Where the $N_{FCW}(k)$ is the required FCW as a function of k, N_{CH0} is the base frequency of the channel 0, M is the frequency multiplier for the DCO and DCO frequency division factor is given by D.

The block diagram of the CFTL is shown in the Figure. 6. The main blocks of the CFTL consist of the Main Controller (MC), Counter Mask Control (CMC), Target Frequency Control Word Generator (TFCWG), Frequency Offset Detector (FOD), and Capacitor Bank Decoder (CBD). The CFTL is fully synthesizable and designed by HDL coding. The MC is controlling the overall operation of the CFTL.

The DCC will count the DCO clock cycles within the counter mask duration generated by CMC. The TFCWG generates the target frequency control word (TFCW) which is provided to the MC. The FOD compares the current DCO frequency with the target DCO frequency. It generates the control signals for the MC to increase or decrease the DCO frequency. To achieve the target frequency, the CBD controls the capacitor banks in the DCO and increases or decreases the

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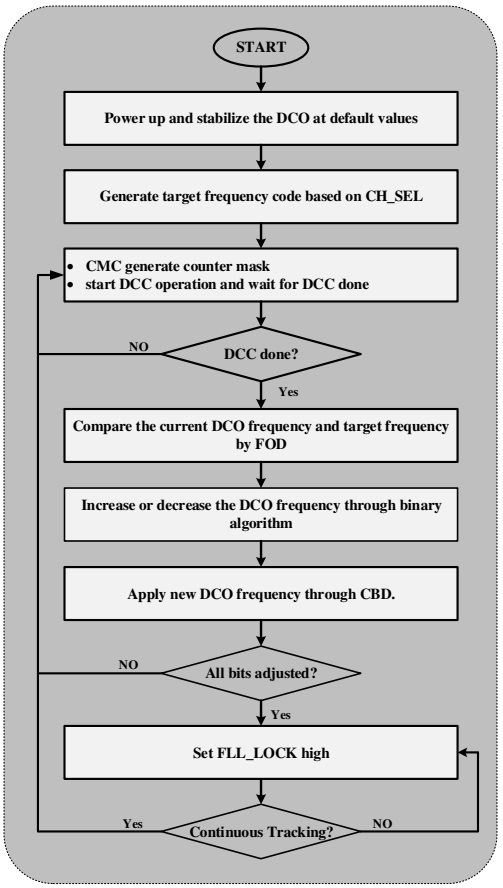

FIGURE 7. Flow diagram of CFTL

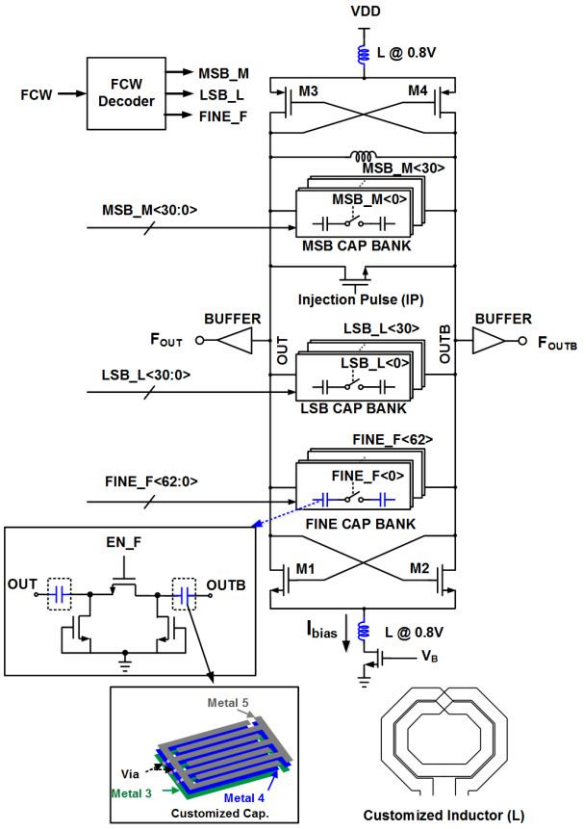

FIGURE 8. Simplified architecture of DCO.

DCO frequency. The CBD generates a corresponding thermometer code to control the capacitor's bank in the DCO. The flow diagram indicating the operation of the CFTL is shown in Figure 7. When the CFTL is powered up, then it is initialized with the default setting of the DCO and wait till DCO output frequency is stable. Then the TFCW generates the Target_F code based on the CH_SEL. The MC provides mask control (M_CTRL) signal to the CMC to generate the counter mask. The DCC starts counting the number of cycles based on the counter mask provided by DCC_CTRL. The MC waits till DCC completes its operation. After the completion, the MC activates the FOD to compare the DCO current frequency (CNT_DCC) and the target frequency. The FOD generates the UP/DN control signals accordingly to increase or decrease the FOUT. The MN adjust the DCO frequency through a binary algorithm. The binary algorithm adjusts bits of the capacitor banks from MSB to LSB to achieve target DCO frequency. After adjusting all control bits of DCO, the MN generates the FLL LOCK signal and the DCO output frequency is set at the target frequency. In the case of continuous tracking, the CFTL again calculates the DCO current frequency and compensates any PVT variations. Reference frequency is used as 32 MHz with 50% duty cycle.Duty cycle of refence frequency significantly affects the operation of the ADPLL. It can result in incorrect calculation of output frequency of ADPLL and cause strong distortion at the output of ADPLL.

The DCO is designed by focusing on the ultra-low power consumption for IoT applications. The target frequency range of the DCO is from 2.402 GHz to 2.480 GHz. The DCO is designed by MOSFET switches and their sizes are adjusted to provide almost ideal characteristics. During the design, considering the Process, Voltage, and Temperature (PVT) variations, the frequency range of the DCO is optimized to use the maximum inductance value for the resonance. Besides, it offers high swing characteristics and omits the need for increasing current to achieve sufficient swing. The proposed DCO operates in the sub-threshold region and satisfies the oscillation condition of equation (2) as represented in [13].

$$g_m \geq 1/R_p \qquad (2$$

where g_m and R_p are the transconductance of the cross-coupled pair and equivalent parallel resistance of the tank, respectively. The high-frequency resolution is achieved through the fine-tuning bank. The small capacitance is achieved through customized lateral MOM capacitors. This provides low capacitance values of 16.22 aF. An ultra-wide Aluminum (Al) metal layer is used as a superconductor to eliminate routing metal parasitic inductance. The simplified DCO schematic is shown in Figure 8. Three capacitor banks configurations

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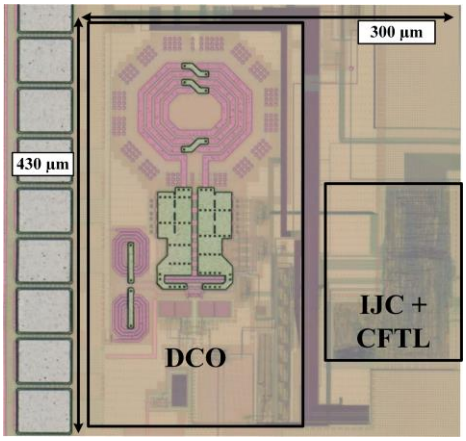

FIGURE 9. **Chip photograph of the proposed ILFM based ADPLL.**

(MSB CAP BANK, LSB CAP BANK, and FINE CAP BANK) are shown which are controlled by the decoding FCW. A low supply voltage (VDD) of 0.5 V is used for the DCO, which reduces the total power consumption of the DCO circuit efficiently. Each MSB CAP Bank and LSB CAP bank consist of 32 capacitors units. While the FINE CAP bank consists of 64 unit capacitors. The 1- bit resolution of the MSB CAP BANK, LSB CAP BANK, and FINE CAP BANK is 18.7 MHz, 72 kHz, and 4.8 kHz, respectively

III. EXPERIMENTAL RESULTS

The chip is fabricated using 55 nm CMOS technology. Figure 9 shows the microphotograph of the proposed chip. The active area of the proposed ILFM is 0.129 mm^2. The active size of DCO is 0.1175 mm^2 which mainly because of the inductor. The area of IJC and CFTL is significantly smaller than the DCO.

The measurement environment of the proposed ILFM is shown in Figure 10. It consists of a fabricated chip with the test board, spectrum analyzer, power supply, and UART based control of chip The tuning curves for the DCO versus tuning codes to capacitor banks MSB and LSB are shown in Figure 11. As we increase the tuning codes for the MSB capacitor bank, the output frequency of DCO is changing with a large frequency offset which is around 18 MHz. Due to PVT

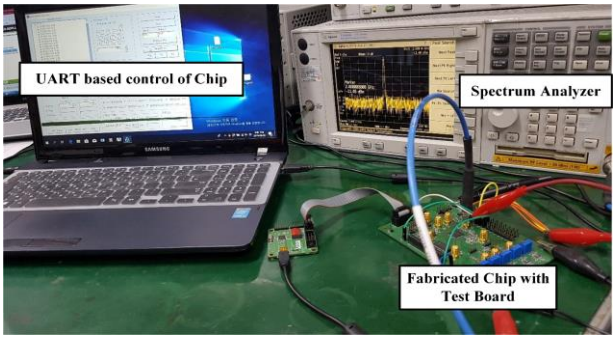

FIGURE 10. **Chip Measurement Setup**

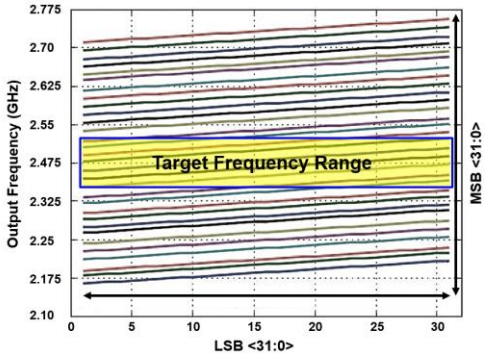

FIGURE 11. **Tuning curve of DCO versus tuning codes to cap banks MSB and LSB..**

variation, the step size for the output frequency of DCO is not equal to the lower tuning range but in target frequency range the output frequency of DCO shows linear step size. The change in LSB tuning codes for the DCO shows almost linear behaviors and it has fewer effects of PVT variation at the DCO output frequency. Phase noise is measured by using divider output which divides the DCO output frequency by a factor of 4. The phase noise performance of the ILFM based ADPLL is about -111.15 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz. The operation of the FLL is shown in

figure 12. The DCC generates a counter mask for counting the number of cycles of DCO output. At the start, the difference in the target frequency and DCO output frequency is large so a small counter mask is generated. When the output frequency of DCO is getting closer to the target frequency, CMC adaptively increases the duration of mask for the better accuracy of the target frequency. When the target frequency is achieved at the DCO output, the FLL_LOCK signal is set high. When the counter mask is generated through DCC_CTRL, the counter is reset through the RST_CNT signal. The phase noise of ILFM based ADPLL is shown in figure 13. The output frequency is 2.4 GHz for the measurement of DCO phase noise. The phase noise at offset of 10 kHz, 100 kHz, 1 MHz, 10 MHz and 100 MHz are -88.28 dBc/Hz, -86.72 dBc/Hz, -111.15 dBc/Hz, -122.99 dBc/Hz, and -141.74 dBc/Hz respectively. The Spectrum of the output of ILFM based ADPLL after injection of 32 MHz reference are shown in figure 14. Table 1 shows the comparison of the proposed design with the previous architectures. The integrated rms jitter of proposed design is 1.652ps. Other works such as [16] , [17] and [7] shows better integrated rms jitter performance but at the cost of additional hardware which results in design complexity and higher power consumption.
The figure of merit (FoM) to evaluate the performance of the design based on the measured integrated jitter and the power consumption is given by equation (3).

$$FoM = 10log_{10}\left[\left(\frac{\sigma_t}{1s}\right)\left(\frac{P_{DC}}{1mW}\right)\right] \quad (3)$$

Where σt is integrated jitter, P_{DC} is the power consumption of the design, and 1s indicates the one second time reference.

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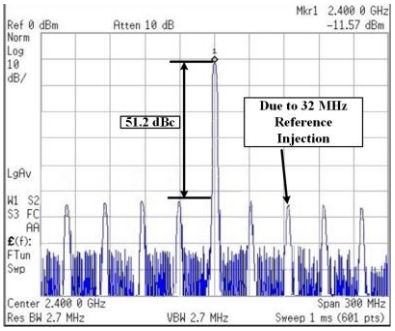

FIGURE 14. The Spectrum of the output of ILFM based ADPLL after injection of 32 MHz reference.

TABLE 1 indicates that FOM of proposed design shows better performance than previous works. It is mainly due to less power consumption as compared to previous designs.

VII. CONCLUSION

An ILFM based ADPLL was proposed for low power IoT sensor applications. The ILFM based ADPLL eliminates the requirement of TDC which makes the design simple and reduces the power consumption. The operating frequency range of the ILFM based ADPLL is from 2.402 to 2.480 GHz. The power consumption of the whole architecture is minimized using all-digital implementation and design of an ultra low power LC-DCO. It consumes only 0.46 mW with an area of 0.129 mm^2. The phase noise is -111.15 dBc/Hz at 1 MHz offset from the carrier frequency of 2.4 GHz.

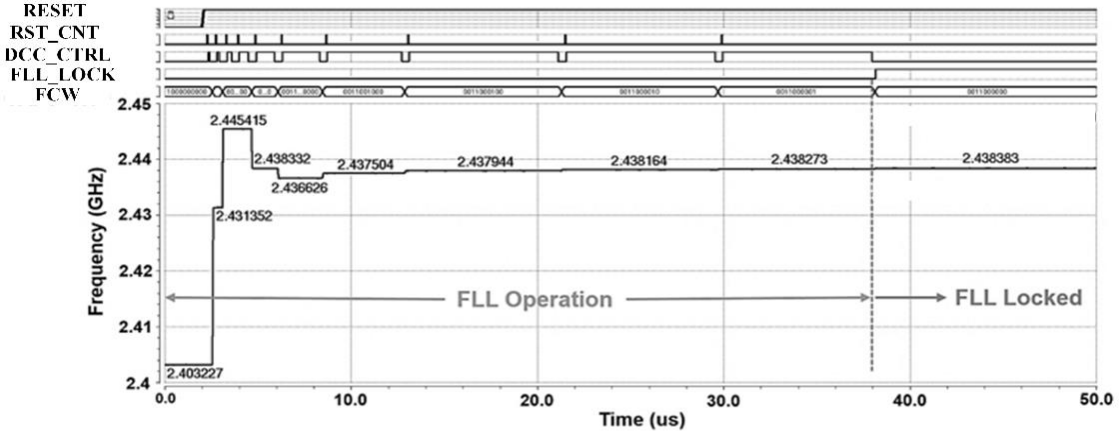

FIGURE 12. The Frequency-Locked Loop Operation.

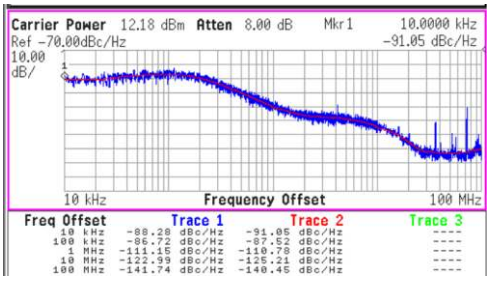

FIGURE 13. Phase noise plot of ILFM based ADPLL at 2.4 GHz.

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TABLE I
PERFORMANCE COMPARISON

	[14]	[15]	[16]	[17]	[7]	This work
Technology (nm)	40	55	65	65	65	55
Architecture	PLL	PLL	PLL	PLL	PLL	PLL
Output Frequency Range (GHz)	0.4-1.6	0.216	0.52-1.15	2.5-5.75	2.5-5.63	2.402-2.480
Reference Frequency (MHz)	50	27	150	125	156.25	32
Integrated RMS jitter (ps)	2.29	2.4	0.42	0.34	0.168	1.652
Phase noise dBc @1MHz	-106	-122	-119	-115	-105	-110.78
Spur Level dBc	-44	-70	NA	-45	-42	-51.2
Power (mW)	1.49	6.9	3.8	5.3	15.4	0.46
Area (mm^2)	0.14	0.03	0.028	0.09	0.06	0.129
FOM	-231.1	-224	-241.3	-242.1	-243.6	-245.3

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MUHAMMAD RIAZ UR REHMAN received his B.S. Computer Engineering and M.S. Electrical Engineering from University of Engineering and Technology, Taxila, Pakistan, in 2007 and 2011, respectively. From 2007 to 2016, he was with Horizon Tech Services, Islamabad, Pakistan, where he was a Senior Engineer of the Product Development Division. He is currently working toward the Ph.D. degree in the School of Information and Communication Engineering at Sungkyunkwan University, Suwon, Korea. His research interests include time to digital conversion systems, and embedded and digital systems design.

ARASH HEJAZI received the B.S. degree in electrical and electronics engineering from the Islamic Azad University of Urmia, Urmia, Iran, in 2013, and the M.S. degree in electrical and communication systems engineering from the Urmia Graduate Institute, Urmia, Iran, in 2016. He is currently pursuing the Ph.D. degree in electrical and electronics engineering with the ICLab, Sungkyunkwan University, Suwon, South Korea. His research interests include CMOS RF transceiver, wireless power transfer, analog/all-digital phase-locked loop, delay-locked loop, and time-to-digital converter for time-of-flight applications.

IMRAN ALI received his B.S. and M.S. degrees in Electrical Engineering from University of Engineering and Technology (UET), Taxila, Pakistan, in 2008 and 2014, respectively. He received his Ph.D. degree in Electronic and Electrical Engineering from Sungkyunkwan University, South Korea in 2020. From 2008 to 2015, he was with Horizon Tech. Services, Islamabad, Pakistan, where he was a Senior Engineer in the Product Development Division and worked on the design and development of hardware-based crypto/non-crypto systems. He is currently a Post-Doctoral Research Associate with the College of Information and Communication Engineering, Sungkyunkwan University, South Korea. His research interests include digital system design, digital controllers, digital calibration algorithms, artificial intelligence, and analog/digital mixed-signal integrated circuits.

MUHAMMAD ASIF received his B.S. in Electrical and Electronic Engineering from the National University of Modern Languages and Science, Islamabad, Pakistan, in 2013. He completed his M.S in Electrical and Computer Engineering from Sungkyunkwan University, Suwon, South Korea, in 2020. Currently, he is serving as a researcher in the Integrated Circuits (IC) Lab at Sungkyunkwan University, Suwon, South Korea. His research interests include the implementation of power integrated circuits, analog/digital mixed circuits, and CMOS digital controller.

SEONGJIN OH received his B.S. degree from the Department of Electronic Engineering at Sungkyunkwan University, Suwon, Korea, in 2014, where he is currently working toward the Combined Ph.D. & M.S degree in School of Information and Communication Engineering. His research interests include CMOS RF transceiver, All Digital Phase-Locked Loop, Wireless Power Transfer Receiver, and Rectifier.

Pervesh Kumar (Student Member, IEEE) received his B.S., in Electrical (computer) Engineering form COMSATS Institute of Information Technology Lahore, Pakistan and M.Sc. in Computer Science from South Asian University New Delhi, India in 2013 and 2015 respectively. Currently he is pursuing Ph.D in Electrical and Computer Engineering, with School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interests include VLSI system, digital system design, artificial intelligence and deep learning.

YOUNGGUN PU received his B.S., M.S., and Ph.D. degrees from the Department of Electronic Engineering at Konkuk University, Seoul, Korea, in 2006, 2008, and 2012, respectively.
From 2012 to 2013, he served as a Senior Engineer in Modem RF Lab at DMC R&D Center, Samsung Electronics, Korea. From 2013 to 2019, he worked as a Senior Engineer at WDT/Hivics, Korea. Currently, he is a research Professor at Sungkyunkwan University. His research interest is focused on high-speed interface, CMOS fully integrated frequency synthesizers, oscillators, and RF transceivers.

Sang-Sun Yoo received his B.S. degree from Dong-guk University, Seoul, Korea, in 2004, and his M.S/Ph.D. degree received from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2012. He worked for System LSI division in Samsung Electronics from 2012 to 2015 where he focused on ADPLL for 3/4G mobile applications as a senior design engineer. From 2015 to 2016, he was a Research Assistant Professor at KAIST and Sungkyunkwan University. Since 2017, he has been with the Department of Smart Automobile, Pyeongtaek University, where he is currently an Assistant Professor. His research interests include RF systems for mobile communications, reconfigurable RFICs, automotive ICs, ADPLL, RFID, and sensor communications.

Keum Cheol Hwang (SM' 13) received his B.S. degree in Electronics Engineering from Pusan National University, Busan, South Korea in 2001 and M.S. and Ph.D. degrees in Electrical and Electronic Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea in 2003 and 2006, respectively. From 2006 to 2008, he was a Senior Research Engineer at the Samsung Thales, Yongin, South Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and Cass-grain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor in the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea from 2008 to 2014. In 2015, he joined the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, where he is now an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multi-band/broadband antennas and radar antennas, and optimization algorithms for electro-magnetic applications. Dr. Hwang is a Life-Member of KIEES, a senior member of IEEE and a member of IEICE

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Youngoo Yang (SM' 15) was born in Hamyang, Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology (Postech), Pohang, Korea, in 2002. From 2002 to 2005, he was with Skyworks Solutions Inc., Newbury Park, CA, where he designed power amplifiers for various cellular handsets. Since March 2005, he has been with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently an Associate Professor. His research interests include power amplifier design, RF transmitters, RFIC design, integrated circuit design for RFID/USN systems, and modeling of high power amplifiers or devices.

Yeonjae Jung received the B.S., M.S. and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1997, 1999, and 2003, respectively.
From 2003 to 2014, he was with GCT Semiconductor Inc., San Jose, CA, where he was involved in the design of CMOS RF transceiver ICs for W-CDMA, WLAN, WIMAX, CDMA, GPS, and LTE. From 2014 to 2020, he was with Celfras Semiconductor Inc., where he worked on BLE v4.2 ultra-low power RF transceiver IC and power ICs for wireless power receiver, battery charger, and DC-DC converter. He is currently a VP with SKAiChips and a university-industry collaboration professor also with Sungkyunkwan University. His research interests include the design of power integrated circuits and CMOS RF transceiver.

Hyungki Huh was born in Seoul, Korea. He received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering and Computer Science, Seoul National University, in 1998, 2001, and 2006, respectively.
From 2001 to 2014, he was with GCT Semiconductor Inc., San Jose, CA, where he was involved in designing wireless transceivers. From 2017 to 2021. He was with Anapass Inc., Seoul, where he was involved in designing high-speed serial links. In 2021, he joined SKAIChips Co., Suwon, as a Chief Design Officer. Currently, he is a university-industry collaboration professor also at Sungkyunkwan University. His research interests are in the area of frequency synthesizers, high-speed communication interfaces, and PMIC.

Seokkee Kim received his B.S., M.S., and Ph.D. degrees from Seoul National University, South Korea, in 1997, 1999, and 2006, respectively.
From 2001 to 2016, he was with GCT Semiconductor Inc. From 2016 to 2021, he was with Celfras Semiconductor Inc., Seoul, South Korea. In 2021, he joined SKAIChips Co., Suwon, as a Chief Design Officer. Currently, he is a university-industry collaboration professor also at Sungkyunkwan University. His research interests includes analog backend design and mass-production management, power management intergrated circuits (PMICs) implementation, and CMOS RF transceiver and SOC integrated implementation.

Joon-Mo Yoo received his B.S. degree from the Department of Electronic Engineering at Ajou University, Gyeonggi-do, Korea, in 2002, M.S. from the School of Electrical Engineering at Seoul National University, Seoul, Korea, in 2004 respectively.
From 2004 to 2014, he worked as Principal Engineer and R&D Manager in GCT Semiconductor, Inc, at San Jose, CA, and GCT Research, Inc, in Korea, where he's developing PHS, CDMA, WCDMA, LTE RF Multi-mode Multi band transceivers. From 2014 to 2016, he worked as Chip Development Director at MELFAS, Korea, where he was leading the capacitive touch-screen controller IC development. And then he worked as Sr. Director at Celfras Semiconductor located in Jiangxi province in China from 2016 to 2021, where he leading for the various power of wireless-charging solutions. Currently, he is working at SKAIChips as an R&D executive at Sungkyunkwan University. His research interest is focused on digital circuit design and CMOS RF transceiver and wireless charging solutions.

KANG-YOON LEE received the B.S., M.S., and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chipsets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University as an Associate Professor. Since 2012, he has been with the College of Information and Communication Engineering, Sungkyunkwan University, where he is currently a Professor. His research interests include the implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.