An Ultra-Low-Power Digitally-Controlled Buck Converter IC for Cellular Phone Applications

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Abstract— **This paper describes a dual-mode digitally-controlled buck converter IC for cellular phone applications. An architecture employing internal power management is introduced to ensure voltage compatibility between a single-cell lithium-ion battery voltage and a low voltage integrated circuit technology. Special purpose analog and digital interface elements are developed. These include a ring-oscillator based ADC (ring-ADC), which is nearly entirely synthesizable, robust against switching noise, and has flexible resolution control, and a very low power ring oscillator-multiplexer based Digital PWM generation module (ring-MUX DPWM). The chip, which includes an output power stage rated for 400 mA, occupies 2 mm^2 active area in 0.25-μm CMOS. Very high efficiencies are achieved over a load range of 0.1 to 400 mA. Measured quiescent current in PFM mode is 4 μA.**

I. Introduction

This paper presents an ultra-low-quiescent-power dual-mode digitally-controlled buck converter IC for cellular phone applications. While the cellular phone is in talk mode, the load on the buck converter is high and pulse width modulation (PWM) is used to achieve high regulation quality as well as high efficiency. However, when the cellular phone is in standby mode, in which the load current is very low, PWM mode leads to low efficiency due to excessive switching, gate drive, and quiescent current losses. To extend the standby time a cellular phone can sustain with each full charge of the battery, pulse frequency modulation (PFM) mode is preferred for light load operation. The designed IC supports PWM mode for heavy load and PFM mode for light load. The system block diagram of the buck converter IC and the external filter is shown in Fig. 1. The pin MODE is used to switch between the two modes. The PFM mode quiescent power is the fundamental limitation on light-load efficiency, and in this work, an ultra low quiescent current of 4 μA is achieved in PFM mode. Details of the dual-mode design are presented in Section II.

For the digital implementation, small feature size processes with low supply voltages are preferred for implementing the digital circuits to achieve small die area, high speed, and low power consumption. In cellular phone applications, the power supply of the buck converter system is usually a single cell lithium-ion battery, with voltage range of 2.8-5.5 V. Thus, the input voltage of the converter may be higher than the allowed supply voltage of the process (e.g., maximum 2.75 V for a 0.25-μm CMOS process). A solution that allows a low voltage process to be used for the digital controller with high input voltage can be of great interest considering the possible cost reduction from integrating the switching regulator on the same die with the power train devices. Internal power management is introduced to resolve the conflict of high input voltage and a low voltage process, the details of which are also presented in Section II.

The Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM) are used to provide the analog and digital interface between the digital compensation network and the buck converter. A general purpose ADC can be unnecessarily expensive in terms of both power consumption and chip area, therefore a novel ring-oscillator-based averaging ADC (ring-ADC) is developed which has reduced quantization range. The details of the ADC are

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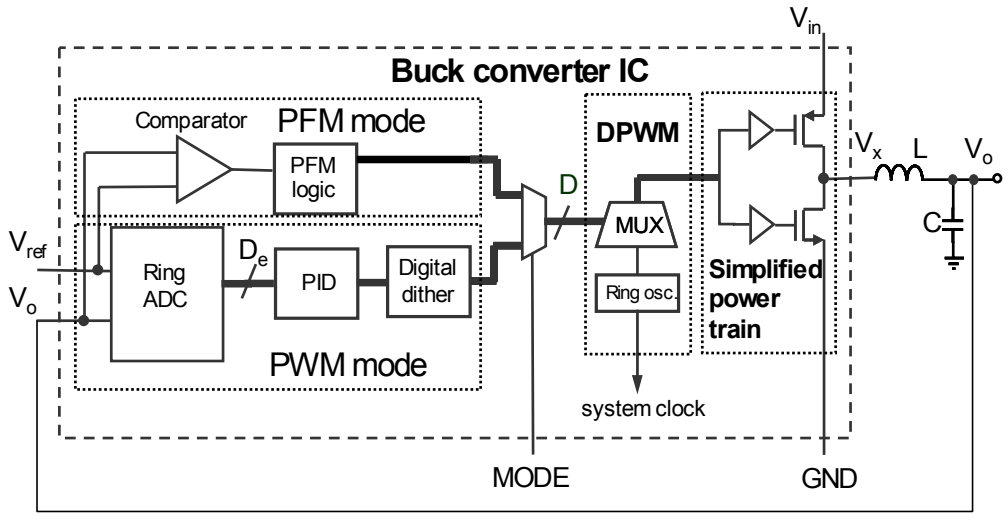


Fig. 1. Block diagram of dual-mode buck converter IC and external LC filter.

presented in Section III. The DPWM runs in both PWM and PFM modes, thus low power is a primary design objective for this block. A very low power DPWM scheme based on a ring oscillator-multiplexer structure (ring-MUX DPWM) is developed, the details of which are presented in section IV.

A prototype IC takes 2 mm^2 active area in a 0.25-μm CMOS process. With a cascode power train and internal power management, the IC demonstrates safe operation of a standard CMOS process rated for 2.75 V with a 5.5 V supply. The power train on the chip is rated for 400 mA load current, and efficiency above 90% is achieved for a load range of approximately 50-300 mA under PWM operation. Efficiency above 70% is achieved over the load range of 0.1-400 mA in PFM mode. The latter result is enabled by a 4 μA quiescent current in PFM mode. Further experimental results are detailed in section V.

II. Architecture and Voltage Compatibility

A. PWM Mode

The PWM mode runs the converter in continuous conduction. As shown in Fig. 1, in PWM mode, the error voltage $v_e = V_o - V_{ref}$ is quantized by the ADC to provide an error signal in the digital domain D_e, and the digital PID compensation network generates a duty ratio command D. The DPWM converts the duty ratio command into a PWM signal that controls the high side and the low side switches.

Subharmonic limit cycles may occur in a digitally controlled dc-dc converter because of the presence of two quantization operations, one in the ADC and one in the DPWM. Sufficient conditions to avoid subharmonic limit cycles are given in [1]. One step to avoid subharmonic limit cycles is the use a modulator (DPWM) that has higher resolution (smaller digital bin size) than that of the ADC. To meet this limit cycle avoidance condition, as well as the dc voltage precision specifications, the ADC quantization step size is designed to be 16 mV, and the DPWM step size is designed to be 5.4 mV. We note that this is one convenient design choice, but that substantially smaller step sizes can be readily implemented with the technology at hand.

A digital dither method that effectively reduces the DPWM hardware requirement, while keeping the same output resolution is employed [1]. With this method, 10-bit output resolution is achieved with a 5-bit hardware DPWM and

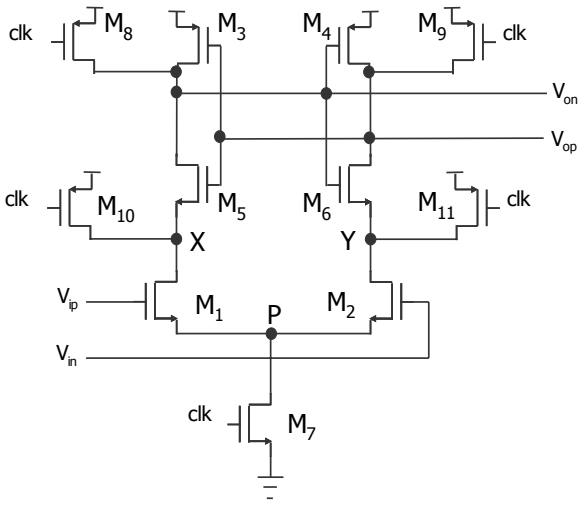


Fig. 2. Zero-bias-current comparator.

a 5-bit digital dither modulation process. The DPWM is implemented with a very low power ring oscillator-MUX structure reported in [2]. The ring oscillator in the DPWM runs at the switching frequency f_s, and provides clock signals for the whole system. Thus, high modulation resolution is obtained without any high frequency clock. The digital dither modulation provides very fine scale resolution of an additional five bits, by modulating the pattern for the hardware LSB over a 32 clock cycle period [1].

B. PFM Mode

The PFM mode runs the converter in discontinuous conduction mode with variable switching frequency and fixed on-time. Referring again to Fig. 1, a comparator samples the output voltage V_o at a fixed frequency $f_{samp,PFM}$ and compares it to the reference V_{ref}. When $V_o < V_{ref}$, the controller generates a fixed-on-time pulse through the DPWM to charge up the output capacitor. Otherwise, the converter and the controller are idling. The switching frequency in PFM mode scales roughly proportionally to the load current, thus the switching loss is greatly reduced in light load conditions. Thus, PFM mode enables high efficiency with ultra-light loads, and is ideal to control the converter in standby mode.

The PFM mode quiescent power is the fundamental limitation on ultra-light load efficiency. To reduce it, a clocked zero-dc-current comparator [3] is used, as shown in Fig. 2. When the clock signal clk is high, the comparator is in reset mode. Nodes V_{op}, V_{on}, X and Y of the comparator are precharged to supply voltage by $M_8 - M_{11}$, and node P is discharged to ground by M_7. When clk goes low, the comparator goes into evaluation and regeneration mode. Input pair M_1 and M_2 resolves the input voltage, and the differential current develops a voltage difference between nodes X and Y before the cross-coupled latch turns on. Then, the latch transistors $M_3 - M_6$ regenerate the amplified output signal back to full swing. After the output signals are fully regenerated, the cross-coupled inverter pair holds the logic levels without taking any power. Very low power is consumed by this comparator since only dynamic current flows through the input pair and the regeneration pair during the evaluation transient, and once the output signals are fully established, there is no dc current flowing in the comparator.

C. Voltage Compatibility and Internal Power Management

Small feature size processes with intrinsic low supply voltage are preferred to implement the digital circuit to achieve small die area, high speed and low power. A 0.25-μm CMOS process with highest allowable supply of 2.75 V is used to implement the IC. As mentioned in Section I, the battery in cellular phones supplies a voltage range between 5.5 V and 2.8 V. Thus, the circuit cannot run directly from the battery, and internal power management is introduced to ensure voltage compatibility.

As shown in Fig. 3, a cascode structure is used to protect the power train switches from high input voltage. An intermediate voltage $V_m = V_{in}/2$ is needed to bias the cascode transistors M_{P2} and M_{N2}, and to power the digital

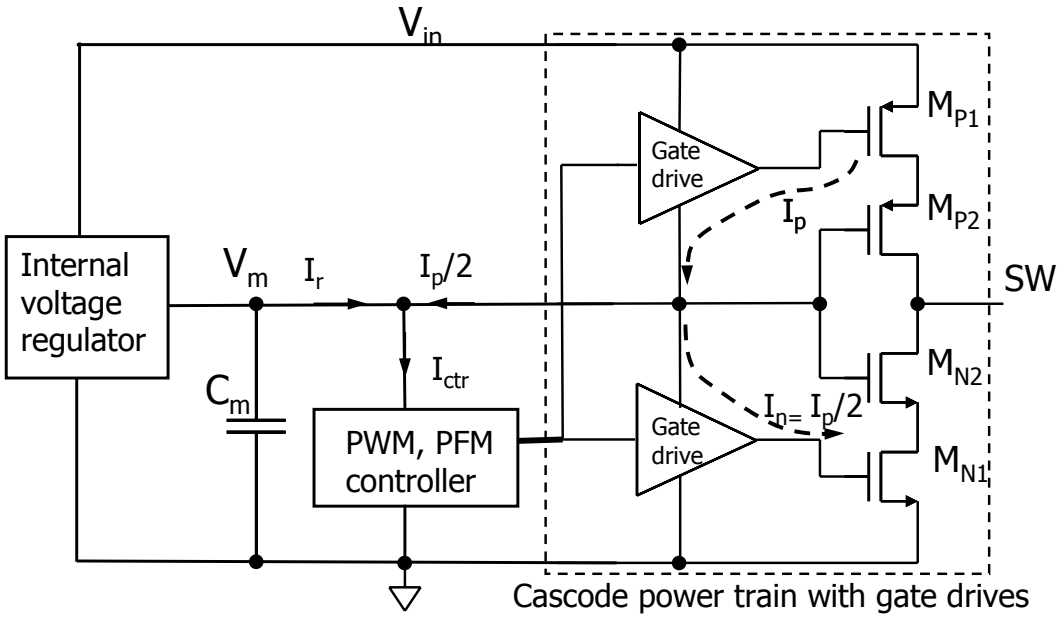


Fig. 3. Block diagram of internal power management.

circuits. A very low bias current internal class B regulator is used to provide a stable V_m.

The high side gate driver works between supplies V_{in} and V_m, and the low side gate driver works between V_m and ground. In each switching cycle, the average current I_p flowing into node V_m through the high side gate driver is approximately twice the current I_n flowing out of V_m through low side gate driver, since the power train PMOS transistor has twice the width of the NMOS transistor in this design to optimize conduction loss. The difference current $I_p - I_n$ can be used as a partial or complete supply for the controller. The total current consumed by the controller and the gate drivers can be calculated by summing the equivalent dc current that flows into the ground node. If the internal power management scheme were not employed, the resulting total current consumption would be $I_p + I_n + I_{ctr}$, where I_{ctr} is the equivalent dc current drawn by the controller. With the internal power management scheme, the overall current consumption reduces to $I_n + I_{ctr}$. The dc bias current

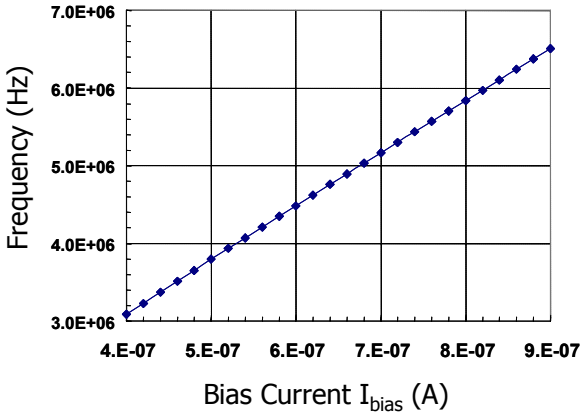


Fig. 4. Simulated frequency-current dependency of a 4-stage differential ring oscillator biased in subthreshold region.

in the class B internal regulator is more than two orders of magnitude lower than I_{ctr} alone and is thus neglected. Therefore, a current savings of I_p is achieved in PWM mode by using the internal power management scheme.

III. Ring-oscillator ADC

In PWM mode, since V_o is regulated to be in the vicinity of V_{ref}, an ADC that can handle a rail-to-rail input is

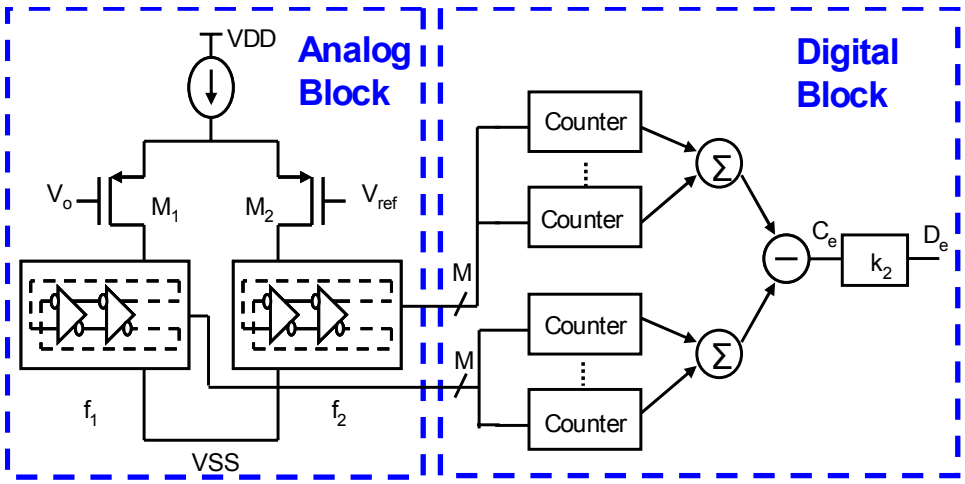


Fig. 5. Block diagram of ring-ADC.

not necessary, and a windowed ADC that realizes high resolution with reduced quantization range can be used [2], [4]. The main idea is to reduce the quantization window to the possible V_o variation range, which is usually tens of millivolts centered at V_{ref}. Due to switching activities of the power train, disturbances might be observed on V_o. Therefore, an averaging ADC that is insensitive to switching noise and has a windowed quantization range is desirable.

Synthesizable ADC's based on VCO or delay-line structures have been reported [5], [6]. In this work, we develop an averaging windowed ring-ADC which is nearly entirely synthesizable. Compared to the VCO or delay-line based ADC, the resolution of the developed ring-ADC is invariant under reference voltage changes, and can be flexibly adjusted to meet a wide range of applications.

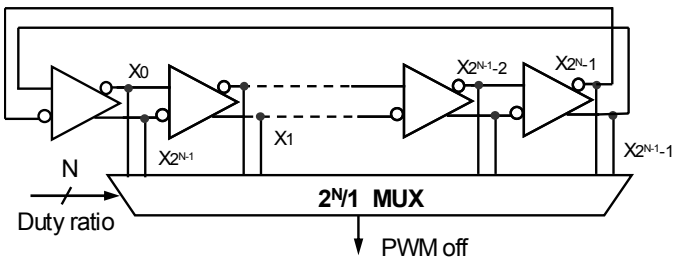
The design of the ring-ADC is based on the observation that the oscillation frequency in a CMOS ring oscillator, biased in subthreshold region, has a linear dependency on the bias current, as illustrated in Fig. 4. The block diagram of the ring-ADC is shown in Fig. 5. The ADC consists of a simple analog block and a synthesizable digital block. A differential transistor pair $M_1 - M_2$ drives two identical ring oscillators as a matched load. The bias current is such that the voltage swing on the ring oscillator is below threshold. Thus each ring oscillator's frequency is linearly dependent on its supply current. The error voltage v_e develops differential current in the two branches that results in instantaneous differential frequency at the two oscillators. The frequency of each oscillator is captured by a counter that is reset at the beginning of each sampling cycle. At the end of the cycle, one counter output is subtracted from the other, and the result C_e is used to calculate digitized error voltage D_e. Since there is uncertainty in the initial and ending phase, instead of looking at one output per ring, all the M taps on each ring oscillator are observed for frequency information. It can be shown that, ignoring quantization error and assuming good linearity in the input differential pair, C_e is given by

$$C_e = Mk_1 g_m T_{ADC} v_e, \tag{1}$$

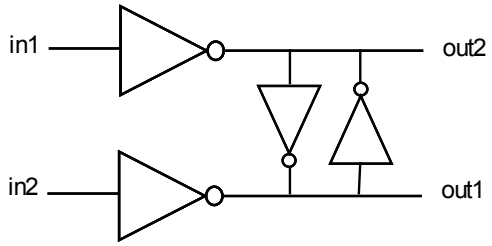
where M is the number of taps on each ring, k_1 is the ring oscillator frequency sensitivity function to bias current, g_m is the transconductance of the input differential pair, and T_{ADC} is the ADC sampling period, which equals the switching period T_s of the converter. Finally, digitized error voltage

D_e is calculated by rounding off C_e. Since the saturation behavior of the input differential pair is dependent on the ratio of the input signal and the overdrive voltage of the differential pair, good linearity of the input transistors can be obtained by designing the overdrive voltage a few times higher than the differential input voltage. Since v_e is usually less than 100 mV, the overdrive voltage needs to be only a few hundred millivolts.

In this design, a ring-ADC with 16 mV quantization bin size, and a total quantization window of 80 mV takes 0.15 mm^2 chip area. At 500 kHz sampling frequency, the measured current consumption of this ADC is 37 μA. The digital block can be further simplified by using a decoder and a counter, instead of a number of counters, to monitor the signals on all the taps in each ring, resulting in significantly smaller die area and much lower power consumption. Compared to ADC's based on a VCO or a delay-line, this ring-ADC has invariant resolution under different reference voltage levels due to the common mode rejection capability of the differential pair, thus is suitable for a wide range of applications. Furthermore, the resolution of the ring-ADC can be controlled through the bias current, which can be made either constant or adjusted for automatic gain control. For example, the bias current in the differential pair of the ring-ADC can be made a function inverse to the square of the input voltage. Thus when the input voltage reduces, the gain of the ADC increases, and hence the controller gain is also raised proportionally, resulting in a stabilized loop gain. In summary, the ring-ADC has low power and small area, and its resolution can be designed with high flexibility depending on application requirements. The quantization resolution of the ring-ADC can be scaled by changing the number of stages in the ring, and varying the bias current of the differential pair.



(a)



(b)

Fig. 6. (a) Block diagram of an N-bit ring-MUX DPWM, (b) the delay stage of the differential ring oscillator in the DPWM.

IV. RING-MUX DPWM

One method to digitally create PWM signals is with a fast-clocked counter-comparator scheme [7]. Such a design takes reasonable die area but the power consumption reported is on the order of mW's because of the high clock frequency in the counters [8]. A tapped delay line scheme is proposed in [9]. Power is significantly reduced with respect to the fast-counter-comparator scheme since the fast clock is replaced by a delay line which runs at the switching frequency of the converter. A combined delay-line-counter structure is reported in [5], [10], aiming to make a compromise between area and power.

A ring-oscillator-MUX implementation of a DPWM module, with block diagram shown in Fig. 6(a), has area and power considerations similar to those of the delay line approach. The ring oscillator runs with subthreshold voltage

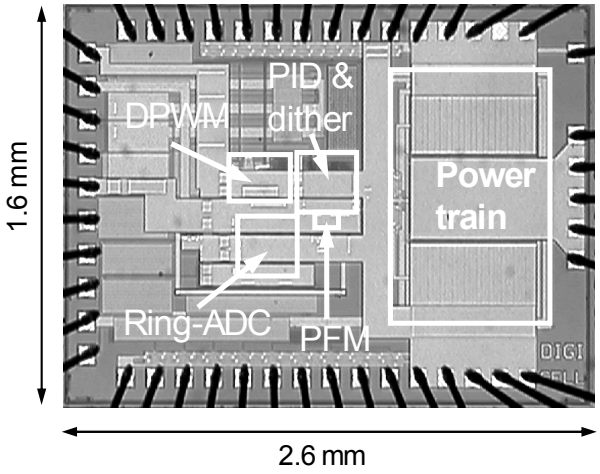


Fig. 7. Chip micrograph.

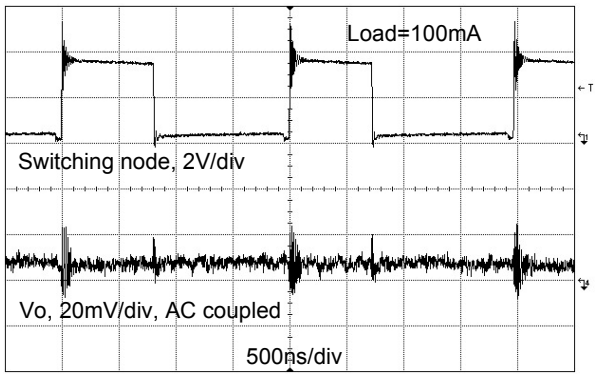


Fig. 9. Experimental steady-state response in PWM mode with V_{in} =3.2 V, V_o =1.2 V, and f_s =500 kHz.

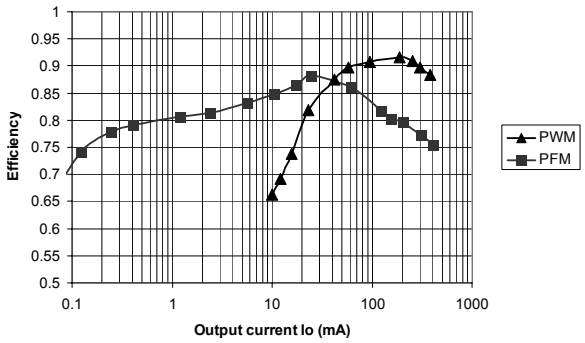


Fig. 10. Measured PWM and PFM mode converter efficiency as functions of output current, with V_{in} =4 V and V_o =1.5 V.

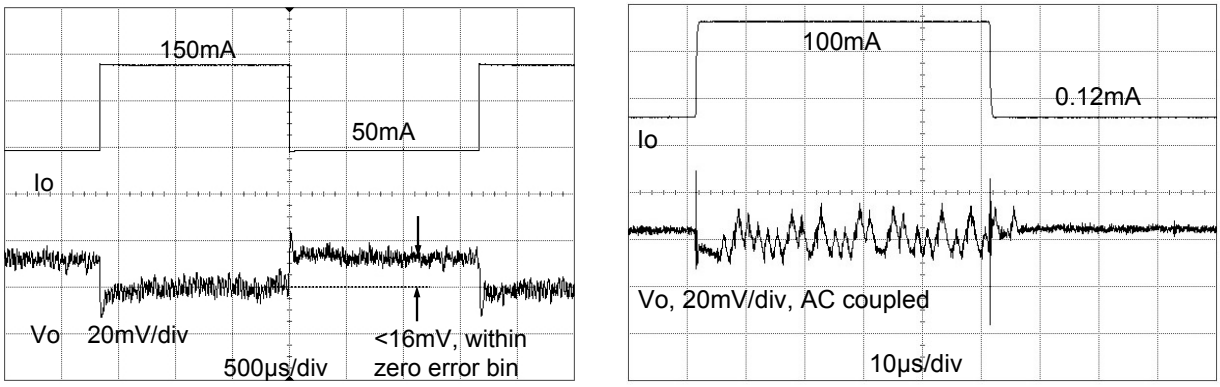
swing, thus the power consumption is much lower than the delay-line structure due to the reduced swing. Since the ring oscillator in the DPWM runs in current starved mode, the frequency can be controlled by adjusting the supply current to the entire ring. Thus the switching frequency of the converter can be locked to an external clock by controlling the DPWM ring current. The ring oscillator in the DPWM also generates the clock signals for the entire converter system.

The main components of the ring-MUX scheme are an N-stage differential ring oscillator, which yields 2N symmetrically oriented taps, and a 2N/1 MUX that can select appropriate signals from the ring. The delay stage in the differential ring oscillators in the DPWM is shown in Fig. 6(b). A square wave propagates along the ring. When the rising edge reaches tap X_0 in the ring, the rising edge of the PWM signal is generated. The falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified tap in the ring. The MUX is used to specify the tap in accord with the commanded duty cycle.

V. Experimental Results

The complete dual-mode digitally-controlled buck converter IC is implemented in a 0.25-μm CMOS process. The die photo of the chip is shown in Fig. 7. The total chip area is 4 mm^2, out of which 2 mm^2 is the active area. The required pin count for the buck converter IC is 10, and all the other pins are for test purposes. Table I summarizes the application and the measured performance of the IC.

Experimental closed-loop load transient responses with a current load step of 100 mA for PWM mode and PFM mode, respectively, are shown in Fig. 8. In PWM mode, it can be seen that the dc voltages at high load and low load are within the zero error bin of the ADC, which is 16 mV. In PFM



(a) (b)

Fig. 8. Experimental load transient response with V_{in} =3.2 V, V_o =1.2 V (a) PWM mode response with f_s =1 MHz, (b) PFM mode response with $f_{samp,PFM}$ =600 kHz.

TABLE I

CHIP PERFORMANCE SUMMARY.

Technology	0.25-μm CMOS (Max. supply 2.75 V)
Input voltage range	5.5-2.8 V
Output voltage range	1.0-1.8 V
External LC filter	L=10 μH, C=47 μF
Maximum load current	400 mA
PFM mode sampling frequency	600 kHz
PFM mode quiescent current	4 μA
PWM mode switching frequency	0.5-1.5 MHz
PWM mode dc output voltage precision	$\pm 0.8\%$
PWM mode output voltage ripple	2 mV
Active chip area	2 mm^2

mode, the voltage excursion is below 30 mV when the load current is 100 mA. Steady-state waveforms in PWM mode are shown in Fig. 9. Efficiencies as a function of load current of the buck converter in both PWM mode and PFM mode are measured with V_{in} =4 V and V_o =1.5 V, as illustrated in Fig. 10. An efficiency of 92% is achieved in PWM mode with load current of 189 mA. It can be observed that 40 mA is the crossover point of the PWM and the PFM efficiency curves. Thus, when load current is lower than 40 mA, the converter should be switched from PWM to PFM mode for better efficiency. Furthermore, over a 20 mA to 200 mA load current range, high efficiency (over 80%) can be observed in each mode, thus it is easy to implement a scheme to switch between the two modes due to the wide load range of overlapping high efficiency.

VI. Conclusion

This paper describes an ultra-low-quiescent-current dual-mode digital controller IC for high frequency dc-dc buck converters. Internal power management and power switch structures enable the use of a small feature size (0.25-μm) CMOS process with voltages up to 5.5 V. The paper further demonstrates sub-threshold operation of CMOS transistors as a viable, very low power option for analog-digital interface elements. The work illustrates the promise of implementing digital power management IC's in standard CMOS processes, with low power and small area, using a combination of digital processing and special purpose analog-digital interface structures.

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