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An ultra-low power successive approximation A/D converter with time–domain comparator

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Abstract This paper presents an ultra-low power successive approximation analog-to-digital converter. An improved implementation of the binary weighted capacitors array and a novel comparator that operates in the time instead of the voltage domain are effective and power efficient. The circuit, fabricated in a conventional 0.18-μm CMOS technology, achieves a sampling rate of 100 kS/s and an effective number of bit of 9.4. Using a 1-V supply voltage, the achieved power consumption is 3.8 μW, leading to a Figure of Merit as low as 56 fJ/conversion-level.

Keywords Analog-digital conversion · SAR · Low-power

1 Introduction

In energy-limited applications, such as wireless sensor networks and portable instruments, the use of ultra-low power analog-to-digital converters (ADCs) is crucial to enable autonomous operation. The successive approximation (SA) algorithm achieves low-power consumption, especially when the input signal bandwidth is up to about 1 MHz and provides medium resolutions (10–12 bit). A SA ADC typically consists of a comparator, a subtracting DAC, and the successive approximation register (SAR) [1–7]. The conversion starts with the sampling of the input signal and requires one clock period per bit. Therefore, the sampling rate is lower than the clock rate by a factor at least equal to (N + 1), N being the resolution of the ADC. The dominant sources of power dissipation in a SA ADC are the comparator, the SA logic, and the switching of the capacitor array.

This paper presents an ultra-low power SA ADC working at a sampling rate of 100 kS/s. The circuit, fabricated in a conventional 0.18-μm CMOS process, achieves an effective number of bits (ENoB) equal to 9.4 and consumes only 3.8 μW from a 1-V power supply. The low power consumption is achieved by optimizing the subtraction DAC and the input sampling. In addition, the circuit uses a novel comparator, named time–domain comparator, which, instead of operating in the voltage domain, transforms the input and the reference voltages into pulses and compares their duration. The comparator operates with less than 1 μA at 1-V supply with 0.2-mV sensitivity and a clock frequency of 1.4 MHz.

Section 2 describes the ADC architecture and discusses design strategies for ultra-low power. The section focuses on the improved binary weighted capacitor array with attenuation capacitor and on the novel time–domain comparator. Section 3 shows experimental results and compares the proposed converter with other state-of-the-art ADCs. Finally, Sect. 4 draws some conclusions.

2 ADC architecture

Even if the SA ADC topology is a very good candidate for obtaining ultra-low power consumption, the design of medium resolutions (10–12 bit) converters with very low Figure of Merit (FoM) is quite challenging and definitely not straightforward. The designer must account for the kT/C noise limit, the matching accuracy of the DAC elements,

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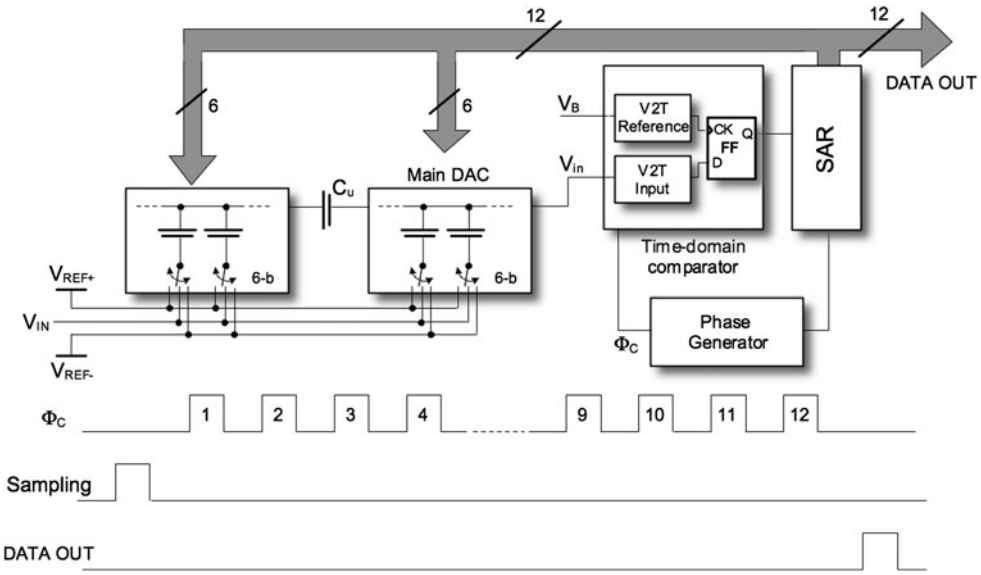

Fig. 1 SA A/D converter block diagram

and the effect of parasitics. Recently, methods that recycle the power consumed by the capacitive DAC have been proposed [8]. They are not used here, but can be obviously applied to obtain a further improvement of the power efficiency. The presented 12b SA ADC architecture, shown in Fig. 1, uses a capacitive split-array consisting of a 6b main array, a 6b sub-array and a unity coupling capacitor. Moreover, this design uses a time–domain comparator. The SAR logic is optimized for minimum power consumption. The conversion requires 14 clock periods of the main clock: the first for the input sampling, 12 periods for the SA cycles and the last period for end of conversion and data transfer.

2.1 Time–domain comparator

With an input voltage range of 0.8 V and the target resolution (12 bit), the LSB of the proposed ADC is less than 200 μV. Montecarlo simulations results, performed with the used technology, show that, to avoid latching errors, the input differential signal of a conventional latch circuit should be at least 15 mV. Therefore, a preamplifier with about 40-dB gain is necessary. The conventional scheme used is shown in Fig. 2. In order to minimize the power consumption, the transconductance is kept at the minimum. Therefore, instead of the DC gain $g_m r_0$, the designers use the dynamic gain

$$\frac{V_o}{V_{in}} = \frac{g_m T_p}{C_p}, \tag{1}$$

where T_p and C_p are the preamplification time and the output node parasitic capacitance, respectively, which has to be at least 77 (about 38 dB). Assuming the input transistors in weak inversion, (1) becomes

$$\frac{V_o}{V_{in}} = \frac{I_B T_p}{2mV_T C_p}, \tag{2}$$

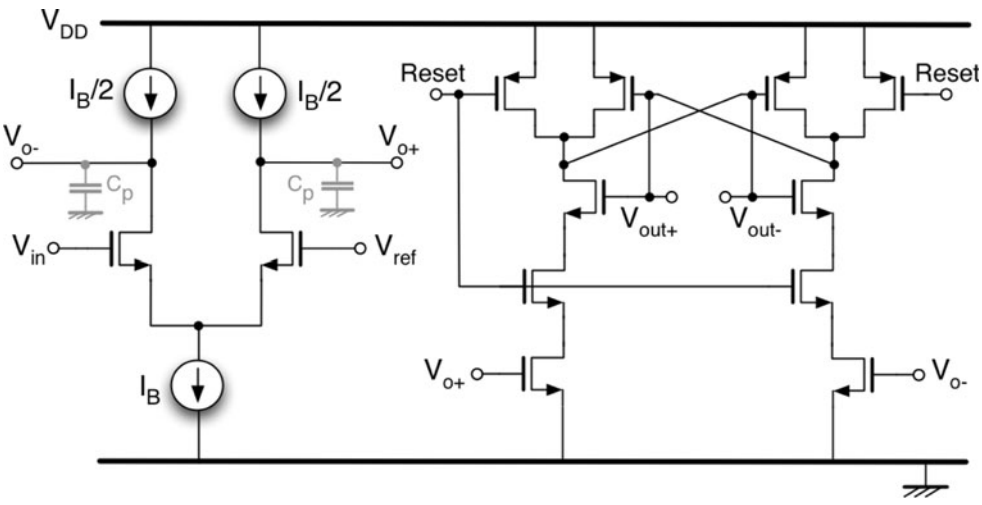

Fig. 2 Conventional voltage comparator made by a preamplifier and a latch

where $I_B/2$, m, and V_T are the input transistor bias current, the slope factor, and the thermal voltage, respectively.

Equation 2 provides an estimation of the consumed power for the expected speed of this design. The sampling rate is 100 kHz and the clock frequency is 1.4 MHz. Therefore, assuming to use half clock period for pre-amplification, $T_p = 357$ ns. Assuming $m = 1.75$, $C_p = 40$ fF, a differential dynamic gain of 43 dB, which allows a robust design margin, we achieve a preamplifier bias current of 1.44 μA. The power consumption is 1.44 μW, with 1-V supply. However, simulations that account for the effects of parasitics with the used 0.18-μm CMOS technology show a power consumption of the preamplifier and of the latch equal to 2.15 and 0.7 μW, respectively, leading to an overall power consumption of 2.85 μW.

As an alternative to the conventional solution described above, this paper uses a novel time–domain comparator. Figure 3 shows the circuit schematic of the voltage-to-time (V2T) cell. When Φ_C is low, transistor M_1 charges capacitor C_1. In the meantime, transistor M_4 discharges the parasitic capacitor C_{par} to cancel out any memory of the previous conversion. When Φ_C rises, transistor M_2 turns on and the current generator, consisting of M_5 and R_D, discharges C_1 at constant rate. The input voltage V_{in} establishes a current through R_D, equal to V_1/R_D. At time T_1, when the voltage across C_1, V_{C1}, crosses the threshold of M_3, signal Out_{V2T} rises. Figure 4 shows the V2T voltage signals. T_1 increases when the input voltage diminishes and vice-versa. Moreover, since the parasitic capacitor C_{par} is discharged by M_4, at the beginning of the comparison phase, it removes some charge from C_1, being connected in parallel to C_1. Therefore, V_{C1} immediately falls to

$$V_{CF} = V_{DD}\frac{C_{par}}{C_1 + C_{par}}. \tag{3}$$

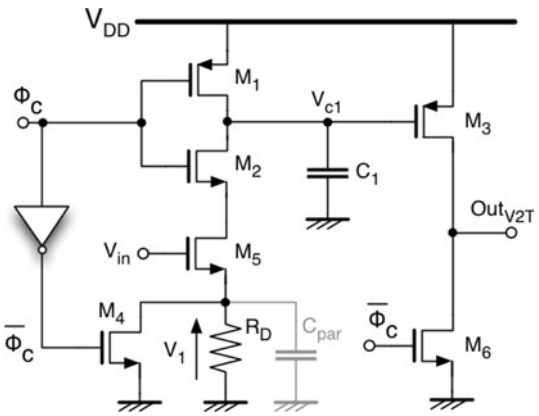

Fig. 3 Schematic diagram of the proposed V2T cell

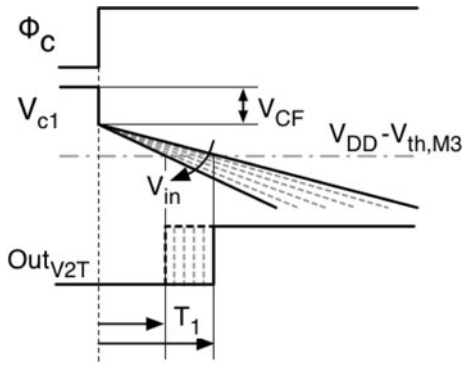

Fig. 4 V2T cell main signals

The initial drop of V_{C1} is positive because it reduces T_1 without increasing the discharge current.

Figure 5 shows the complete schematic diagram of the time–domain comparator. Two V2T cells process the input voltage and the voltage reference. The delay flip-flop (FFD) reveals the pulse that ends first and provides the comparator output.

The components sizing of the V2T cells depends on the period of time available for comparison and the accuracy. Two factors influence the time accuracy: the kT/C noise voltage across C_1 and C_2, and the latch plus jitter time error ΔT.

The switching-off of M_1 and M_7 causes a noisy difference between V_{C1} and V_{C2} equal to $\sqrt{(2kT/C)}$, being $C_1 = C_2 = C$. This error is equivalent to an input error $\varepsilon_{v,thermal}$ that changes the discharge current by

$$\delta I_D = \frac{\varepsilon_{v,thermal}}{R_D}. \tag{4}$$

The error $\sqrt{(2kT/C)}$ causes a time error of

$$\delta t_{thermal} = \frac{C\sqrt{\frac{2kT}{C}}}{I_D}, \tag{5}$$

where $I_D = V_1/R_D$.

The equivalent input error leads to

$$\delta t_\varepsilon = \frac{\delta I_D}{I_D}\frac{CV_{th,3}}{I_D}. \tag{6}$$

Combining (4), (5), and (6), we obtain

$$\varepsilon_{v,thermal} = \sqrt{2\frac{kT}{C}}\frac{V_1}{V_{th,3}} = \frac{\sqrt{2\frac{kT}{C}}}{G_N} \tag{7}$$

that determines a condition on the value of C.

The time error ΔT is equivalent to an input error, obtained by the use of Eq. 6. It results

$$\varepsilon_{v,\Delta t} = \frac{\Delta T}{R_D C}\frac{V_1}{V_{th,3}}V_1. \tag{8}$$

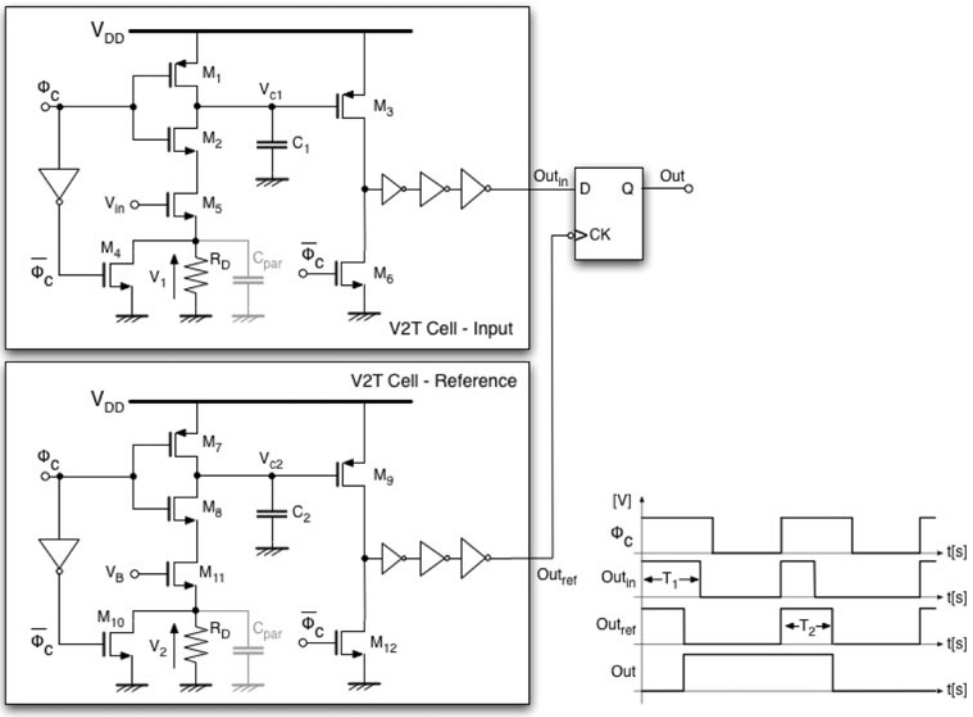

Fig. 5 Schematic diagram of the time–domain comparator

2.2 Capacitive array

The binary weighted capacitor array can be made by 2^N unity elements (Fig. 6) or by two sub-arrays with an attenuation capacitance between the arrays (Fig. 7). Typically, the two sub-arrays serve for the conversion of an equal number of elements. Therefore, for 12-bit, each sub-array uses 64 unity elements. A further segmentation of the resolution with three sub-arrays is not practical because of the difficulties in realizing the attenuating capacitors.

The value of the unity capacitor is determined by two conditions: the kT/C noise and the matching accuracy. The sampling of the input signal over the array or the sub-arrays (N/2 + N/2) gives rise to a noise power equal to

$$V_n^2 = \frac{kT}{2^N C_U} \tag{9}$$

or

$$V_n^2 = \frac{kT}{2^{N/2} C_U}. \tag{10}$$

The noise must be lower than the quantization noise $\Delta^2/12$. Therefore, the value of C_U must satisfy

$$C_U > \frac{12kT}{V_R^2} 2^{2N-N/2}. \tag{11}$$

Remind that the binary weighted capacitive DAC is not intrinsically monotonic. The worst situation is at the mid-point of the dynamic range where the DNL caused by the random mismatch between capacitors $C_U/\overline{C_U} = (1 + \varepsilon_c)$ is

$$DNL \approx \varepsilon_c 2^{3N/4}. \tag{12}$$

The above equation accounts for the switching of two arrays of $32C_U$ and $(31 + 63/64)C_U$ whose error is assumed $\varepsilon_c\sqrt{32}$, being errors quadratically combined. Since $\varepsilon_c = k_c/\sqrt{(WL)}$, Eq. 12 determines the minimum area of the unity capacitance.

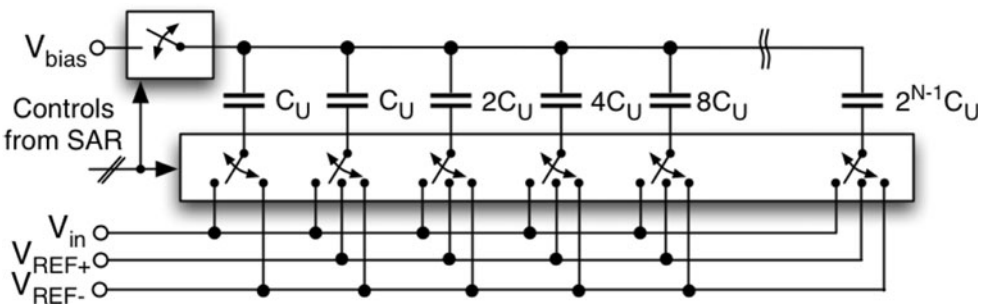

Fig. 6 Binary weighted capacitors array

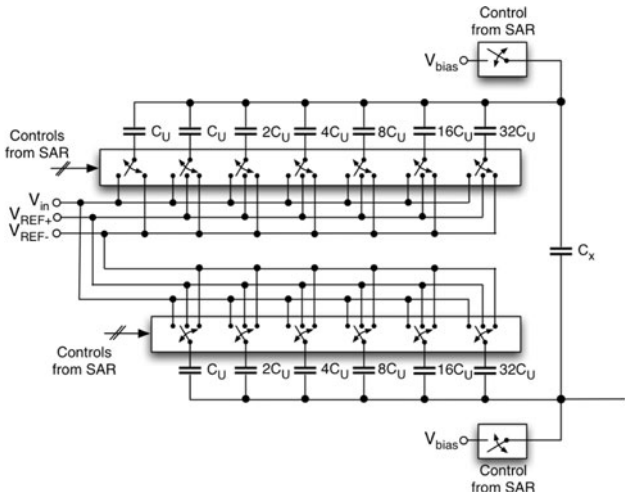

Fig. 7 Binary capacitors array with attenuation capacitor (N = 12)

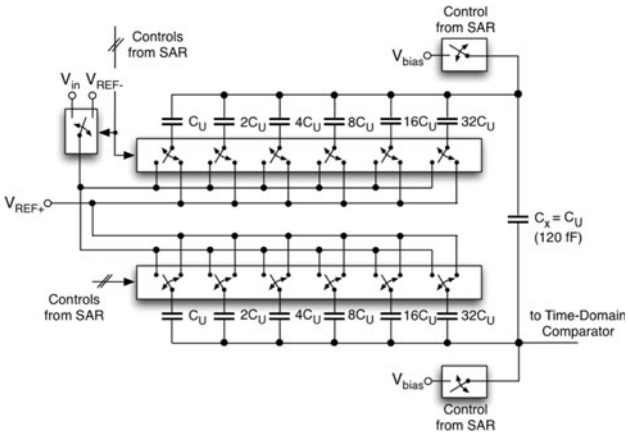

Fig. 8 Proposed split-capacitive array

As known, the attenuation capacitor C_x used between the two sub-arrays of Fig. 7 is not unity:

$$C_x = \frac{2^{N/2}}{2^{N/2}-1} C_U. \tag{13}$$

The way used here to avoid the limit is to remove a capacitor from the LSB sub-array and to use a unity capacitor as an attenuating element. The result is shown in Fig. 8. By inspection of the circuit, assuming and that k_1 and k_2 elements of the LSB and MSB sub-arrays, respectively, are connected to V_{REF+}, the voltage generated by the DAC (N = 12) turns out to be equal to

$$V_{DAC} = V_{REF-} + (V_{REF+} - V_{REF-}) \frac{k_1 + 64k_2}{63 \cdot 64 + 63}. \tag{14}$$

The full scale ($k_1 = k_2 = 63$) is $V_R = V_{REF+} - V_{REF-}$ instead of $V_R 2^N/(2^N - 1)$. Equation 14 verifies that the error is equally distributed between the quantization intervals of the DAC and, instead of causing INL, the error leads to a 1-LSB gain error, negligible with respect to the error on the reference voltages. This result is an improvement of the technique proposed in [2].

3 Circuit design

The critical issues in the circuit implementation are the design of the V2T cell and the unity capacitance sizing. In the proposed V2T cell (Fig. 5), $R_D C_1 = 0.1$ µs, $V_{th,3} = 0.4$ V and $V_1 = 0.15$ V. Considering $C_1 = C_2 = 0.8$ pF, Eqs. 7 and 8 give $\varepsilon_{v,thermal} = 38$ µV and $\varepsilon_{v,\Delta t} = 73$ µV, respectively. Moreover, the equivalent noise generator of M_3, $V_{n,3}$, is referred to the input multiplied by $V_1/V_{th,3}$ and is estimated equal to 90 µV. Summing up quadratically the three contributions on the two channels leads to an overall noise voltage of 172 µV. The value used for resistors R_D is 125 kΩ

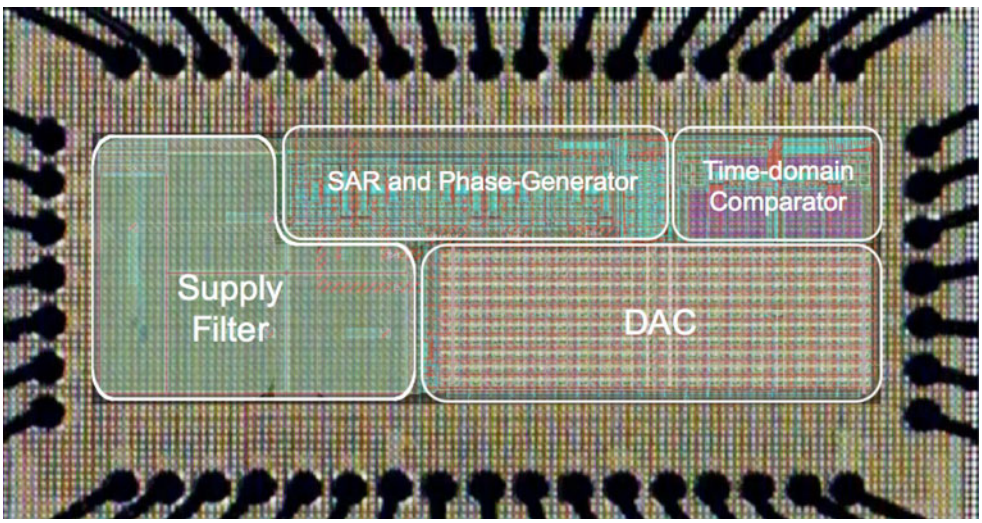

Fig. 9 Chip microphotograph

so that the discharge current flowing in the reference branch is 1.2 μA, flowing with 50% duty cycle. The time required to discharge 0.8 pF by 0.4 V with a 1.2-μA constant current is 0.267 μs. Therefore, the maximum usable clock is 1.87 MHz. However, to have margin for possible errors, this design uses, as mentioned, $f_{CK} = 1.4$ MHz.

The power consumed to charge and discharge C_1 depends on the successive-approximation sequence at the gate of M_5. If that voltage is much higher than V_B, then C_1 is fully discharged; if the gate voltage of M_5 is much lower than V_B, the capacitance C_1 remains charged to V_{DD}. Therefore, the consumed energy is $C_1V_{DD}^2$ or zero. Assuming that the number of ones is equal in average to the number of zeros, the energy per conversion is $NC_1V_{DD}^2/2$. With $N = 12$, $V_{DD} = 1$ V and $f_s = 1/T_s = 100$ kS/s, the current consumption is 0.48 μA. It is worth noting that the overall estimated power consumption of the proposed time–domain comparator (about 1 μW) is much lower than the conventional counterpart (about 2.85 μW).

Referring to the capacitive array of Fig. 8, it is assumed that the supply voltage of the converter can range from 0.8 to 1.8 V and that the reference voltage is $0.8V_{DD}$. Therefore, in the worst case, Eq. 11 gives $C_U > 1$ fF. The value of k_c for the used technology is 0.0038. Therefore, requiring to have a DNL = 0.5 at 3σ, the area of the unity capacitance becomes 120 μm^2. Since the specific capacitance is 0.97 fF/μm^2, the corresponding value of C_U is 120 fF. Complementary *n*–*p* pairs with W/L of 1/0.18 μm and 2/0.18 μm, respectively, and dummy transistors with half width are used to implement the switches used for each unity capacitance. The switching array and the charging and discharging of capacitor, with 1-V supply and 1.4-MHz clock, require a power of about 0.5 μW.

The logic circuits that store the sequence of the comparator outputs during each conversion and that realize the SA algorithm are full-custom designed in order to minimize the power consumption. The SAR including the phase generator (Fig. 1) uses 870 equivalent gates and consumes 1.4 μW at 1.4-MHz clock frequency, when considering a power supply of 1 V. Therefore, summing up the contributions of time–domain comparator, capacitive array and logic, the estimated power consumption at $V_{DD} = 1$ V is about 3 μW.

4 Measurement results

The proposed SA ADC was fabricated in a 0.18-μm two-poly five-metals CMOS process. Figure 9 shows the chip microphotograph with layout on the background. To avoid interferences, a shield of metal 5 almost completely covers the active area. In Fig. 9 the position of main circuital blocks is highlighted. The core area is 0.24 mm^2 and the entire die area is 0.7 mm^2.

Figure 10 shows the low frequency differential nonlinearity (DNL) and integral nonlinearity (INL) for 10-bit and 12-bit output obtained by the histogram of 65536 points ($V_{DD} = 1$ V). The 3.2-mV mismatch in the comparator is corrected by an external trimming of V_B (with V_{bias} at 0.54 V).

Figure 11 shows the FFT of the output with 0 dB_{FS} sine waves at 2.8 and 43.8 kHz. The main clock frequency is 1.4 MHz (100 kS/s). The single ended configuration is the source of the second harmonic distortion that dominates the SFDR: −71.8 dB at low frequency and −64.2 dB near the Nyquist frequency, as shown in Fig. 12. The SNDR at Nyquist drops by 1.7 dB with a loss of 0.3-bit with respect to its low frequency value (58 dB, equivalent to an effective number of bit equal to 9.4). The loss of SNDR is likely due to noise coming from the substrate and references and a relatively poor PSRR. Larger distortion at higher frequency is due to a relatively high non-linear on-resistance of the switches connecting the capacitive arrays to V_{bias} (Fig. 8).

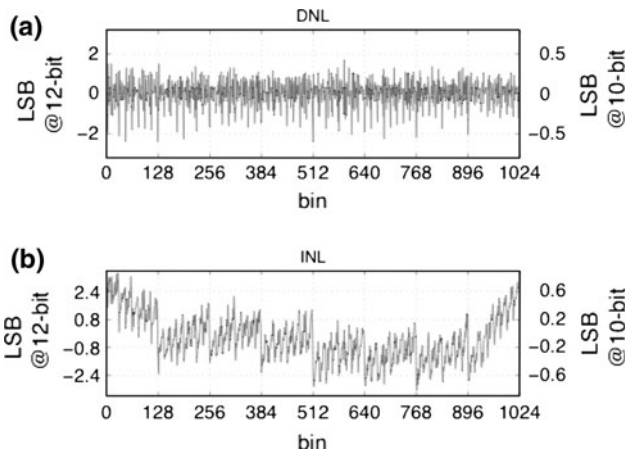

Fig. 10 Measured INL and DNL

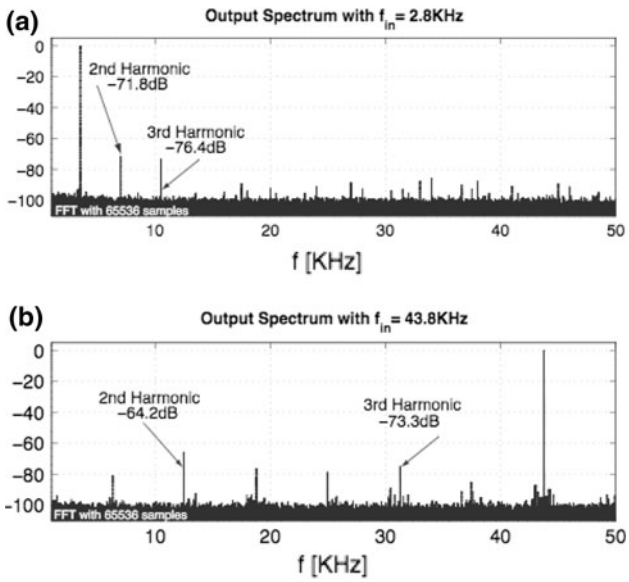

Fig. 11 Measured output spectrum

Table 1 Performance comparison

Work	[3]	[4]	[5]	[6]	[7]	This work [9]
Technology	0.18 μm	90 nm	0.18 μm	90 nm	0.18 μm	0.18 μm
Supply voltage	1 V	1 V	0.83 V	1 V	0.6 V	1 V
Sampling rate	100 kS/s	20 MS/s	111 kS/s	40 MS/s	100 kS/s	100 kS/s
ENoB	10.55	7.8	7.46	8.56	8.7	9.4
Power consumtion	25 μW	290 μW	1.16 μW	820 μW	1.3 μW	3.8 μW
FoM	167 fJ/c.-l.	65 fJ/c.-l.	60 fJ/c.-l.	54 fJ/c.-l.	31 fJ/c.-l.	56 fJ/c.-l.

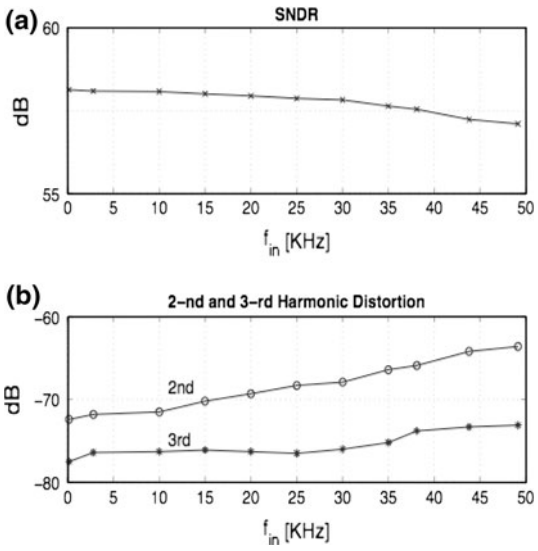

Fig. 12 SNDR, 2-nd and 3-rd harmonics as a function of the input signal frequency

The Figure of Merit (FoM) allows comparing different ADCs from an energy perspective. The FoM is defined as

$$\mathrm{FoM} = \frac{\mathrm{P}}{2^{\mathrm{ENoB}} 2\mathrm{BW}}, \tag{15}$$

where P and BW are the ADC power consumption and input signal bandwidth, respectively.

The measured power consumption is 3.8 μW when using a supply voltage of 1 V and 11.5 μW at 1.8 V. The increasing supply voltage improves the SNDR (at $V_{DD} =$ 1.8 V is 4.8 dB more), but the FoM worsens. The proposed circuit does not use buffers for reference voltages to keep at the minimum the power consumption. We obtain the best FoM, equal to 56 fJ/conversion-step, at $V_{DD} = 1$ V. Table 1 reports a performance comparison with previously published low-energy ADCs with similar technologies.

5 Conclusion

An ultra-low power SA ADC is presented. The circuit uses a novel time–domain comparator and an improved realization of the binary weighted capacitor array with attenuation capacitor. At 1-V supply voltage and sampling rate of 100 kS/s, the SA ADC achieves a peak SNDR of 58 dB, consuming 3.8 μW. This power consumption leads to the remarkable FoM of 56 fJ/conversion-level.

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