Open access • Journal Article • DOI:10.1109/TMTT.2009.2027079

An Ultra-Wideband High-Linearity CMOS Mixer With New Wideband Active Baluns

Pei-Zong Rao, Tang-Yuan Chang, Ching-Piao Liang, Shyh-Jong Chung

Institutions: National Chiao Tung University

Published on: 11 Aug 2009 - IEEE Transactions on Microwave Theory and Techniques (Institute of Electrical and Electronics Engineers Inc.)

Topics: Gilbert cell, Wideband, Balun, Cascode and Noise figure

An Ultra-Wideband High-Linearity CMOS Mixer With New Wideband Active Baluns

Pei-Zong Rao, Tang-Yuan Chang, Ching-Piao Liang, and Shyh-Jong Chung, *Senior Member, IEEE*

***Abstract*—A 2–11-GHz high linearity CMOS down-conversion mixer with wideband active baluns using 0.18-μm CMOS technology is demonstrated in this paper. The mixer employs a folded cascode Gilbert cell topology and on-chip broadband active baluns. The folded cascode approach is adopted to increase the output swing, and the linearity is enhanced by a harmonic distortion canceling technique derived from the harmonic balance analysis. The proposed configuration shows the highest IIP_3 and $\mathrm{IP}_{1\,\mathrm{dB}}$, and exhibits more compact size than most published studies. A broadband active balun is used to generate wideband differential signals, together with the derivation of a closed-form expression for the phase imbalance. This single-ended wideband mixer has the conversion gain of 6.9$\pm$1.5 dB, input 1-dB compression point $(\mathrm{IP}_{1\,\mathrm{dB}})$ of -3.5 dBm, single-sideband noise figure of 15.5 dB, and third-order input intercept point (IIP_3) of 6.5 dBm under the power consumption of 25.7 mW from a 1.8-V power supply. The chip area is 0.85×0.57 mm^2.**

***Index Terms*—Active baluns, CMOS, mixers, phase splitters, ultra-wideband (UWB).**

I. Introduction

THE MIXER, which is responsible for frequency conversion, is an essential building block of transceivers. It is also an important component associated with the linearity of the front-end receivers. The first stage of mixer must have high linearity to handle the large input signals from the low-noise amplifier (LNA) without significant intermodulation [1]. Nonlinearity will cause many problems such as cross modulation, desensitization, harmonic generation, and gain compression [2]. The differential architecture can be used to reduce the even-order nonlinearity, but it is difficult to suppress the odd-order one, especially for the third-order intermodulation distortion (IMD3), which is the dominant part of the odd-order nonlinearity.

The Gilbert cell is a typical type of active mixer. The Gilbert mixer consists of three stages: transconductor stage, switching stage, and load stage. The linearity of the Gilbert mixer will be dominated by the transconductor stage if the switching stage is ideal. Third-order input intercept point (IIP_3), second-order input intercept point (IIP_2), and input 1-dB compression point $(\mathrm{IP}_{1\,\mathrm{dB}})$ are the principal parameters of linearity. IIP_3 and IIP_2 are the effects of intermodulation terms in nonlinear circuits, and $\mathrm{IP}_{1\,\mathrm{dB}}$ is the ceiling of the input power. In order to improve the linearity of the Gilbert mixer, many methods have been used such as adding source degeneration resistors below the gain stage [3], using a bisymmetric class-AB input stage [1] and multiple gated transistor [2], and employing common-source and common-emitter RF transconductors [4].

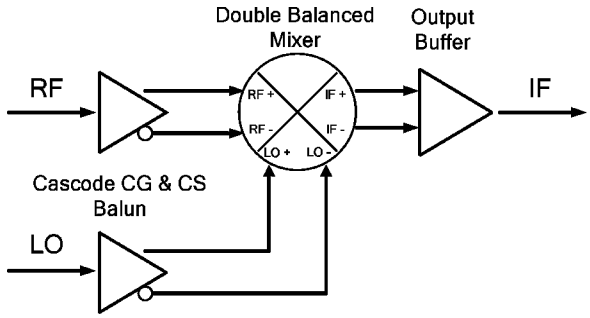

Fig. 1. Block diagram of the proposed mixer.

In order to get higher conversion gain, good isolation, and better dynamic and static offsets, and help improve the second- and third-order intermodulation rejection, the double-balanced Gilbert mixer with differential RF, local oscillator (LO), and IF signals are commonly used for optimum operation [5]–[6]. Differential balun (or phase splitter) circuits play an important role in generating differential output signals, which characterize balanced amplitude and phase. Here are two distinct types of baluns, i.e., passive and active baluns. In general, the passive baluns have the advantage of consuming no dc power, and they are often implemented in the forms of *LC* networks or microstrip line transformers. The *LC* network baluns can be used in narrowband and the microstrip line transformers in wideband applications. However, both of them are lossy and expansive for larger physical size at frequencies below X-band, which limit the practicability of the passive baluns in monolithic microwave integrated circuit (MMIC) designs. Conversely, the active baluns have the characteristics of more acceptable gain imbalance and phase imbalance in a wideband range. The compact size also makes the active baluns more suitable than passive baluns in integrated circuit designs.

Several types of active balun topologies have been proposed in the literature. Three configurations are commonly used: single field-effect transistor (FET) circuits, common-gate cascaded with common-source (CGCS) circuits, and differential amplifier circuits. The challenge of the active balun design is to maintain an 180° phase difference and limit gain imbalance between the two output ports in a wide frequency range. The common-source single-FET type is the simplest configuration

Manuscript received November 27, 2008; revised May 06, 2009. First published August 11, 2009; current version published September 04, 2009. This work was supported by the National Science Council of Taiwan under Contract NSC97-2221-E-009-040-MY2.

The authors are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: sjchung@cc.nctu.edu.tw).

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Digital Object Identifier 10.1109/TMTT.2009.2027079

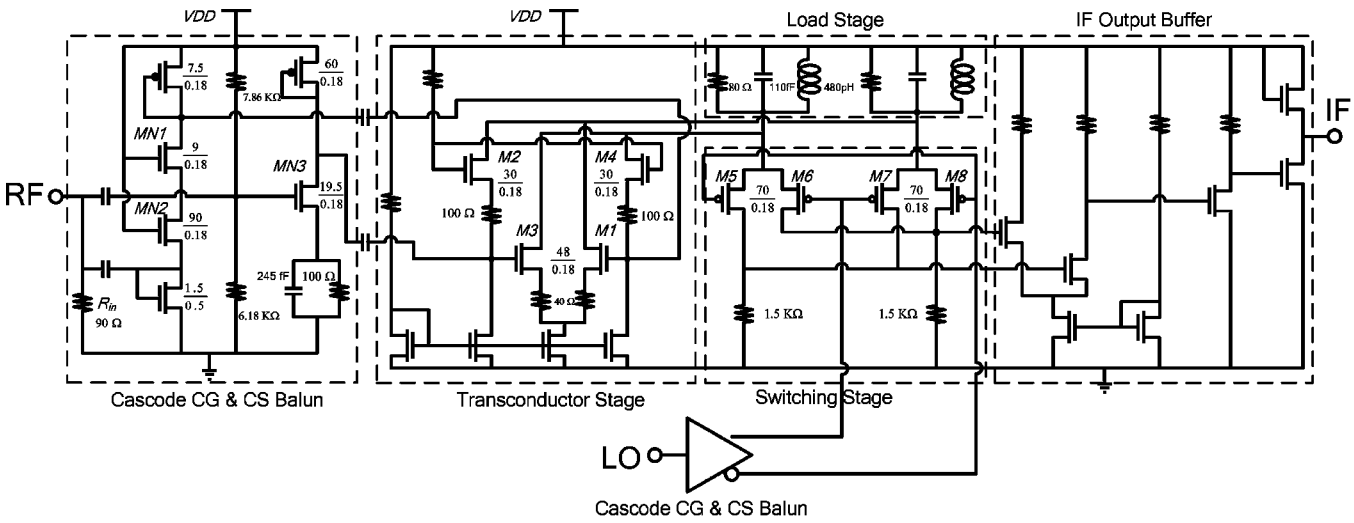

Fig. 2. Completed circuit schematic of the proposed mixer with wideband active baluns.

of active baluns. When signals enter the gate, ideally the output signals at the drain and source will be out of phase by 180° and have equal amplitude. However, the parasitic capacitance of the FET makes the common-source FET difficult to achieve the required phase difference for wideband and high-frequency application. Examples can be found in [7] and [8] with operation frequency lower than 2 GHz. As for the second configuration, the CGCS circuit, its characteristics are low power consumption and adequate isolation. However, it does not have low phase error performance in broadband applications due to the parasitic effects. An active phase splitter proposed in [9] adopted the common base/common emitter structure using the InGaP HBT foundry process, which exhibited a maximum amplitude error and a phase error up to 1.3 dB and 8°, respectively, at the personal communication system (PCS) frequency band (1850–1910 MHz).

For the third configuration, the differential amplifier balun circuit, the output signals are usually poor in equal amplitude and out-of-phase since the current source becomes an imperfect open circuit at the high frequency. The leakage signal to the current source will cause the phase and gain imbalances. The over-driven voltage of the differential amplifier will also decrease the headroom of the output signals. Viallon *et al.* [10] utilized this configuration to implement an active balun with a very wide frequency range from 0.2 to 22 GHz. The drawback of their design is the large power consumption up to 166 mW.

In this paper, we proposed a new high linearity down-conversion mixer with wideband active baluns by using the standard 0.18-μm CMOS process. Detailed design information is presented. The adopted cascode CG and CS active balun is improved from the CGCS structure for better performance at high-frequency and wideband applications. This paper is organized as follows. In Section II, the equations describing harmonic terms in the feedforward transconductor are first derived from which one observes that the high linearity can be achieved by canceling the harmonic distortion. A closed form of phase imbalance for the wideband active balun is then given with small-signal analysis. In Section III, the experimented results of the fabricated chip designed on the basis of the circuit simulations are presented and compared to other wideband mixers using the similar technology. Finally, Section IV gives a conclusion with a brief summary of the proposed mixer.

II. Circuit Design and Analysis

Fig. 1 illustrates the block diagram of the proposed mixer. It includes the mixer core (double-balanced mixer), two active baluns (modified CGCS baluns) for RF and LO ports, and an output buffer for the IF port. The mixer core uses the *LC* folded cascode topology with differential transconductor to improve the linearity. The active baluns also adopts the improved common gate that cascaded with common-source baluns to generate balanced RF and LO signals. The output buffer is a differential common-source amplifier for testing and matching purposes. All input/output ports are single ended so that the proposed mixer circuit can be directly combined with single-ended frond-end and back-end circuits.

A. Mixer Core

The completed circuit schematic of the high linearity mixer is shown in Fig. 2. The proposed mixer is based on a Gilbert cell mixer, which is composed of an LO switching stage $(M5$–$M8)$, an RF transconductor stage $(M1$–$M4)$, current mirrors, and IF buffer amplifiers.

The transconductor, as shown in Fig. 3, consists of two degenerate common-source transistors $(M1, M3)$ and two degenerate common-gate transistors $(M2, M4)$, which used to be the input stage and achieve feed-forward distortion linearization [11]. This feedforward compensated differential transconductor has the function of providing accurate input impedance and high intermodulation intercepts, and has less distortion than the class-AB [12], multi-tanh [13], degenerated differential pair, and cascode compensation [14]. R_1 and R_2, as will be described below, are used for suppressing the excited harmonics, and thus the nonlinearity, in the circuit. R_2 also serves for input matching purposes. Without input matching active baluns, a wideband mixer with a feedforward compensated differential transconductor in CMOS 0.18-μm technology was previously presented by the authors [15]. Although good

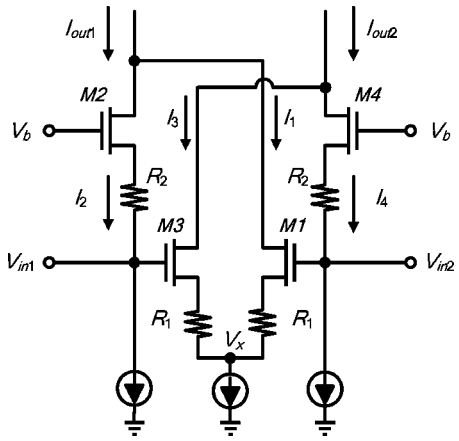

Fig. 3. Differential transconductor stage of the proposed mixer.

linearity was achieved, neither theoretical study, nor design formula was given there.

In order to analyze the nonlinear effects generated by the transconductor stage, the harmonic balance analysis started from the derivation of the output current. The output currents $I_{\rm out1}$ and $I_{\rm out2}$ of the differential transconductor stage characterize a nonlinear relationship with the input voltages $V_{\rm in1} = V_{\rm dc} + V_m \cos\omega t$ and $V_{\rm in2} = V_{\rm dc} - V_m \cos\omega t$, where $V_{\rm dc}$ is the dc-bias voltage of the input signals. The differential output current I_{od} can be written as

$$I_{od} = I_{\rm out1} - I_{\rm out2} = (I_1 + I_2) - (I_3 + I_4) \tag{1}$$

where I_1 to I_4 are the currents for transistors M_1 to M_4. In this study, the third-order harmonic distortion canceling technique is adopted for achieving high linearity. To this end, the cancellation criterion for wideband applications is first derived based on the harmonic balance analysis.

Assume that all the FETs in Fig. 3 are operated in the saturation region with channel length modulation parameter $\lambda = 0$. The currents I_1 and I_2 can be expressed as

$$I_1 = \frac{1}{2}K_1\left[V_{\rm dc} - V_m\cos\omega t - (I_1R_1 + V_x) - V_{\rm TH}\right]^2 \tag{2}$$

$$I_2 = \frac{1}{2}K_2\left[V_b - (I_2R_2 + V_{\rm dc} + V_m\cos\omega t) - V_{\rm TH}\right]^2 \tag{3}$$

where $V_{\rm TH}$ and V_b are the threshold voltage and bias voltage, respectively. The transconductance parameter K (= K_1 or K_2) is also given as

$$K = \mu_n C_{ox}\frac{W}{L}.$$

Reforming (2) and (3), one obtains

$$\begin{aligned} I_1 = {} & \left(\frac{2}{R_1^2K_1} - \frac{K_1V_{P1}^2}{2} + \frac{1}{2}R_1K_1^2V_{P1}^3 + \frac{2V_{P1}}{R_1} - \frac{1}{4}K_1V_m^2 \right. \\ & \left. + \frac{3}{4}R_1K_1^2V_{P1}V_m^2\right) \\ & + \left(-\frac{3}{2}R_1K_1^2V_{P1}^2V_m - \frac{3}{8}R_1K_1^2V_m^3 + K_1V_mV_{P1} \right. \\ & \left. - \frac{2V_m}{R_1}\right)\cos\omega t \\ & + \left(-\frac{1}{4}K_1V_m^2 + \frac{3}{4}R_1K_1^2V_{P1}V_m^2\right)\cos 2\omega t \\ & - \frac{1}{8}R_1K_1^2V_m^3\cos 3\omega t \end{aligned} \tag{4}$$

and

$$\begin{aligned} I_2 = {} & \left(\frac{K_2V_{P2}^2}{2} - \frac{1}{2}R_2K_2^2V_{P2}^3 + \frac{1}{4}K_2V_m^2 - \frac{3}{4}R_2K_2^2V_{P2}V_m^2\right) \\ & + \left(\frac{3}{2}R_2K_2^2V_mV_{P2}^2 + \frac{3}{8}R_2K_2^2V_m^3 - K_2V_mV_{P2}\right)\cos\omega t \\ & + \left(\frac{1}{4}K_2V_m^2 - \frac{3}{4}R_2K_2^2V_{P2}V_m^2\right)\cos 2\omega t \\ & + \frac{1}{8}R_2K_2^2V_m^3\cos 3\omega t \end{aligned} \tag{5}$$

where $V_{P1} = V_{\rm dc} - V_{\rm TH} - V_x$ and $V_{P2} = V_b - V_{\rm TH} - V_{\rm dc}$.

Similarly, the currents I_3 and I_4 for $M3$ and $M4$, respectively, can be derived as

$$\begin{aligned} I_3 = {} & \left(\frac{2}{R_1^2K_1} - \frac{K_1V_{P1}^2}{2} + \frac{1}{2}R_1K_1^2V_{P1}^3 + \frac{2V_{P1}}{R_1} - \frac{1}{4}K_1V_m^2 \right. \\ & \left. + \frac{3}{4}R_1K_1^2V_{P1}V_m^2\right) \\ & - \left(-\frac{3}{2}R_1K_1^2V_{P1}^2V_m - \frac{3}{8}R_1K_1^2V_m^3 + K_1V_{P1}V_m \right. \\ & \left. - \frac{2V_m}{R_1}\right)\cos\omega t \\ & + \left(-\frac{1}{4}K_1V_m^2 + \frac{3}{4}R_1K_1^2V_{P1}V_m^2\right)\cos 2\omega t \\ & + \frac{1}{8}R_1K_1^2V_m^3\cos 3\omega t \end{aligned} \tag{6}$$

and

$$\begin{aligned} I_4 = {} & \left(\frac{K_2V_{P2}^2}{2} - \frac{1}{2}R_2K_2^2V_{P2}^3 + \frac{1}{4}K_2V_m^2 - \frac{3}{4}R_2K_2^2V_{P2}V_m^2\right) \\ & - \left(\frac{3}{2}R_2K_2^2V_mV_{P2}^2 + \frac{3}{8}R_2K_2^2V_m^3 - K_2V_mV_{P2}\right)\cos\omega t \\ & + \left(\frac{1}{4}K_2V_m^2 - \frac{3}{4}R_2K_2^2V_{P2}V_m^2\right)\cos 2\omega t \\ & - \frac{1}{8}R_2K_2^2V_m^3\cos 3\omega t. \end{aligned} \tag{7}$$

Substituting (4)–(7) into (1), the differential output current I_{od} turns out to be

$$\begin{aligned} I_{od} &= I_{\rm out1} - I_{\rm out2} \\ &= (I_1 + I_2) - (I_3 + I_4) \\ &= A_F\cos\omega t + A_{HD3}\cos 3\omega t. \end{aligned} \tag{8}$$

where A_F and A_{HD3} represent the amplitudes of the fundamental and third-order harmonics, respectively. A_F and A_{HD3} can be found as

$$A_F = \frac{V_m}{4}\left[\begin{matrix} 8\left(K_1V_{P1} - K_2V_{P2}\right) + 3V_m^2\left(-R_1K_1^2 + R_2K_2^2\right) \\ +12\left(-R_1K_1^2V_{P1}^2 + R_2K_2^2V_{P2}^2\right) - \dfrac{16}{R_1} \end{matrix}\right] \tag{9}$$

$$A_{HD3} = \frac{V_m^3}{4}\left(-R_1K_1^2 + R_2K_2^2\right). \tag{10}$$

The even-order harmonic distortion is canceled due to the differential architecture. The third-order distortion is the dominant part of the nonlinearity, and it may induce problems like intermodulation, cross-modulation, desensitization, and gain compression. All these higher order distortions deteriorate the circuit linearity. The dc and second-order harmonics in (4)–(7) are canceled due to the differential architecture. It is seen from (10) that the amplitudes of the third-order harmonic A_{HD3} become null if it follows that

$$R_1K_1^2 = R_2K_2^2. \tag{11}$$

This means that the third-order distortion, which is the dominant part of the nonlinearity, can be eliminated if one designs the resistances R_1 and R_2 and the transconductance parameters K_1 and K_2 properly according to (11). The formula is proposed to provide design guidance for obtaining better linearity by canceling the third-order distortion. Based on the above criteria, the third-order harmonic of the differential output current becomes null. The fundamental amplitude can also be rewritten as follows:

$$A_F = \frac{V_m}{4}\Bigg[8\left(K_1V_{P1} - K_2V_{P2}\right) + 12\left(-R_1K_1^2V_{P1}^2 + R_2K_2^2V_{P2}^2\right) - \frac{16}{R_1}\Bigg]. \tag{12}$$

Formula (12) shows that the fundamental amplitude will enlarge when the resistor R_2 increases. However, with the unchanged transconductor parameter K, (11) indicates that R_1 should be increased at the same time to meet the criteria if R_2 is increased. Meanwhile, (12) shows that the increased R_1 will lessen the fundamental amplitude due to the term $\left(-R_1K_1^2V_{P1}^2\right)$ though the term $(-16/R_1)$ is enlarged. The method of increasing mixer gain at the same IP_3 point is to find out the maximum R_2 under the consideration of R_1 in (12). Hence, in an attempt to find out the maximum mixer gain, R_1 and R_2 should be well chosen and is a tradeoff.

However, the mixer gain is proportional to the transconductance g_m, and higher overdrive voltage will get higher gain. Furthermore, the level of the supply voltage for the feedforward compensated differential transconductor is critical to keep the driver FETs always operated in the saturation region. To overcome this problem, the *RLC* folded cascode circuit is used as the load to get larger output voltage headroom [2], [3], [16], [17]. Since the inductor is short circuited at dc operation, this modified *LC* folded load can still provide more voltage headroom for the output signal. The addition of the resistance in the *LC* tank helps to reduce the quality factor, and thus increase the bandwidth of the mixer.

In function, the differential signal get into the feedforward compensated differential transconductor for amplification first. The small-signal voltage is converted to a small-signal current at this stage. The current signal is then down-converted by the switching pair. Finally, the *RLC* tank provides loading to the preceding stages and converts the current signals back to the voltage signals.

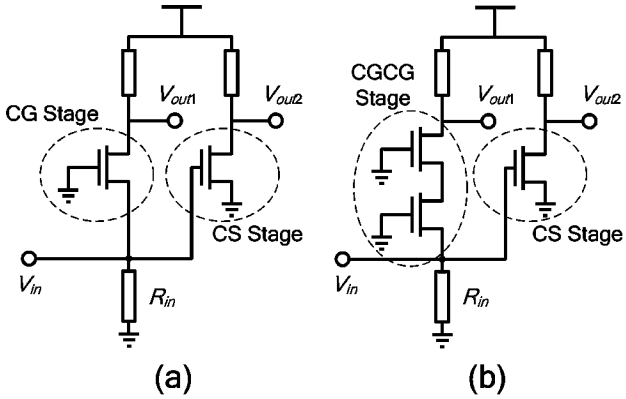

Fig. 4. Circuits of: (a) the conventional CGCS balun and (b) the cascode CG and CS balun.

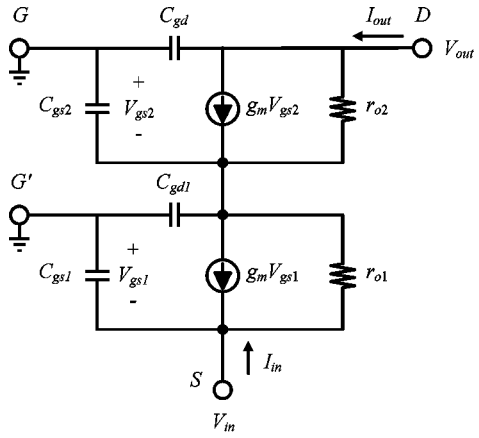

Fig. 5. Small-signal equivalent-circuit model of cascode common-gate stage.

B. Wideband Active Balun

In this section, the adopted cascode CG and CS active balun is analyzed and compared to the conventional CGCS one. As shown in Fig. 4(a), a conventional CGCS balun consists of common-gate and common-source stages, whose advantages are low power consumption and adequate isolation. However, it gets too much phase error for broadband application.

To meet the bandwidth requirement in this study, the active balun, as illustrated in Fig. 4(b), is used, which is modified from the CGCS circuit by replacing the CG stage into a cascode CG stage to improve the phase error of differential output. The resistance R_{in} is utilized for input matching to save the die area.

To demonstrate the superiority of the cascode CG and CS structure in wideband phase balance, the transmission phase $\angle S_{21}|_{\mathrm{CGCG}}$ (i.e., the phase of $V_{\mathrm{out}}/V_{\mathrm{in}}$) of the cascode CG structure is derived by using the small-signal equivalent circuit shown in Fig. 5. The transmission phases $\angle S_{21}|_{\mathrm{CS}}$ and $\angle S_{21}|_{\mathrm{CG}}$ for the conventional CS and CG stages are then derived from the corresponding small-signal circuits [18]. The results are shown,

respectively, in (13)–(15) at the bottom of this page, where

$$
\begin{aligned}
A =& \left\{1 + r_o\left(1+K\right)Z_0^{-1} + \left(1+g_m r_o\right)K \right.\\
&\left. - \omega^2 C_{\rm gs} r_o \left[C_{\rm gs}\left(Z_0 + r_o\right) + Z_0 C_{\rm gd}\left(2 + g_m r_o\right)\right]\right\}\\
&\times \left(g_m^2 + \omega^2 C_{\rm gs}^2\right)\\
B =& \left\{r_o\left(C_{\rm gs} + C_{\rm gs} r_o Z_0^{-1} + 2C_{\rm gd} + g_m r_o C_{\rm gd}\right)\right.\\
&+ \left(1+g_m r_o\right)\left[C_{\rm gs} Z_0 + Z_0 C_{\rm gd}\left(1+g_m r_o\right) + C_{\rm gs} r_o\right]\\
&\left. + C_{\rm gs}\left[Z_0 + r_o\left(1+K\right)\right]\right\}\left(g_m^2 + \omega^2 C_{\rm gs}^2\right)\\
C =& 2g_m^3 Z_0 + 2r_o g_m^3\left(1+K\right) + 2\omega^2 C_{\rm gs} r_o g_m^2\\
&\times \left(2Z_0 C_{\rm gd} + Z_0 C_{\rm gd} g_m r_o + C_{\rm gs} Z_0 + C_{\rm gs} r_o\right)\\
D =& 2g_m^2\left[g_m r_o\left(2Z_0 C_{\rm gd} + Z_0 C_{\rm gd} g_m r_o + C_{\rm gs} Z_0 + C_{\rm gs} r_o\right)\right.\\
&\left. - Z_0 C_{\rm gs} - r_o C_{\rm gs}\left(1+K\right)\right]\\
K =& 1 + g_m r_o - \omega^2 C_{\rm gs} C_{\rm gd} r_o Z_0.
\end{aligned}
$$

From the derived transmission phases, the phase imbalances for the conventional CGCS balun and the cascode CG and CS balun are obtained as follows:

$$
\begin{aligned}
&\text{Phase imbalance of conventional CGCS balun}\\
&\quad = \pi - \left|\angle S_{21}\right|_{\rm CS} - \angle S_{21}\left|_{\rm CG}\right| \qquad (16)\\
&\text{Phase imbalance of cascode CG and CS balun}\\
&\quad = \pi - \left|\angle S_{21}\right|_{\rm CS} - \angle S_{21}\left|_{\rm CGCG}\right|. \qquad (17)
\end{aligned}
$$

Fig. 6 depicts the calculation results for the two circuits. Here, the process parameters given by the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, with 0.18-μm CMOS technology are used (W/L $= 18.15/0.18$, $g_m = 8.9$ ms, $C_{\rm gs} = 18.4$ fF, $C_{\rm gd} = 6.02$ fF, $r_o = 301.5\ \Omega$). It is seen that, in the frequency range from 0 to 13 GHz, the phase imbalance of the conventional CGCS balun is varied from 0° to −10°, while that of the cascode CG and CS balun is from 0° to −2.2°. Obviously, the latter has better performance than the former.

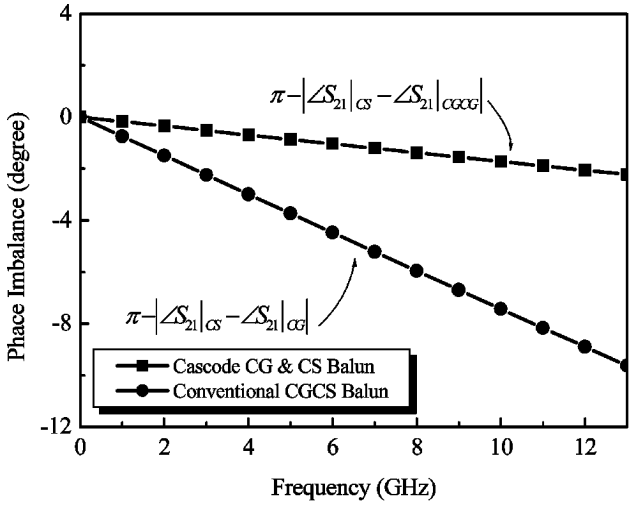

Fig. 6. Calculated phase imbalances of the conventional CGCS balun and cascode CG and CS balun in Fig. 4.

TABLE I
COMPARISON OF ACTIVE BALUNS

Ref.	this work*	[13]	[18]	[19]	[20]	[21]
Frequency (GHz)	2~13	0.2~22	0.5~10	0~8	1.7~5.8	5.1~5.9
Gain imbalance (dB)	2	0.5	0.5	2.7	2	0.02
Phase imbalance	4°	4°	5°	4.2°	2°	0.58°
$P_{dis.}$ (mW)	1.8	166	---	1.44	11.4	9.17

* For the simulation result of this work in Table I, the active balun is connected with the mixer core.

Table I summaries the performances of reported active baluns and this study. It is seen that the cascode CG and CS active balun

$$
\angle S_{21}\left|_{\rm CS}\right. = \tan^{-1}\left\{\frac{\omega\left[C_{\rm gd}\left(\frac{1}{r_o}+\frac{1}{Z_0}\right)+g_m(C_{\rm gd}+C_{db})\right]-\omega Z_0\left[(1+g_m r_o)C_{\rm gd}+C_{\rm gs}\right]\left[\omega^2 C_{\rm gd}(C_{\rm gd}+C_{db})-g_m\left(\frac{1}{r_o}+\frac{1}{Z_0}\right)\right]}{\left[\omega^2 C_{\rm gd}(C_{\rm gd}+C_{db})-g_m\left(\frac{1}{r_o}+\frac{1}{Z_0}\right)\right]+\omega^2 Z_0\left[(1+g_m r_o)C_{\rm gd}+C_{\rm gs}\right]\left[C_{\rm gd}\left(\frac{1}{r_o}+\frac{1}{Z_0}\right)+g_m(C_{\rm gd}+C_{db})\right]}\right\} \qquad (13)
$$

$$
\angle S_{21}\left|_{\rm CG}\right. = \tan^{-1}\left\{\frac{-\omega\left[C_{\rm gs}Z_0\left(1+\frac{r_o}{Z_0}\right)+r_o(1+g_m Z_0)(C_{\rm gd}+C_{db})\right]}{(1+g_m Z_0)\left(1+\frac{r_o}{Z_0}\right)-\omega^2 C_{\rm gs}Z_0\left[r_o(C_{\rm gd}+C_{db})\right]}\right\} \qquad (14)
$$

$$
\angle S_{21}\left|_{\rm CGCG}\right. = \tan^{-1}\left(\omega\frac{AD-BC}{AC+\omega^2 BD}\right) \qquad (15)
$$

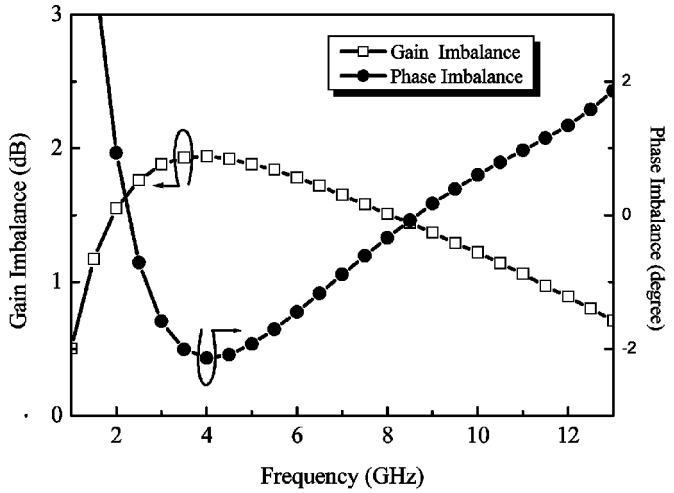

Fig. 7. Simulated amplitude imbalance and phase imbalance of the cascode CG and CS active balun with mixer core.

in this study has higher upper frequency bound than others, except [13]. The balun in [13] adopted the differential amplifier topology, and has a wideband range performance from 0.2 to 22 GHz. However, it consumed a very large power, which is 92 times the power used in this study. The main difference between the cascode CG and CS active balun and conventional one is the cascode common-gate stage. The common source stage characterizes high resistance with the reactance composed of parasitic capacitance $C_{\rm gs}$ and $C_{\rm gd}$ in the transmission process. The large resistance and parasitic capacitance will lead to higher *RC* delay. Therefore, larger phase delay will be generated. As to the common gate stage, the resistance in the transmission process is approximate to $1/g_m$ with the reactance composed of parasitic capacitance of $C_{\rm gs}$. Hence, its *RC* delay effect is less than the common source stage, especially for wideband application. The cascode common gate stage is used to add phase delay to approach the tendency toward the phase variation of the common source stage when frequency varies. The cascode common-gate configuration is adopted to increase the phase delay to attain the bandwidth extension in the less phase error condition.

The simulated gain imbalance and phase imbalance of the cascode CG and CS active balun combined with the mixer core, presented in Section II-A, are shown in Fig. 7. The Agilent Advanced Design System (ADS) simulated data show that in the bandwidth from 2 to 13 GHz, the gain imbalance is less than 2 dB (0.7–1.9 dB) and the phase imbalance is within $\pm 2^{\circ}$.

III. Measurement Results

The proposed cascode Gilbert cell mixer with wideband active baluns was designed and fabricated using the TSMC 0.18-μm CMOS process. The die photograph of the proposed circuit is depicted in Fig. 8 with a chip size of 0.85×0.57 mm^2, where the active region occupies an area of 0.44×0.48 mm^2.

The measurements were performed with the chip directly mounted on a 20-mil RO4003 high-frequency microwave substrate and tested through subminiature A (SMA) connectors, as shown in Fig. 9.

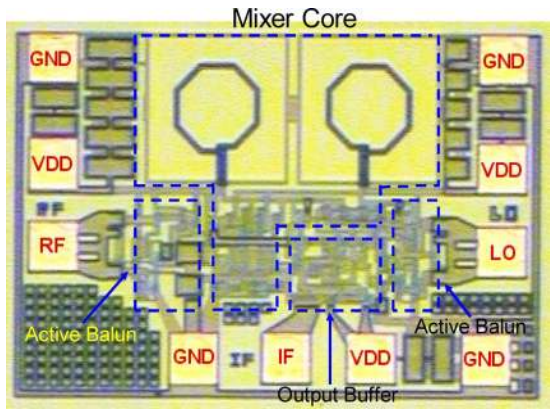

Fig. 8. Micrograph of the proposed mixer (size: 0.85×0.57 mm^2).

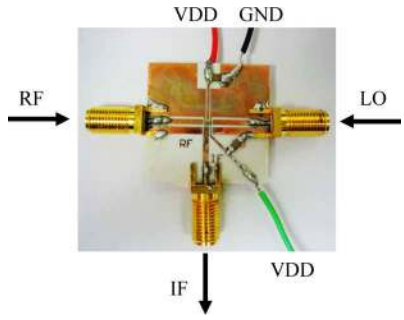

Fig. 9. Die mounted printed circuit board for testing.

The effects of the chip pads, bond wires, and transmission lines in the circuit board are taken into consideration in the simulation process of the entire circuitry. All measurements were done at a 1.8-V supply voltage and the total power consumption is 25.7 mW, including that (14.5 mW) consumed by the output buffer. The conversion gain of the proposed mixer was measured for an IF frequency of 50 MHz with both RF and LO ports swept in frequency up to 12 GHz. The RF and LO signal power were set to be -30 and -5 dBm, respectively. The simulated and measured power conversion gain versus the RF frequency is shown in Fig. 10. The mixer achieved a conversion gain of better than 4.4 dB over a wideband frequency from 2 to 12 GHz. The conversion gain also exhibited a 3-dB variation across the RF frequency of 2–11 GHz with an average conversion gain of 6.9 dB and maximum gain of 8.4 dB. The measured return loss for the RF signal is also shown in Fig. 10, which illustrates that the proposed mixer possesses a return loss better than 10 dB from 2 to 12 GHz. Although not shown, the measured LO and IF return losses are also larger than 10 dB. The port-to-port isolations of the proposed mixer were measured and are presented in Fig. 11. The LO-to-RF and RF-to-IF isolations of the mixer are both better than 25 dB, and the LO-to-IF isolation is above 20 dB over the entire measurement frequencies.

The simulated and measured power conversion gain versus RF input power is illustrated in Fig. 12 for RF frequency of 8 GHz and LO frequency of 7.95 GHz. The LO power is fixed at -5 dBm.

In Fig. 12, it is seen that the RF input 1-dB compression point $(\mathrm{IP}_{1\ \mathrm{dB}})$ of -7 dBm is obtained. Fig. 13 depicts the main signal

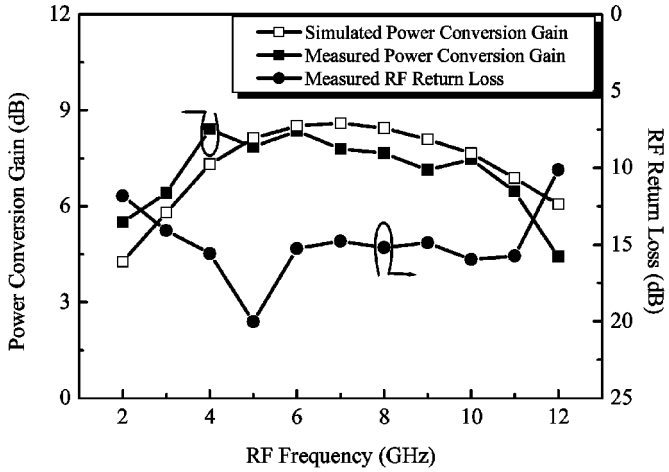

Fig. 10. Power conversion gain and RF return loss versus RF frequency. The IF frequency is 50 MHz, RF power is −30 dBm, and LO power is −5 dBm.

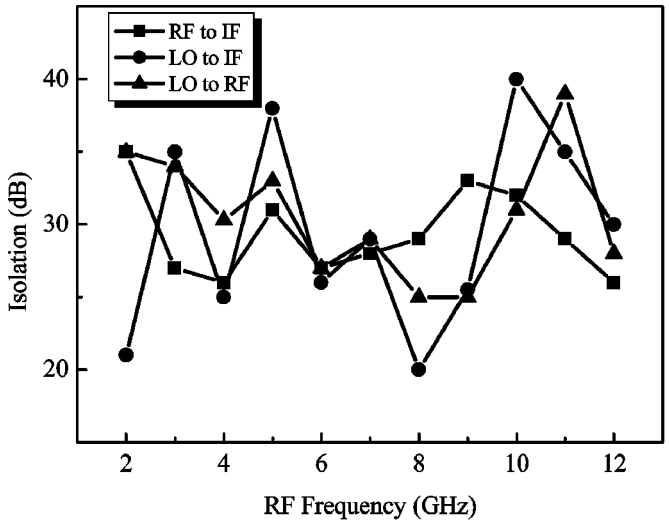

Fig. 11. Measured isolations versus RF frequency.

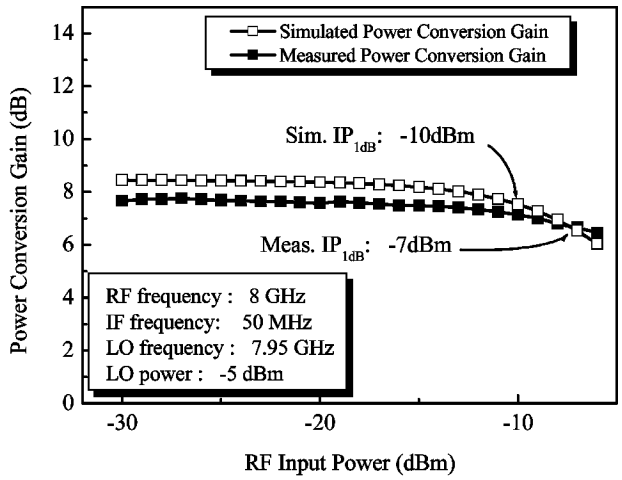

Fig. 12. Power conversion gain versus RF input power.

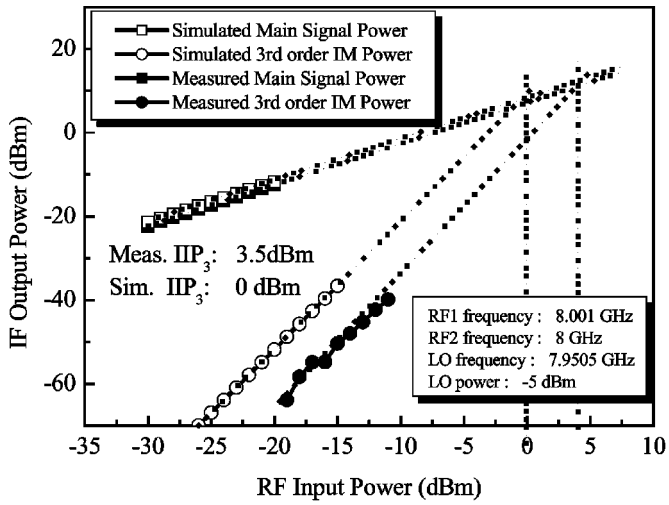

Fig. 13. Main signal power and third-order intermodulation power as functions of the RF input power.

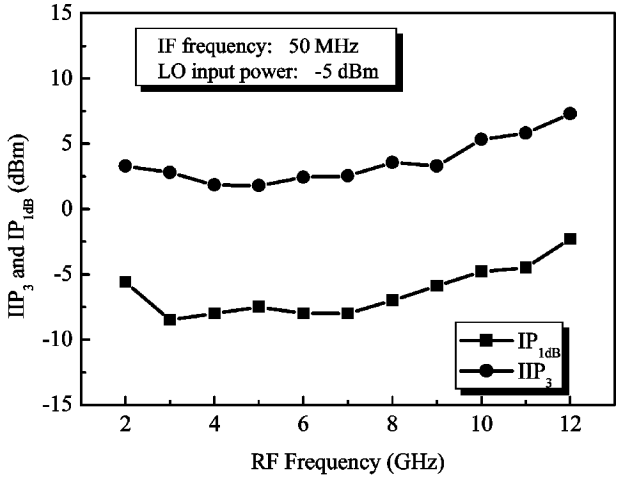

Fig. 14. Measured $\mathrm{IIP_3}$ and $\mathrm{IP_{1\ dB}}$ versus RF frequency.

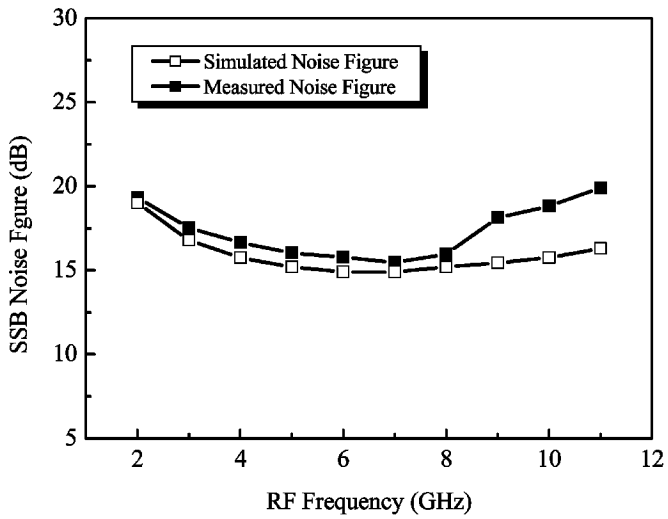

Fig. 15. Noise figure versus RF frequency.

power and third-order intermodulation power as functions of the RF input power. There are two signals fed to the RF input port for IIP3 measurement, one at 8 GHz and the other at 8.001 GHz. The LO signal has a frequency of 7.9505 GHz and power level of −5 dBm. The proposed mixer exhibited an input third-order intercept point ($\mathrm{IIP_3}$) of 3.5 dBm at the RF frequency of 8 GHz.

TABLE II
PERFORMANCE COMPARISON BETWEEN THIS STUDY AND OTHER WIDEBAND MIXERS

Reference	this work	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]
Technology	0.18μm CMOS	GaAs HBT	GaAs HBT	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm BiCMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	GaAs HBT
Freq. (GHz)	2 ~ 11	DC ~ 9	DC ~ 8	0.3 ~ 25	3.1 ~ 8.7	1~1.6	3.5~14.5	0.2~16	3~7	0.5~7.5	1.5~14
CG (dB)	6.9 ± 1.5	10.5 ± 1.5	9.5 ± 1.5	11 ± 1.5	3.75 ± 1.25	5.9	15	>5.3	5.3~8.2	5.7	20
IIP_3 (dBm)	6.5	2	-7	---	5	4.1	-7	---	-3.2~-0.3	-5.7	-3
IP_{1dB} (dBm)	-3.5	-4	-17	-5	---	---	-19	-10 (OP_{1dB})	---	-16	-17
LO Power (dBm)	-5	-8	-2	-1	9	0	6	-2	450 mV_{pp}	5	---
Pdis. (mW)	25.7	25	---	71	10.4	20.7	60	15	2.5~5.8	0.48	16.32
Supply Voltage (V)	1.8	5	5	5	1.8	1.8	5	1.8	0.8~1.2	0.77	2.4
Die Area (mm^2)	0.85 × 0.57	---	---	0.8 × 1	1.4 × 1.16	0.43 × 0.36 (core)	1 × 1	0.68 × 0.65	0.36 × 0.38 (core)	0.86 × 0.72	1 × 1
Balun Type	Active (Cascode CG & CS)	Active (CBCE)	Active (CBCE)	w/o	w/o	w/o	Passive (Marchand)	w/o	w/o	w/o	Passive (Transformer)

Finally, $IP_{1\,dB}$ and IIP_3 were measured for various RF frequencies ranging from 2 to 12 GHz. The results are shown in Fig. 14. In the measurement, the LO power was set as -5 dBm and the IF frequency was fixed at 50 MHz. The measured single-sideband (SSB) noise figure is 15.5 dB, and the overall measured results are shown in Fig. 15. The proposed mixer works well from 2 to 11 GHz with maximum $IP_{1\,dB}$ and IIP_3 of -3.5 and 6.5 dBm, respectively. The proposed mixer is compared with the state-of-the-art Gilbert cell mixers [22]–[31] in Table II.

It shows that the proposed mixer provides better linearity, more compact chip size, and acceptable conversion gain and power consumption than other studies. The proposed configuration shows the highest IIP_3 and $IP_{1\,dB}$, and exhibits more compact size than most of the published studies.

IV. CONCLUSION

In this paper, a high linearity mixer using *LC* folded cascode mixer topology, a feedforward compensated differential transconductor, and wideband active baluns in TSMC 0.18-μm CMOS technology has been presented. The *LC* folded cascode method is used to get more voltage headroom, and the feedforward compensated differential transconductor is adopted to achieve broadband impedance matching and lower the overall distortion. The cascode CG and CS active balun structure exhibits a broadband performance, which provides balance signals for the mixer core from a single input. The finished mixer core and active baluns possess good linearity, wide bandwidth, and occupy an area of only $0.85 \times 0.57\ mm^2$ with a consumed power of 25.7 mW under a 1.8-V supply voltage, which is suitable for application in various wireless communication systems.

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Pei-Zong Rao was born in Kaohsiung, Taiwan, on February 15, 1980. He received the B.S. degree in physics from National Kaohsiung Normal University, Kaohsiung, Taiwan, in 2002, the M.S. degree in physics from National Tsing Hua University, Hsinchu, Taiwan, in 2004, and is currently working toward the Ph.D. degree in communication engineering at National Chiao Tung University, Hsinchu, Taiwan.

His currently research interests are microwave circuits and RF integrated circuits.

Tang-Yuan Chang received the B.S. degree in electrical engineering from Yuan Ze University, Taoyuan, Taiwan, in 1998, and the M.S. degree in communication engineering with National Chiao Tung University, Hsinchu, Taiwan, in 2007.

He spent several years in industry prior to earning the M.S. degree. His currently research interests include wideband mixers for synthesizers and 24-GHz phase-locked loops for collision-avoidance radar systems.

Ching-Piao Liang was born in Changhwa, Taiwan, in 1980. He received the B.S. and M.S. degrees in communication engineering from Yuan Ze University, Taoyuan, Taiwan, in 2003 and 2005, respectively, and is currently working toward the Ph.D. degree in communication engineering at National Chiao Tung University, Hsinchu, Taiwan.

His primary research interests include RF integrated circuits and MMICs.

Shyh-Jong Chung (M'92–SM'06) was born in Taipei, Taiwan. He received the B.S.E.E. and Ph.D. degrees from National Taiwan University, Taipei, Taiwan, in 1984 and 1988, respectively.

Since 1988, he has been with the Department of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he is currently a Professor. From September 1995 to August 1996, he was a Visiting Scholar with the Department of Electrical Engineering, Texas, A&M University, College Station. His research interests include the design and applications of active and passive planar antennas, communications in intelligent transportation systems (ITSs), low-temperature co-fired ceramic (LTCC)-based RF components and modules, packaging effects of microwave circuits, and numerical techniques in electromagnetics.

Dr. Chung was the treasurer of the IEEE Taipei Section from 2001 to 2003 and the chairman of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Taipei Chapter from 2005 to 2007. He was the recipient of the 2005 Outstanding Electrical Engineering Professor Award of the Chinese Institute of Electrical Engineering and the 2005 Teaching Excellence Award of National Chiao Tung University.