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ANALOG AND DIGITAL PERFORMANCE OF THE SCREEN-GRID FIELD EFFECT TRANSISTOR (SGrFET)

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The Screen-Grid Field Effect Transistor (SGrFET) is a planar MOSFET-type device with a gating configuration consisting of metal cylindrical fingers inside the channel perpendicular to the current flow. The SGrFET operates in a MESFET mode using oxide insulated gates. The multi-gate configuration offers advantages for both analog and digital applications, whilst the gate cylinder holes can be exploited for bio-applications. In this manuscript TCAD results are presented on the analog and digital performance of the Screen-Grid Field Effect Transistor. The results are compared to the operation of an SOI-MOSFET and a finFET.

Keywords: MOSFET; multi-gate; performance comparison; finFET.

1. Introduction

Until recently, the research on field effect transistors has been controlled by the overpowering presence of silicon based conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). This success was ensured by the abundance of Si and the quality of the silicon oxide (SiO_2). Only in domains such as e.g. communications, where high speed operation is required, alternative transistor and gating structures have been used. As a result of the requirement for higher speed and higher packing density, the dimensions of the Si MOSFETs have been aggressively scaled down[1]. The gate length has been reduced to sub-50 nm, the oxide thickness to 1.2 nm, the doping in the channel has increased and the junction depth has decreased. The MOSFET has now reached GHz operation speeds as a result of this dramatic downscaling. However, the price for this speed performance is an increase in power consumption that results from the leakage currents that are partially associated with short channel effects (SCEs)[2]. One of the important parameters that benchmark the SCEs is Drain Induced Barrier Lowering (DIBL). DIBL is related to a threshold voltage shift as a function of applied drain bias and is a consequence of the influence of the drain potential on the source-channel

potential barrier. In electrically robust MOSFETs, the source-channel potential barrier is controlled by the gate voltage only, however, for dramatically reduced gate lengths where the drain becomes close to the source, the drain potential shares the control of the barrier with the gate. In order to prevent the drain from taking control, the doping level in the channel is increased. This practice severely reduces the mobility of the carriers in the channel due to impurity scattering. As a consequence of all these factors, MOSFET technology has now reached the point where industry is actively pursuing research into alternative field effect transistor structures preferably based on Si. The first accepted change was the introduction of silicon-on-insulator substrates (SOI)[3]. An approach that takes control of the leakage into the substrate and that reduces the parasitic capacitances of the junctions. Another approach that has proved successful is the multi-gate FET (MuGFET). Although it was known for a long time that adding supplementary gates will improve the control of the carriers in the channel and therefore help to contain DIBL, the MuGFET idea only became successful with the discovery of a CMOS-compatible fabrication approach. Now the best known MuGFET is the finFET[4]. The finFET has an out-of-plane channel (the fin) that is partially surrounded by the gate electrode. FinFETs take advantage of the SOI technology to restrict carrier flow to the channel. Apart from these popular high-visibility alternative MOSFET structures, the research literature presents many more sophisticated approaches; examples include the wrap-around nanowire FET[5], the ballistic deflection transistor[6], the source-gated transistor[7], the Screen-Grid Field Effect Transistor (SGrFET)[8], etc.

In this manuscript the analog and digital performance of the SGrFET will be evaluated and compared to that of the SOI-MOSFET and finFET. The evaluation and comparison will be done using TCAD from Synopsys[9], 2D Medici and 3D Taurus. The manuscript is organized as follows: section 2 describes the different device structures used in the simulations and gives some DC performance comparison. In 3 the analog RF performance is compared. In 4 the use of the multi-gate character of the SGrFET and finFET for digital applications is explored. Conclusions are presented in 5.

2. The simulated device structures

Three devices, SOI-MOSFET, finFET and SGrFET were simulated in order to make a performance comparison between them. The simulations were done using the hydrodynamic model and the full coupled energy balance equations where necessary. The field effect mobility is used to take into account the influence of the effective electric field on the mobility of the carriers. The analog performance is studied using 3D Taurus simulations. The digital performance is done in 2D as the circuits consist of more than one transistor and thus create a large number of mesh points that can impede convergence of the simulations. The simulated 3D structures obtained via the Taurus process simulation software are shown in fig. l.

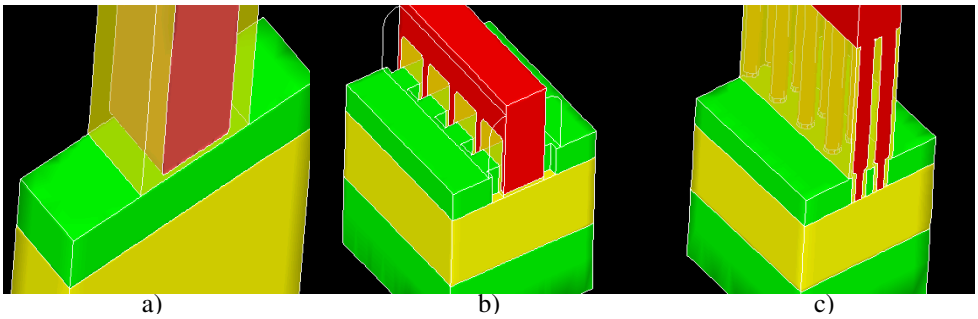

Fig. 1. Three different devices "fabricated" using Taurus process simulation. Green: Si, yellow: insulator, red: gate. Source and drain are at the left, resp. right of the gated area in all devices. a) SOI-MOSFET, b) a finFET with 4 parallel fins and c) and SGrFET with 4 parallel channels/unit cells.

In order to visualize the functioning of the different structures a cross-section is taken from surface into the buried oxide (BOX) layer for the SOI-MOSFET and perpendicular to the surface for both finFET and SGrFET. These cross sections are given in fig. 2.

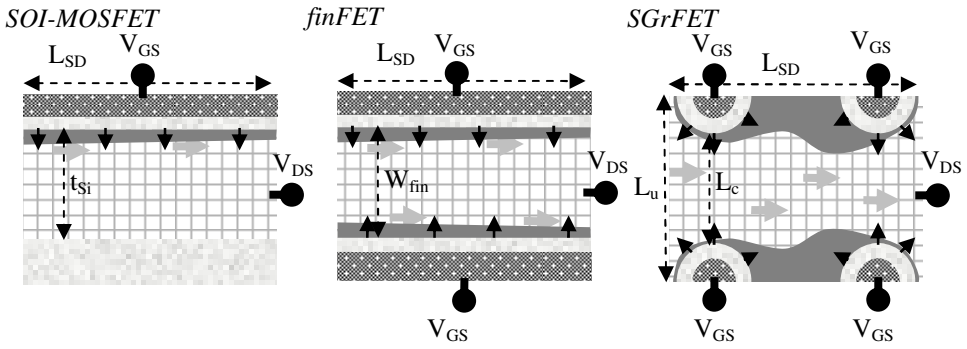

Fig. 2. The cross section through one channel/fin region for the three devices. The channel/fin region is checked, light grey is oxide, dark grey is depletion region, dotted dark grey are the gate contacts. Black arrows indicate the direction of the field imposed by the gate voltage, grey arrows indicate the position and direction of the carrier flow. The geometry given for the SGrFET is called a unit cell.

The main differences seen in the schematic cross sections in fig. 2 are that the SOI-MOSFET has one channel created by inversion at the Si/SiO_2 interface. Thus the carriers will scatter at this interface reducing the channel mobility μ. Unless the Si body thickness t_{Si} is sufficiently thin, this device will suffer from SCE. The finFET can have two channels for one fin, both created by inversion. The channel is close to the oxide interface and thus mobility will be similarly reduced by interface roughness scattering. The finFET is robust against downscaling if the fin width W_{fin} is correctly scaled with the source-drain distance L_{SD}. The SGrFET has one channel for the same dimensions as the finFET. The SGrFET functions by controlling the carrier density by depletion as in a MESFET. The carriers flow away from the interface, thus suffer reduced surface roughness scattering and have higher mobility. The SGrFET is robust against downscaling when the

width L_c is reduced with a reduction of L_{SD}. The gate length in the SGrFET is uncoupled from the source-drain distance but the minimum L_{SD} is imposed by the radius of the gate cylinders. The depletion widths around the gates are not symmetrical in the length of the device. Those around the drain-side gates expand faster with drain voltage than the source-sided ones. The row of gates near the drain electrostatically shield the source from the drain potential, preventing its parasitic control of the source-channel barrier and thus helps to control DIBL [8]. A comparison of the main performance benchmarks: threshold voltage, subthreshold slope and DIBL are given in fig. 3 as a function of source-drain distance L_{SD}. The gate for all devices is Al with a workfunction of ϕ_{Al}=4.1eV. The channel doping is $N_{A/D} = 10^{15}$ cm^{-3}.

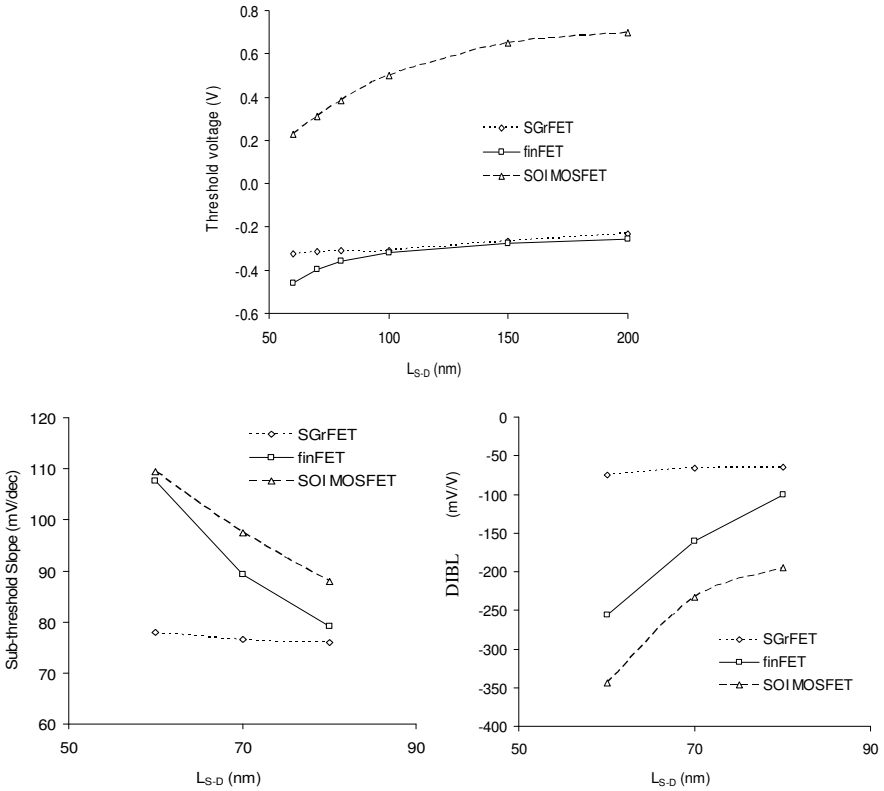

Fig.3. Downscaling trend of some device benchmarks, threshold voltage (top), subthreshold slope (left bottom) and drain induced barrier lowering (right bottom) for the SGrFET, the finFET and the SOI-MOSFET.

The simulated benchmark parameters presented in fig. 3 are typical DC parameters and thus do not take into account capacitive parasitics. The simulations are done for all devices with the same dimensions: t_{Si} = 40 nm (the Si body thickness on top of the SOI layer), t_{ox} = 5 nm (oxide thickness), $W_{fin} = L_u$= 30 nm (the fin width resp. unit cell width), thus L_c = 25 nm for the SGrFET. The radius of the gate cylinders for the SGrFET is 5 nm. From the graphs in fig. 3 we conclude that the SGrFET shows an excellent robustness

against SCE, high potential for ultra low-power applications (the subthreshold slope is very close to the theoretical limit) and immunity against threshold voltage roll-off with downscaling. The drawback at these small dimensions is that e-beam lithography (or soft imprinting techniques) is necessary to define the device – fabrication steps that are currently mainly used in research and development environments.

3. Analog RF performance of the devices

The radio frequency (RF) performance of the devices is investigated using Taurus. The AC small-signal simulations give the Y-parameters as a function of frequency and bias voltages. From these, the high frequency parameters such as small-signal current gain (*h21*) and Mason unilateral power gain (*U*) can be derived, which yield the corresponding cut-off frequencies (f_T) and the maximum oscillation frequency (f_{max}). Basic analog parameters such as transconductance (g_m), transconductance efficiency (g_m/I_{DS}), output resistance (r_o) and intrinsic voltage gain (A_v) can also be extracted. The device simulations are carried out ignoring any contact resistance of gate, source and drain. This assumption causes an overestimation of the high frequency performance. Additionally the hydrodynamic model, which is used for increased accuracy at small device dimensions, tends to predict higher transconductance[10] and lower gate-to-source capacitance, C_{GS}[11] than what is experimentally obtained. Thus the extracted cut-off frequency will be over-estimated. This however is not an issue in a comparative study.
In order to extract $r_o=1/g_{ds}$, g_m/I_{DS}, f_T and $A_v=g_m/g_{ds}$ a simple MOSFET equivalent circuit has been used for all devices, given in fig. 4.

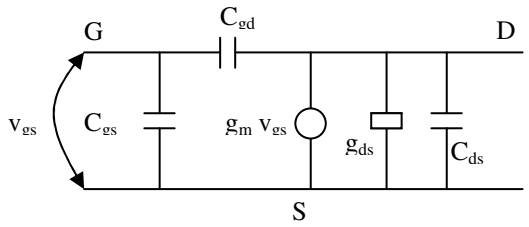

Fig. 4: Simple equivalent circuit for all FETs including the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, the drain-source capacitance C_{ds}, the output conductance g_{ds} and the current source $g_m \times v_{gs}$ g_m is the transconductance.

The circuit components are then extracted from the simulated Y-parameters as[12]:

$$C_{GD} = -\frac{\mathrm{Im}(Y_{12})}{w} \tag{1}$$

$$C_{GS} = C_{GG} - C_{GD} = \frac{\mathrm{Im}(Y_{11})}{w} - C_{GD} \tag{2}$$

$$g_m = \mathrm{Re}(Y_{21}) \tag{3}$$

$$g_{ds} = \mathrm{Re}(Y_{22})\big|_{w=0} \tag{4}$$

$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})} = \frac{g_m}{2\pi C_{GG}} \tag{5}$$

where C_{GG} is the total gate capacitance. The cut-off frequency f_T given in (5) is only an approximation and in this work f_T has been derived by plotting the simulated current gain *h21* as a function of frequency. The frequency where *h21* becomes unity defines f_T. The magnitude of current gain, *h21* is given by:

$$|h21| = \frac{|Y_{21}|}{|Y_{11}|} \tag{6}$$

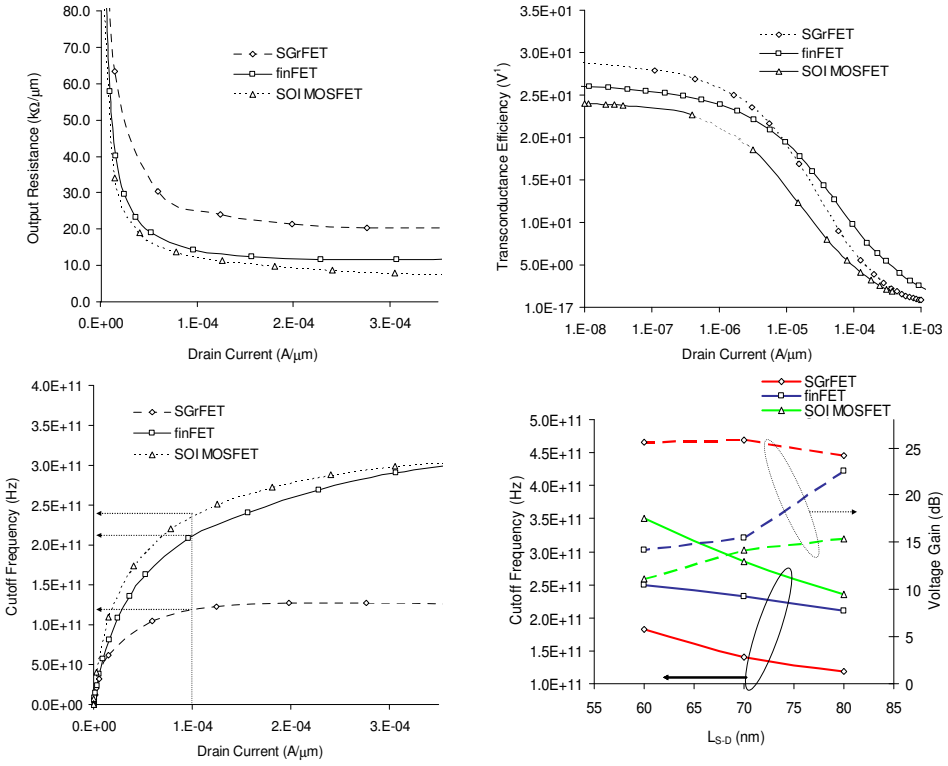

Fig. 5. The performance parameters of the SGrFET, SOI-MOSFET and the finFET as a function of current drive. Bottom right: the cut-off frequency, f_T and voltage gain, A_v as a function of source-drain distance, L_{SD} at a current drive of 0.1 A/μm as indicated in bottom left figure. Dashed lines: A_v, full lines f_T.

In fig. 5, r_o, g_m/I_{DS} and f_T are given as a function of source-drain current for the three devices under study. f_T and A_v as a function of L_{SD} are also shown. r_o and g_m/I_{DS} are best in the SGrFET whilst f_T is highest in the SOI-MOSFET. The graph on downscaling gives an interesting result: A_v is not degraded for the SGrFET whilst downscaling. This result stands in contrast with all other FET behavior which shows systematic A_v degradation for

smaller source-drain distances. The price that is paid for this gain however is a lower f_T for the SGrFET. As can be seen from the g_m/I_{DS} plot, the SGrFET behaves best at lower current levels, confirming the potential of the SGrFET for low-power applications as pointed out before. This is because when driving the SGrFET in strong inversion the inversion channel around the circular gate fingers do not overlap and therefore the energy used for inversion can not be exploited for higher current drive. This can change when exploring still smaller dimensions in which the inversion layers interact.

4. Digital performance of the devices

2D TCAD has been used to analyze and compare the digital performance of the SGrFET with the finFET of the same dimensions. Both device types are ideally suited for multi-gate functionality (MuGFETs) where different gate voltages are applied to the different gate contacts. An analysis of the digital SGrFET only was presented in [13]. In this manuscript we will focus on a comparison of the switching speeds and multi-gate operation of both technologies. The MuGFET approach reduces the circuit complexity and enhances speed. The gate metal for the enhancement mode devices is Au (ϕ_{Au}=4.8eV) and for the depletion mode devices Al. The channel has a doping of $N_{A/D} = 10^{15}$ cm^{-3}.

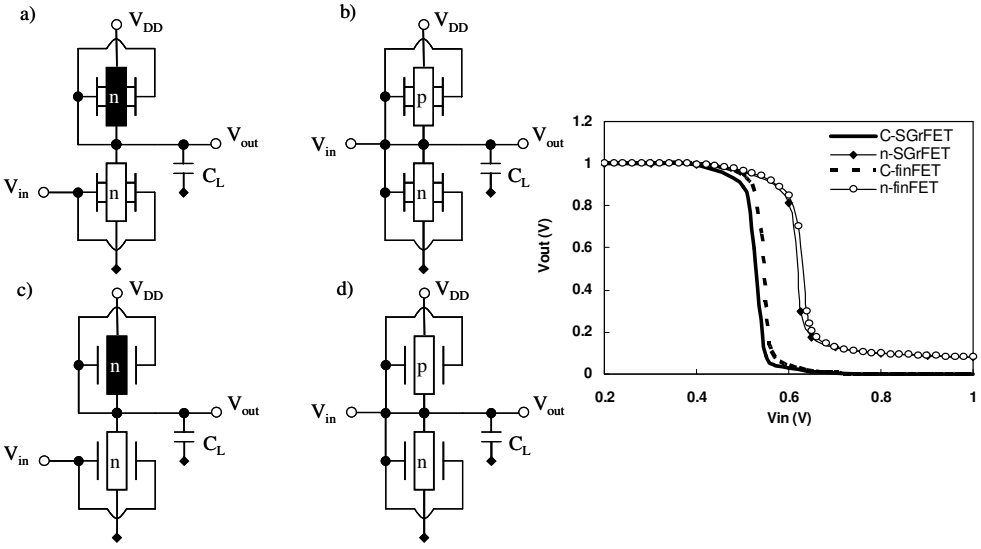

Fig. 6. Left: Definition of device circuit symbols and circuit. Black/white device rectangle: depletion/inversion mode. Letter in rectangle defines device type. a) n-SGrFET inverter, b) C-SGrFET inverter c) n-finFET inverter [12] d) C-finFET inverter [12]. Right: output characteristic. C_L = 0.27fF and 0.24fF for the SGrFET and finFET respectively. V_{DD} = 1V.

Four different logic gates have been investigated, the inverter, NAND, NOR and XOR. The dimensions of the devices are: gate oxide thickness t_{ox} = 2 nm, source-drain distance L_{SD} = 140 nm, $L_c = W_{fin}$ = 50 nm (see fig.2). This means that the width of a SGrFET unit cell is $L_u = 2\times L_o/2+2\times t_{ox}+L_c$. The diameter of the gate cylinders is L_o = 50 nm. The gate

diameter is an extra SGrFET parameter that can be used to control its operation. All circuits operate at V_{DD} = 1V. Note that the SGrFET is not as aggressively scaled down as for the analog performance study in order to allow sufficient drive current. The finFET circuits are as those presented in [14], the reader is referred to the circuit diagrams presented in [14]. In fig. 6 the inverter circuits, both CMOS and all n-MOS are given together with the output characteristics for both finFET and SGrFET. The difference between the outputs from both devices is negligible. The all n-type inverters exhibit the typical poor switch-off characteristics. Increasing the width of the driver mitigates this problem but does not solve it. In the SGrFET good off-switching can be obtained by adding extra unit cells to the driver. This increases current drive whilst retaining the other FET parameters. The total width of the driver for N unit cells then becomes $N \times L_u$ and the number of gate fingers (N+1)×2, with the gate fingers at the outer edges halve cylinders. Thus the complete switch-off character comes at a price of an increased footprint to 312 nm. The same approach for finFETs needs N parallel fins, giving a footprint of min. 250nm for N=3. This is possible for the inverter circuits but for the other logic circuits, where the gate at each side of all fins needs an independent voltage, this approach will be difficult to implement. Therefore in those finFET circuits increased current drive in the driver can only be practically done by increasing its width. This tends to reduce its performance.

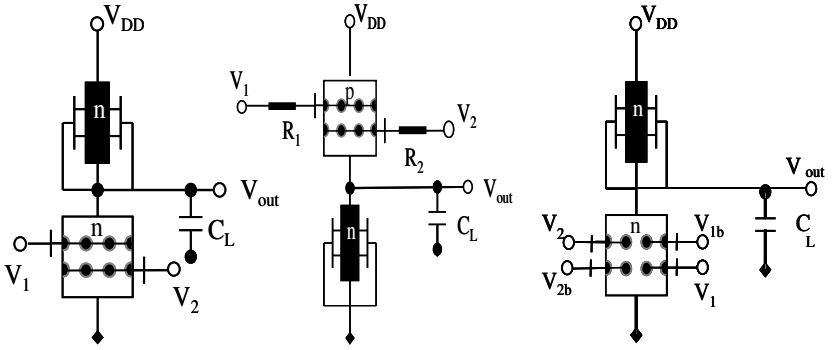

Fig. 7: SGrFET logic circuits. (left) NAND, (middle) NOR, (right) XOR. For full switch off, a 3 unit cell device is used. $V_{1,2\ max}$=1V and V_{DD}=1V. V_{ib} means NOT(V_i) with i=1,2. The finFET circuits can be found in [13].

The multi-unit cell approach was used in the NAND, NOR and XOR circuits, the SGrFET circuit diagrams are given in fig. 7. In the SGrFET logic gates a 3-unit cell device is used to obtain complete switch-OFF. Note that the XOR can be constructed with only 2 SGrFETs.

Table 1: The rise time of the different logic circuits usig finFETs or SGrFETs.

Circuit & delay Device Type	NAND t_r (ps)	NOR t_r (ps)	XOR t_r (ps)
finFET	127	86	111
SGrFET	45	45	70

For the finFET logic gates the fin width is increased to $3\times W_{fin}$=150nm to minimize leakage while maintaining good finFET performance. However no full OFF-switching could be obtained unless the maximum value of the input voltage is increased to 1.5V, an impractical solution. Only the switching characteristics of the XOR are given here (see fig. 8). The finFET XOR consists or 3 devices [14]. The poor performance of the finFET XOR circuit is potentially due to the unstable circuit node where the source and drain electrodes of the two drivers are connected.

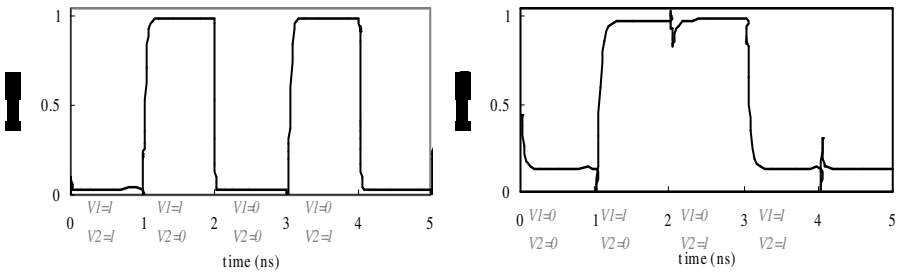

Fig. 8. Left: SGrFET XOR output characteristics, right: finFET XOR output characteristics. Values of the input voltages in each time period of 1 ns are given in grey on the x-axis.

A summary of the performance of the different logic circuits is given in Table 1. The results show that the SGrFET logic is faster than the finFET logic. This result must be attributed to the higher mobility of carriers in the SGrFET than the finFET and the unit cell configuration of the SGrFET.

Table 2 gives the ON and OFF currents in all devices when taking the input voltage for ON=1V and OFF=0V. As the threshold voltage of both SGrFET and finFET are the same within ±0.01V, the gate voltage overdrive at V_{ON} is approximately the same for both devices. ON currents in finFETs are higher than in SGrFETs and thus consume more power during switching. OFF currents in finFETs are also higher and thus the stand-by power consumption will be higher. This result leads us to conclude that the SGrFET can deliver faster switching speed in its split-gate logic configuration for reduced power consumption than the finFET with the same geometrical dimensions.

Table 2: ON and OFF state for enhancement mode, $I_{N,P}$ denotes n,p-type device current.

V_{in} (V)	$I_{N\text{-}SGrFET}$ (A/μm^2)	$I_{P\text{-}SGrFET}$ (A/μm^2)	$I_{N\text{-}finFET}$ (A/μm^2)	$I_{P\text{-}finFET}$ (A/μm^2)
$V_{ON} = V_{DD}$=1 V	$2.08E^{-4}$	$-1.88E^{-4}$	$4.6E^{-4}$	$-3.88E^{-4}$
V_{OFF} = 0 V	$8.023E^{-13}$	$-1.316E^{-10}$	$1.5E^{-12}$	$-2.15E^{-10}$

5. Conclusions

The performance of the SGrFET compares well to that of both the finFET and the more traditional SOI-MOSFET. The RF performance analysis shows that the design of the SGrFET allows it to preserve high values of the low-frequency voltage gain under aggressive channel scaling. This is a strong feature as all FETs suffer from a loss of

voltage gain for decreased gate lengths. The SGrFET exhibits lower cut-off frequencies, f_T than its counterparts only for higher values of drain current, whereas the f_T values are similar for low-power applications in the three transistors. For digital applications the SGrFET lends itself well for low power, high speed operation with reduced devices per circuit and high switching speeds. The footprint of the SGrFET is larger than the finFET but the multiple unit cell approach ensures low OFF currents.

Acknowledgments

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