Analog Circuits With High-Gain Topologies Using a-GIZO TFTs on Glass

Pydi Ganga Bahubalindruni, Bruno Silva, Vítor Grade Tavares, Pedro Barquinha, Nuno Cardoso, Pedro Guedes de Oliveira, Rodrigo Martins, and Elvira Fortunato

***Abstract*—This paper presents analog building blocks that find potential applications in display panels. A buffer (source-follower), subtractor, adder, and high-gain amplifier, employing only n-type enhancement amorphous gallium–indium–zinc–oxide thin-film transistors (a-GIZO TFTs), were designed, simulated, fabricated, and characterized. Circuit simulations were carried out using a neural model developed in-house from the measured characteristics of the transistors. The adder–subtractor circuit presents a power consumption of 0.26 mW, and the amplifier presents a gain of 34 dB and a power consumption of 0.576 mW, with a load of 10 MΩ//16 pF. To the authors' knowledge, this is the highest gain reported so far for a single-stage amplifier with a-GIZO TFT technology.**

***Index Terms*—Analog circuits, a-GIZO TFT, neural modeling.**

I. Introduction

LOW-TEMPERATURE fabrication of amorphous Gallium-Indium-Zinc-Oxide (a-GIZO) based thin-film-transistors (TFT) [1], [2] is proving to be promising in display applications. Compared to other competing TFT technologies, such as OTFT [3] and a-Si:H [4], a-GIZO TFTs show superior electrical mobility [5] and reliability [6]. Even though it was mainly meant for backplanes of AMOLED [7] and ultra definition LCDs [8], it is also finding extensive applications in driving circuits for back-planes of displays [9], [10] and RFIDs [11]. However, a-GIZO TFTs imposes various challenges in circuit design. Lack of commercial device models and technology libraries makes the design and simulation complex. In addition, poor intrinsic mobility compared to crystalline silicon and the absence of stable complementary devices (p-type TFT), makes the design of high-gain amplifier stages more challenging. Nevertheless, an operational amplifier was already reported with a gain of 18.7 dB [12] using enhancement TFTs, in which the amplifiers' first stage gain is limited due to the conventional diode connected loads. However, from a more practical point of view, in most cases this gain is not sufficient, demanding for more or higher gain stages.

The a-GIZO technology is fairly recent and has not yet reached the level of maturity that other technologies show. In general, reports on complex circuits is scarce, without topologies that favors the desired high gains. But in general, designing amplifiers with amorphous oxide-devices is a challenge because the gain is majorly impaired by the absence of stable complementary devices. Other techniques need to be employed to increase the active loads. In fact, one possibility is to use bootstrapping techniques to realize high active impedances. This type of technique was adopted in the past in bipolar technology to attain high-input impedances [13]. However, instead of the input, this very same technique can be used to boost the gain by applying the same principle to the amplifiers load. Such a concept can effectively be applied to single stage amplifiers to enhance the gain, up to values of the order of magnitude of the transistor intrinsic gain, and forms the bases for the proposed double bootstrapping technology. Then, this paper focuses on the design of analog blocks [14], [15] that are useful for high-gain stages, which can also function as buffer, adder and subtractor. All these functional blocks are important for data driver circuits in TFT LCD panels. In order to perform circuit simulations, a neural model was developed from measured characteristics of the transistors.

The rest of the paper is organized as follows. Section II presents the device characterization and modeling. Section III elaborates on the design of basic analog circuits and its operation (buffer, subtractor, and adder), including the proposed high-gain amplifier. Section IV presents the simulation results confronted with measured responses and finally in Section V conclusions are drawn.

II. TFT Characterization and Modeling

A bottom-gate staggered structure for TFTs was employed in all circuits. This structure is widely adopted by the display industry due to its good process compatibility. The a-GIZO devices were fabricated by sputtering, with maximum processing temperature of 200 °C. All the fabrication details are identical to the ones in [16], except for source-drain electrodes, where in the present work e-beam evaporated Ti/Au is used to improve the device performance and enable easier wire-bounding. The device modeling method follows a black-box approach and uses

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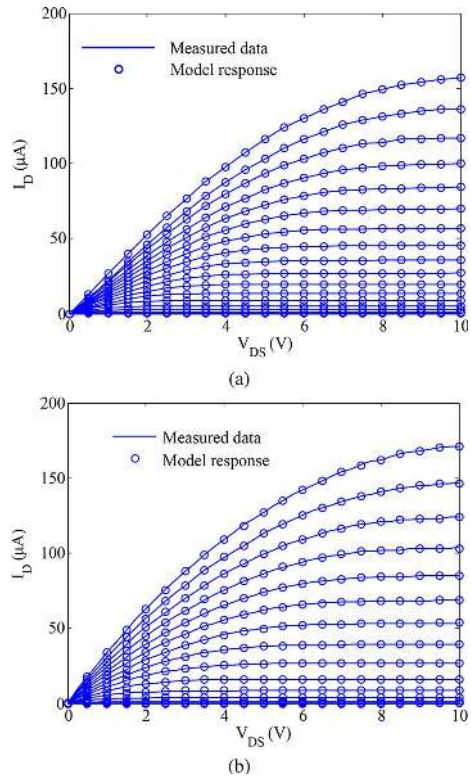

Fig. 1. Output characteristics of a-GIZO TFTs ($W/L = 160/20\ \mu m$) with different layouts: $0 \leq V_{DS} \leq 10$ V and $0 \leq V_{GS} \leq 8$ V, in steps of 0.5 V. (a) Direct layout. (b) Fingered layout.

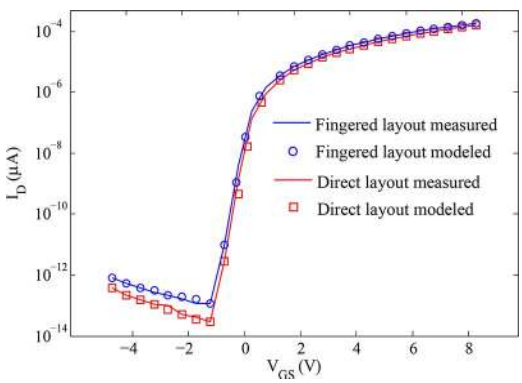

Fig. 2. Transfer characteristics of a-GIZO TFTs ($W/L = 160/20\ \mu m$) with direct and fingered layouts, $V_{DS} = 10$ V and $-5 \leq V_{GS} \leq 8$ V in steps of 0.5 V.

artificial neural networks, as functional approximators, developed from measured characteristics of the transistors [14], [16].

It is recognized that the series contact resistance (R_{SD}) at the source and drain terminals of TFTs lowers the performance of the device. R_{SD} includes the contact resistance between the source/drain electrode to the semiconductor layer and the high-impedance path in the semiconductor between the source/drain and the conductive channel. Part of the applied bias voltages are dropped in the series resistance of the transistor resulting in less drain current, which in turn lowers the device mobility and shows strong impact on the circuit performance. In order to attenuate this problem, when the transistor width is greater than 40 μm, fingered layout is employed to minimize R_{SD} on

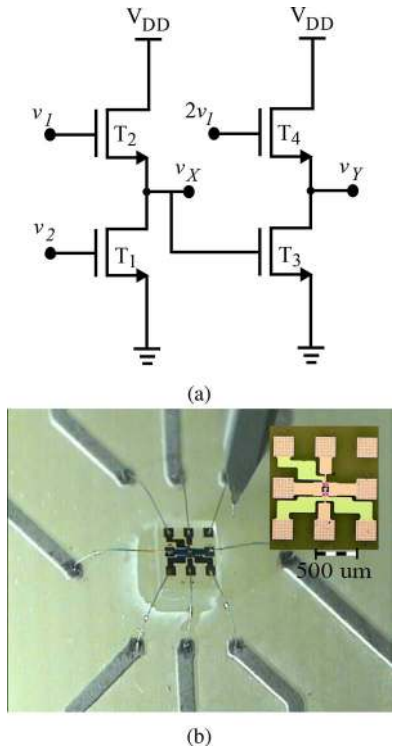

Fig. 3. Adder subtractor circuit. (a) Schematic. (b) Fabricated chip after wire-bonding and the circuit micrograph in the inset, total circuit area (including pads) is $1250 \times 1250\ \mu m^2$.

each transistor, which will result on a bigger effective V_{GS} and V_{DS} (transistors are in parallel) for the same external bias, when compared to the single full width transistor. Under the same conditions, fingered layout shows higher drain current due to the higher effective V_{GS} (can be seen as lower V_{TH}), and the lower total resistance also results in increased mobility, thereby improving the overall performance of the transistor.

The TFT output and transfer characteristics (measured and Verilog-A neural model response) are shown in Figs. 1 and 2, respectively, with both layouts. As it can be noticed, TFT with fingered layout presents more drain current than the direct layout transistor, for the same bias voltages and aspect ratio, which is explained by the effective lower series resistances in the fingered layout compared to the direct layout, as referred above.

III. Circuit Design

The adder-subtractor circuit schematic and its fabricated chip after wire-bonding are presented in Fig. 3(a) and (b), respectively. Based on the type of the inputs, it can function as a buffer, subtractor or adder. In addition, this block can be used to provide positive feedback (FB) for high-gain amplifier designs [17]–[19], as shown in Fig. 4. This circuit forms the basis for the different basic cells presented bellow.

A. Source Follower

A common-drain amplifier is useful in either shifting the DC level of a signal or as a buffer to drive circuits that present a low input impedance. In Fig. 3(a) the buffer circuit is formed with T_1 and T_2, by applying a constant bias (V_2) to T_1 and the input signal (v_1) to T_2.

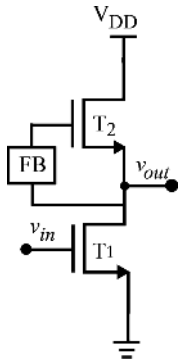

Fig. 4. High-gain amplifier topology using enhancement mode n-type transistors.

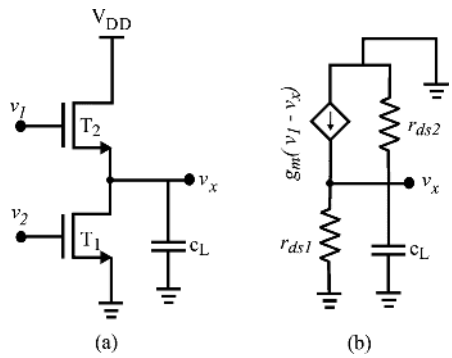

Fig. 5. Source follower configuration (a) Circuit schematic (b) Small signal equivalent circuit.

The schematic and the small signal equivalent circuit of the resulting source follower is shown in Fig. 5. The output (v_x), follows the input (v_1). The relation between v_x and v_1 is given by,

$$\frac{v_x}{v_1} = \frac{g_{m2}}{g_{m2} + g_{ds2} + g_{ds1}}, \tag{1}$$

where g_m and g_{ds} $(= \frac{1}{r_{ds}})$ are the transconductance and output conductance of the transistor. Unlike CMOS transistors, TFTs do not show body-effect, since the bulk is a pure insulator. Hence, a gain very close to unity can be obtained, when $g_m \gg g_{ds}$.

B. Adder-Subtractor

Analog subtractor and adder circuits are important functional blocks in computational systems. In Fig. 3(a), T_1 and T_2 TFTs form the subtractor, whereas T_1–T_4 together constitutes the adder. Assuming all transistors in saturation, and that the drain current (i_D) can be approximately expressed by

$$i_D \approx K * (v_{GS} - V_{TH})^2 \tag{2}$$

it can easily be demonstrated that when all transistors operate in the saturation region, subtraction and addition of the input signals can be obtained at the following nodes:

$$v_X = v_1 - v_2, \tag{3}$$

$$v_Y = v_1 + v_2. \tag{4}$$

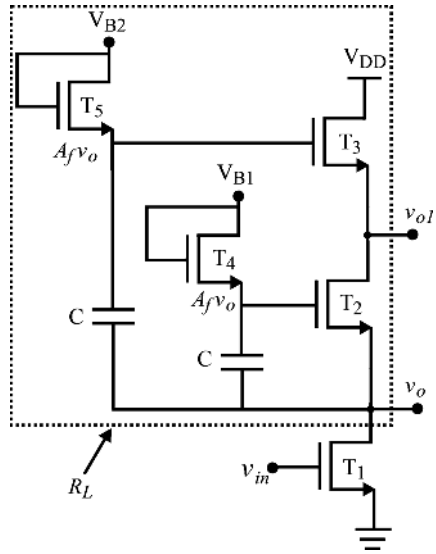

Fig. 6. Proposed high gain amplifier only with n-type enhancement mode transistors P.

C. Amplifier

Fig. 6 presents a circuit proposed to enhance the gain of a single-stage common source amplifier, involving only n-type transistors (enhancement). It employs a double bootstrapping technique that increases significantly the equivalent active-load value, to a point where the global gain gets very close to the intrinsic gain of the input transistor. Fig. 7 depicts the fabricated circuit (hereafter referred to as "Amp") in two versions, one with on-chip capacitors and another with external.

Operation: In order to achieve amplification, transistors T_1, T_2 and T_3 should operate in saturation. The bias transistors T_4 and T_5 operate in cutoff during the DC steady state, because they come in series with a capacitor and high impedance branches from T_2 or T_3 gates (ideally the gate current is zero). Therefore, the biasing transistors represent high equivalent resistors for signal. Accordingly, the bias voltages $\mathrm{V_{B1}}$ and $\mathrm{V_{B2}}$ appear at the gate terminals of the transistors T_2 and T_3, respectively. By choosing proper values for the biasing voltages and power supply, operation in saturation can then be ensured for transistors T_1, T_2 and T_3. The output signal (v_o) is fed back to transistors T_2 and T_3 by means of the feedback circuit that is formed by the capacitor C and the bias transistors $(\mathrm{C}, \mathrm{T}_4)$ and $(\mathrm{C}, \mathrm{T}_5)$, respectively. In small-signal terms, the biasing transistors equivalent circuit can then be represented by a parallel combination of the off-resistance $(\mathrm{R_{OFF}})$ and parasitic capacitance $(\mathrm{C_{OFF}})$, as shown in Fig. 8(a) and (b). The load resistance $(\mathrm{R_L})$, from Fig. 8(a) is given by

$$R_L = \frac{v_o}{i_o}.$$

Before finding the actual value of the load resistor, it should be noted that the feedback paths in the "Amp" circuit cause a high-pass filter action. Consequently, this amplifier cannot amplify DC. However, the lower cutoff frequency can be made very small (mHz range), by choosing a proper high value for C. From Fig. 8(b), the feedback gain (A_f) is given by

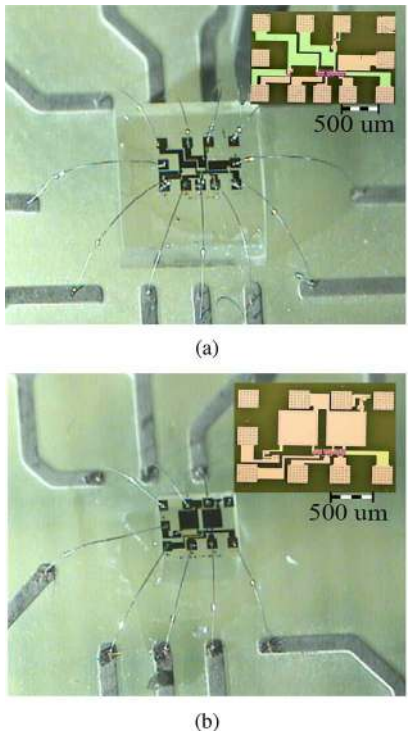

Fig. 7. Proposed bootstrap amplifier fabricated circuits after wire-bonding and the corresponding micrographs in the inset. (a) External capacitance. (b) On-chip capacitance.

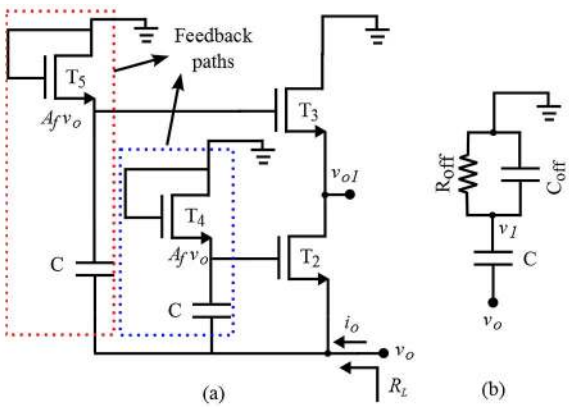

Fig. 8. Active load (a) Schematic (b) Feedback path (C, T4) or (C,T5).

$$A_f = \frac{v_1}{v_0} \tag{5}$$

where

$$v_1 = v_0 \frac{(R_{OFF} // \frac{1}{sC_{OFF}})}{\frac{1}{sC} + (R_{OFF} // \frac{1}{sC_{OFF}})} \tag{6}$$

since R_{OFF} is very high, it can be simplified to

$$v_1 = v_0 \frac{1}{1 + \frac{C_{OFF}}{C}}$$
$$A_f = \frac{v_1}{v_0} = \frac{1}{1 + \frac{C_{OFF}}{C}}. \tag{7}$$

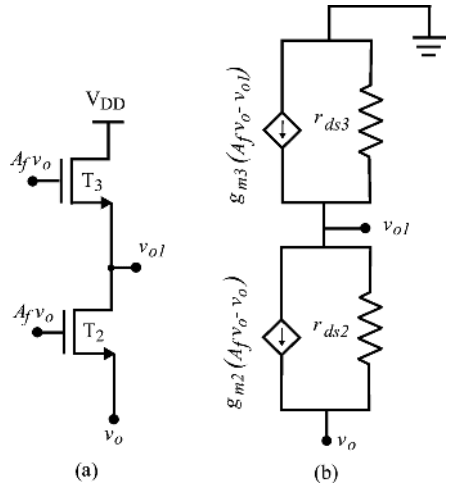

Fig. 9. (a) Simplified load (b) Corresponding small signal equivalent circuit.

Consequently, the amplifier with the simplified load can now be redrawn in the form shown in Fig. 9. Assuming all transistors with the same small-signal parameters, $A_f \approx 1$ and that $g_m \gg g_{ds}$,

$$i_o \approx \frac{g_{ds}^2}{g_m} v_o$$
$$R_L = \frac{v_o}{i_o} \approx g_m r_{ds}^2 \tag{8}$$

The "Amp" gain is then given by

$$\frac{v_0}{v_{in}} = -g_m(r_{ds} // g_m r_{ds}^2) \tag{9}$$

which can basically be reduced to the intrinsic gain of the input transistor. This gain could be increased even further by employing a cascode driver.

IV. Results and Discussion

In order to simulate the above circuits, the developed Verilog-A neural model is used in Cadence Virtuoso Spectre simulator. Since the TFT intrinsic capacitance is not characterized, approximate values of bias dependent capacitance (c_{gd} and c_{gs}) are calculated from the Meyer's capacitance model for FETs, with a relative dielectric constant (ϵ_r) of 10.5 for the dielectric material. In addition, the load impedance offered by the measuring cable (10 M Ω//16 pF) is also considered for all circuits. The power supply is 20 V.

A. Buffer

Simulation results with the measured circuit response are shown in Fig. 10. Under the load conditions described above, this circuit presents a bandwidth of 40 kHz.

B. Adder-Subtractor

Functional verification as subtractor and adder is carried out for the following stimulus,

$$v1 = 9 + sin(2\pi f_1 t),$$
$$v2 = 4.5 + 0.5 * sin(2\pi f_2 t). \tag{10}$$

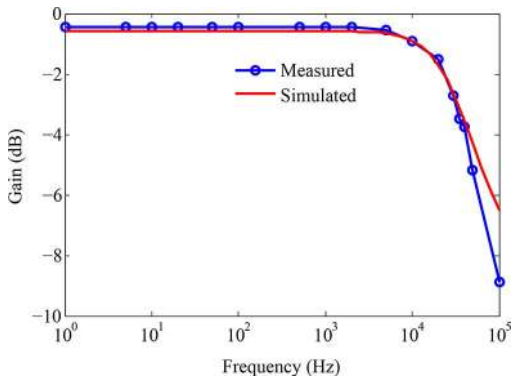

Fig. 10. Source follower simulation and measured circuit response.

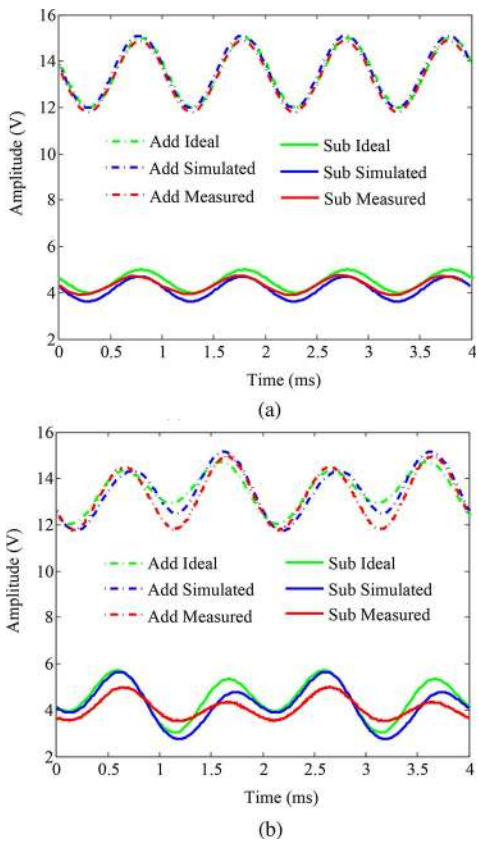

Fig. 11. Adder-subtractor functional verification from simulation, measurements, and expected value. (a) Same frequency. (b) Different frequency.

Verification is performed with two input signals (v_1 and v_2) with the same frequency $f_1 = f_2 = 1$ kHz and also with different frequencies $f_1 = 1$ kHz and $f_2 = 500$ Hz. Since the ANN verilog-A model cannot characterize the bias stress effect, a minor mismatch between the simulated and measured circuit response can be observed in Fig. 11. Non-idealities of the devices such as output resistance (r_{ds}) and minor mismatches between them are the other possible causes for the deviation observed between the ideal and the measured/simulated response. However, all outcomes show the same trend, which also demonstrates that the model is able to capture the device behavior.

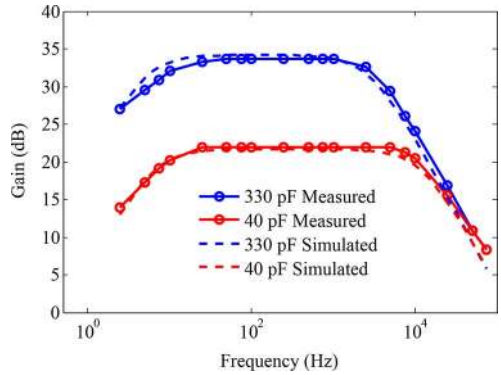

Fig. 12. Gain variation with respect to external and on-chip capacitance in high-gain amplifier. Dashed lines represent simulated data, solid lines with circles represent measured response.

TABLE I
PROPOSED HIGH-GAIN AMPLIFIER PERFORMANCE COMPARISON WITH LITERATURE

Circuit	No. of TFTs	C (pF)	Power (mW)	Bandwidth (kHz)	Mid-band gain (dB)	Load
Amp	5	40	0.576	20	22	10 MΩ//16 pF
Amp	5	330	0.576	5	34	10 MΩ//16 pF
[12]	16	-	0.9	54	18.7	1 MΩ//2 pF

C. High-Gain Amplifier (Amp)

The "Amp" gain variation with respect to C is presented in Fig. 12. For high C values (330 pF), external capacitors are utilized together with the circuit in the chip presented in Fig. 7(a). The second circuit uses on-chip capacitors with smaller values (40 pF) as presented in Fig. 7(b).

Transistors $T_1 - T_3$ were designed with the same aspect ratios ($W = 160\ \mu$m and $L = 20\ \mu$m) with fingered layout, while, T_4 and T_5 were set with $W = 10\ \mu$m and $L = 20\ \mu$m in a direct-layout structure. Fig. 12 presents the Amp frequency response with different values of capacitance (C), including a load (from the measuring cables) similar to the above mentioned circuits. From Fig. 12, it can be noticed that a higher value of C leads to an improvement in the gain, since the feedback factor becomes closer to unity, as shown in (7). A comparison of circuit complexity, power consumption, bandwidth and gain is presented in Table I. It can be noticed that a significant improvement in the gain and reduction in the power consumption is accomplished with the proposed capacitive bootstrapping technique.

V. CONCLUSION

Various analog circuit blocks, such as a buffer, adder-subtractor, and a high-gain amplifier were successfully designed and characterized using a-GIZO TFT. The simulation results, accomplished with the developed neural models, were in agreements with the measured response, showing the effectiveness of the modeling procedure. A new double-bootstrap amplifier was proposed for gain improvement. To the authors' knowledge, it presents the highest gain reported so far from a single-stage

topology, with a-GIZO TFT technology. This gain could be increased further by augmenting the total active load with a cascode driver, instead of the single common-source transistor.

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