Analog Decoding and Beyond

Hans-Andrea Loeliger
ISI / ETH Zentrum
CH-8092 Zürch, Switzerland
e-mail: loeliger@isi.ee.ethz.ch

I. Introduction

In 1998, Hagenauer [6, 7] and Loeliger et al. [9] independently proposed to decode error correcting codes by analog electronic networks. In contrast to previous work on analog Viterbi decoders (e.g. Shakiba et al. [15] and several others before, see [10]), the work both by Hagenauer and by Loeliger et al. was inspired by "turbo"-style decoding of codes described by graphs [5, 16, 17]. Large gains, in terms of speed or power consumption, over digital implementations were envisaged. More complete accounts on these new analog decoders were given in [8] and [10, 11].

Since 1998, much effort has been spent towards turning these ideas into working chips. While only decoders of "toy" codes have so far been successfully manufactured, extensive simulations of such circuits have not revealed any fundamental problems. Some progress has also been made in analyzing the effects of transistor mismatch [12]. While much remains to be learned, this author feels confident that analog decoders will eventually find their way into applications.

The present paper, rather than reporting on circuit details, offers some thoughts on "the bigger picture"—the underlying principles, motivations, and possible directions of future research beyond those mentioned in [10].

II. Power-Efficient Computation

It is commonplace that analog circuits are sensitive to noise, temperature, and component variations, and are therefore hard to design and expensive to manufacture. However, this is not the whole truth on analog computation. First, it has always been known that analog computation is sometimes much faster or less power consuming than digital computation. Second, the most interesting modes of analog computation may yet remain to be discovered. Indeed, Mead [13] has demonstrated unconventional adaptive analog systems for a number of signal processing tasks (primarily in image processing) that share the robustness of digital systems but use several orders of magnitude less power. Mead also observed a surprising similarity between the physics of CMOS transistors in subthreshold mode and that of nervous cells; both are essentially characterized by the Boltzmann (i.e., maximum-entropy) distribution of charged particles in a potential field. It is plausible that information processing in living organisms is highly power efficient, and the prospect, suggested by Mead, of mimicking its principles in silicon circuits is intriguing. However, we are still far from understanding these principles.

A main problem with traditional analog computation is the convention to represent some real quantity X as the potential of (or the current through) a single wire. Clearly, the signal-to-noise ratio of a single wire is finite and decreasing with VLSI miniaturization. Any reliable representation of signals must therefore use *several* wires. Indeed, the robustness of digital circuits is due not only to quantization, but to the fact that each wire represents only one bit. In principle, nothing prevents us from using "distributed" signal presentations also for analog computation.

With further miniaturization, the signal-to-noise ratio may become too low even for (uncoded) digital representations, so that some sort of coding will be required. With such coding, however, the well-known advantages of using "soft-decision" information can only be exploited by *analog* circuits.

III. Canonical Circuits

The new analog decoders belong to a tradition of circuits that solve nontrival nonlinear problems *exactly*. In a research monograph published in 1959 [4], Dennis investigates the correspondence between a class of mathematical optimization problems—linear and quadratic "programming" with inequality constraints—and networks of resistors, sources, and ideal diodes (with zero voltage drop in the forward direction; the basic observations motivating that study are credited to S.J. Mason and N. Arden). Using a different type of "ideal" diodes (with constant positive voltage drop in the forward direction), the "diode decoder" of [2,3] solves the shortest path problem in a directed graph. Finally, as pointed out in [9, 10], the single circuit of Figure 1 (with bipolar or subthreshold CMOS transistors, with or without the dashed box) gives rise to a large class of "probability gates" or "sum-product modules", the building blocks of the analog decoders both by Loeliger et al. and by Hagenauer and Moertz et al. [14]. The fact that such fundamental computations with probabilities are carried out *exactly* by these simple transistor circuits suggests some deeper "isomorphism" between probability propagation in factor graphs and some kind of "network of Boltzmann distributions" that describe the physics of such circuits at the electron level.

IV. Applications: Decoding and Beyond

Potential applications of analog decoding include very high speed and very low power decoders that cannot be

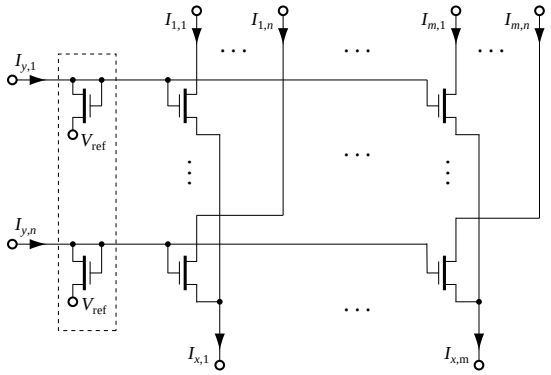

Figure 1: General probability product circuit.

built with digital technology. Analog decoders might also prove useful in areas like inter-chip and intra-chip communication. (For a simple example in this direction, see [1].) Beyond that, it is likely that similar circuits can be used for *adaptive* signal processing such as, e.g., combined decoding and adaptive equalization.

More generally, the whole area of analog front ends of communication receivers appears to offer opportunities for information theoretic thinking—allowing for redundancy and focussing on the preservation of information rather than on linearity. Much interesting work lies ahead.

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