Analog dithering techniques for highly linear and efficient transmitters

Analog Dithering Techniques for Highly Linear and Efficient Transmitters

Foad Arfaei Malekzadeh

Front Cover:

Graphical description of dither averaging, Introduced in chapter 2

Back cover:

PCB photo of the current mode Class D amplifier, with common mode LFD, presented in chapter 8 and short CV of Foad Arfaei Malekzadeh

Analog Dithering Techniques for Highly Linear and Efficient Transmitters

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To my wife, Sahar,

and to my parents

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Contents

Glossary

Symbol	Description
$f_{NL}(.)$	Nonlinear input-output operator
$f_{NL}^{*}(.)$	Linearized (equivalent) nonlinear function after dithering and filtering
f	Real frequency (Hz)
f_r	Central frequency of the band-pass message signal (Hz)
ω_r	Central frequency of the band-pass message signal (rad/sec)
f_d	Central frequency of the dithering signal (Hz)
ω_d	Central frequency of the dithering signal (rad/sec)
Δf	Bandwidth of the input signal (Hz)
$\Delta\omega$	Bandwidth of the input message signal (rad/sec)
ω_Δ	The difference between ω_r and ω_d
$*$	Convolution operator
$p_d(r)$	Probability distribution of the message signal r
$P_d(r)$	Cumulative probability distribution function of the signal r
$\mu(\alpha < r < \beta)$	Amount of time of the time spent by the signal r between values α and β
ω	Radian frequency (rad/sec)
s	Complex radian frequency (rad/sec), in Laplace transformation
$d(t)$	Dithering signal
$d_H(t)$	Dithering signal, high frequency
$d_L(t)$	Dithering signal, low frequency
$D_H(\omega)$	Fourier transform of the high frequency dithering signal
$D_L(\omega)$	Fourier transform of low frequency dithering signal

A	Amplitude of the dithering sinusoid
$r(t)$	Real Gaussian message signal
$r[m]$	Discrete time sampled signal of $r(t)$
$r_c(t)$	Complex Gaussian message signal
$r_g(t)$	A generic message signal
$\tilde{r}(t)$	Complex envelope of the complex Gaussian signal $r_c(t)$
$r_1(t), r_2(t)$	Real and imaginary parts of the input complex envelope
σ_r	Root mean square value of the signal r
σ_d	Root mean square value of the signal d
$x(t)$	Combination of the dithering and message signals
$\langle x(t) \rangle_k$	k'th order average of signal $x(t)$
ω_s	Sampling frequency in multi-frequency averaging method
$y(t)$	Direct output of the nonlinear block f_{NL} before filtering
N_{tones}	Number of tones in a multisine
f_{res}	Tone spacing (frequency resolution) of a multisine (Hz)
ω_{res}	Tone spacing (frequency resolution) of a multisine (rad/sec)
$y^*(t)$	Output of the equivalent nonlinearity
$H(j\omega)$	Output reconstruction filter, band pass or low pass
$h(t)$	Impulse response function of the filter $H(j\omega)$
$h[m]$	Discrete time impulse response of the filter
$R_{xx}(\tau)$	Autocorrelation function of signal $x(t)$
$S_{xx}(\omega)$	Power spectral density (dBm/Hz or W/Hz).
$\Im(x(t))$	Fourier transform operator on function $x(t)$
$\mathcal{L}(x(t))$	Laplace transformation operator on function $x(t)$
DFT	Discrete Fourier transform
FFT	Fast Fourier transform
$IDFT$	Inverse DFT operator
P	Number of harmonics for a harmonic multisine dither
$\theta_r(t)$	The angle between the complex envelope phasor and real x axis
$\theta_1(t)$	The angle between the superposition complex envelope phasor and real x axis
$\overline{r_1}(t)$	Vector superposition of the sinusoidal dither complex envelope of the message signal
$g_0(r)$	The dc term in the Fourier series representation of the output of the nonlinearity, for low pass input r.
$g_m(r)$	Amplitude of the higher order dithering harmonics, in Fourier series.
$\bar{y}$	Time domain or statistical average of the time domain signal y
B	Constant dc input to the nonlinear block
$w_i(\tau)$	Impulse response of the branch number $'i'$, in the parallel filter bank approximation
$x_i(t)$	Input signal to branch number $'i'$ in equivalent parallel filter bank approximation to the nonlinearity
$y_{ai}(t)$	Output of the filter number $'i'$ in the parallel filter bank
$y_a(t)$	Output of the parallel filter bank
$y_r(t)$	Difference of the linear approximation and original nonlinearity

$w_A(\tau)$	Optimum filter impulse response for single sinusoid input to the nonlinear block
$N_A(A,\omega)$	Single sinusoidal input describing function, frequency dependent
$N_{A_i}(A_1, A_2, \dots, A_N, \sigma_r, B)$	Describing function gain of combination of N sinusoids, random signal and bias, corresponding to the sinusoidal number $'i'$.
$M_{m,n,A}(A,B)$	Frequency translated describing function for two in put sinusoids at frequencies ω_A,ω_B, and amplitudes A,B respectively, for cross-modulation orders m and n.
$P_{m,n}(A,B), Q_{m,n}(A,B$	Real and imaginary parts of $M_{m,n}$ respectively
p_{lm}	Coefficients of the surface fit for i_D versus v_{GS} and v_{DS}
α(t)	Instantaneous duty cycle of the output pulse train
η_P	Coding efficiency of the output pulse train
D	Upper level of the switched mode PA (Volts or Amperes)
V_{DD}	Supply voltage of the PA (Volts)
$g_{0I}(r_1, r_2, A)$	Describing function output for real part of the input envelope
$g_{0Q}(r_1, r_2, A)$	Describing function output for imaginary part of the input envelope
$N_r(A,\sigma_r)$	Random part describing function for real Gaussian combined with a sinusoid with amplitude A
$N_A(A,\sigma_r)$	Sinusoidal part describing function for real Gaussian combined with a sinusoid with amplitude A
$Z_L(j\omega)$	Load impedance
C_{in}	Input equivalent capacitance in the parasitic model
C_f	Feedback equivalent capacitance in the parasitic model of VMCD
C_{out}	Output equivalent capacitance in the parasitic model
g_{c0}	On state conductance of the switch
$R_{ds,on}$	On-state resistance of the switch
$R_{ds,off}$	Off-state resistance of the switch
$Z_s(j\omega)$	Source impedance
$N_I(\sigma_r, A)$	Describing function for real part of the input envelope
$N_I(\sigma_r, A)$	Describing function for imaginary part of the input envelope
P_{dc}	DC power consumption of the switched mode PA
P_{out}	The power delivered to the load of the switched mode PA
y_c	Fully correlated output part of the switched mode PA
y_u	Uncorrelated output part of the switched mode PA
y_{uf}	Uncorrelated output part of the switched mode PA, including the negative feedback effect in the closed loop
$\delta(t)$	Dirac delta function
$\delta'(t)$	Doublet function
$c_k(A,\sigma_r)$	Correlation coefficient order k
i, q	Real in-phase and quadrature input signals respectively
Q	Memory span in the W/H memory model

$H_k(r)$	Hermite polynomial of order k
$J_k(r)$	Bessel function, first kind, order k
$G_A(A,B,\omega)$, $G_B(A,B,\omega)$	Calculated voltage gain of the equivalent parasitic model at frequencies ω_A, ω_B, with amplitudes A, B
$G_{m,A}(A,B,\omega)$, $G_{m,B}(A,B,\omega)$	Measured voltage gain of the equivalent parasitic model
ω_{LC}	Limit cycle oscillation frequency
G_F	Forward path gain in the feedback loop
G_s	Subtraction gain in the negative feedback loop
η	Power added efficiency
$G_f(\omega)$	Forward path gain in a feedback loop
$G_s(\omega)$	Subtraction gain in the feedback loop
σ_{in}	rms value of the message signal at the CDA input
$p(t), \widetilde{p(t)}$	Complementary input command signals of the CMCD
$\|CMD\|_1$	L_1 norm of the cross modulation
f_{CMD}	Cross modulation frequency
$Z_L(j\omega)$	Load impedance versus frequency
$G_L(\omega_{LC})$	The gain of the loop except CDA at the limit cycle frequency
f_D	Nonlinear FIR operator
$g(x,\dot{x})$	First order functional form of the differential equation of nonlinear system
R_p, L_p, C_p	Parallel tank resistance, inductance and capacitance
L_s, C_s	Series resonator inductance and capacitance
R_L, C_L	Equivalent parallel resistance and capacitance of the current buffer in the Gilbert cell mixer

Abbreviation	**Description**
EVM	Error vector magnitude
$ACPR$	Adjacent channel power ratio
NPR	Noise power ratio
$MTPR$	Multi tone power ratio
$NBGN$	Narrow band Gaussian noise
DF	Describing function
PDF	Probability distribution function
$RPDF$	Rectangular PDF (uniform)
EF	Absolute voltage gain error function
DE	Drain efficiency
$VMCD$	Voltage mode Class-D
$CMCD$	Current mode Class-D
CMD	Cross modulation
CDA	Class-D amplifier
$SMPA$	Switched mode PA
$SOPA$	Self-oscillating Class-D

LCA	Limit cycle amplifier
SDM	Sigma delta modulator
$ASDM$	Asynchronous sigma delta modulator
LP	Load pull
LSB	Least significant bit
$MILP$	Mixed integer linear programming
PAE	Power added efficiency
LFD	Low frequency dithering
HFD	High frequency dithering
MFA	Multi frequency averaging
HB	Harmonic balance
CE	Circuit envelope method
$MSine$	Multisine
TD	Time domain approach
$VIOP$	Volterra input output polynomial mapping
EER	Envelope elimination and restoration
ET	Envelope tracking
$PISPO$	Periodic in same periodic out
DF	Describing function
$SIDF$	Sinusoidal input describing function
$TSIDF$	Two sinusoidal input describing function
$RIDF$	Random input describing function
$RSIDF$	Random plus sinusoidal describing function
PA	Power amplifier
ADC	Analog to digital convertor
DSP	Digital signal processing
EER	Envelope elimination and restoration
ET	Envelop tracking
WH	Wiener Hammerstein model
PLM	Power load modulation
CMD	Cross modulation
PWM	Pulse width modulation
CW	Continuous wave
$OFDM$	Orthogonal frequency division multiplexing
$WCMDA$	Wideband code division multiple access
$QPSK$	Quadrature phase shift keying
$SNDR$	Signal to noise and distortion ratio
RCE	Relative constellation error
$3G$	Third generation project partnership

Chapter 1

Introduction

Power amplifiers are the most power hungry and perhaps the most expensive part of the wireless transmitters in the RF chain. The key differentiators among different PAs are cost, yield, weight, efficiency, ease of design, reliability, ruggedness and high temperature operation. Generally, the most important of these requirements are linearity and efficiency. Modern communication systems employ high crest factor signals as a result of the urgent need of higher bandwidth efficiency. Achieving mandatory linearity constraints along with competitive efficiency requirements becomes more difficult with increased signal crest factor [37].

In the field of PA design, for linear and efficient operation, two distinct trends exist, which are either using an inherently linear PA (with poor efficiency) with supply or load modulation techniques (e.g. envelope tracking) to enhance their efficiency, while retaining the linearity (with pre-distortion or Cartesian feedback), or using inherently nonlinear (but power efficient) PAs and try to linearize them.

A sub-class of the efficient power amplifiers is known as the class of switched mode PAs (SMPA). These PAs have different classes of operation, while all of them have one thing in common: they move fast between the saturation and off-state of the devices, which makes either the voltage or the current of the device terminals of these amplifiers negligible, hence decreasing the power loss, and thus increasing the efficiency. Among them, operation classes D, E, F, F^{-1} etc. can be named. Another similarity among them is that they all suffer from very poor linearity, i.e. because they switch between cut-off and saturation levels, they cannot reflect the real envelope variations of the input signal on the output signal, which is usually

switching between two constant levels. There are a couple of techniques, for linearization of SMPAs; among them are EER and out-phasing.

1.1 Motivation

In order to obtain the required linearity-efficiency compromise with switched mode power amplifiers, various techniques are being employed in current wireless systems. Among them are polar modulation [94] and out-phasing techniques [95]. These have been discussed in detail. They use the real envelope signal to modulate a switched-mode amplifier output, or convert the modulated signal to a summation of two constant-envelope signals to be processed by switched mode PAs. The major drawback of all those techniques is the complicated signal processing that is needed for wave shaping and the poor efficiency of the tracking amplifier, which affects the overall linearization efficiency.

Besides these techniques, there are also time-domain encoding techniques, like sigma-delta modulators (SDM) or pulse-width modulators (PWM). They show good linearity-efficiency performance. In those techniques, the amplitude and phase information of a digitally modulated message signal is encoded in limited number of quantized levels of an output pulse train (e.g. zero and one for binary encoding) and their zero crossings. This makes it possible to use an efficient switched mode power amplifier like class D. The major drawback is a relatively high clocking (or sampling) frequency, which in turn will degrade the power efficiency due to more reactive power loss.

There is also a class of signal processing techniques which use an external signal to change the linearity behavior of hard nonlinearities, pruned as dithering techniques. The generic name of 'dithering' is used for this phenomenon, which is explained in the following section.

1.2 Dithering concept

The term 'dither' was published in books on analog computation and hydraulic controlled guns shortly after the war [96], [97]. In [108], it is stated that one of the earliest applications of dither came in World War II. Airplane bombers used mechanical computers to perform navigation and bomb trajectory calculations. These mechanical computers performed more accurately when flying on board the aircraft, and less well on ground. Engineers realized that the vibration from the aircraft reduced the error from sticky moving parts. Instead of moving in short steps, they moved more continuously. Small vibrating motors were built into the mechanical computers, and their vibration was called dither from the Middle English verb "diddderen" meaning "to tremble" [108]. Dither successfully makes a digitization system a little more analog in the good sense of the word.

The concept of dithering to reduce quantization patterns was first applied by Lawrence G. Roberts [4] in his 1961 MIT master's thesis [98] and 1962 article [6] though he did not use the term dither. By 1964 dither was being used in the modern sense, described in [99].

The concept of dithering as a linearization technique is exploited in many applications. As an example, dithering has applications for linearization and for quantization noise reduction. Many analog-to-digital converter applications require low distortion for a very wide dynamic range of signals. Unfortunately, the distortion caused by digitizing an analog signal increases as the signal amplitude decreases, and is especially severe when the signal amplitude is of the same order as the quantizing step. In digital audio applications, for example, low-level signals occur often, sometimes alone and sometimes in the presence of larger signals. If these low-level signals are severely distorted by the quantization process, the usefulness of the system is greatly diminished. It is, in fact, possible to reduce the distortion, and also to improve the resolution below one LSB (least significant bit), by adding noise (or dither) to the signal of interest. For ideal converters, the optimum dither is white noise at a voltage level of about 1/3 LSB rms. The addition of dither effectively smoothes the ADC transfer function, which normally has a staircase-like appearance, but it comes with a slight reduction of the signal-to-noise ratio [100], [101].

1.3 Problem statement

The topic of the current thesis lies in the realm of linearized SMPA design. Assuming that we have a static nonlinear input output transfer function, the problem is illustrated in Fig. 1-1. We have a signal that is called $r_g(t)$ which is a band-limited (either a low pass or band-pass signal), and we have a static nonlinear input-output characteristic $y = f_{NL}(x)$, which is a single input

single output mapping function to describe the nonlinear block. The block resembles many types of common switched mode power amplifiers in which the switching device in the block is changing its state between off and saturation states, if we ignore the memory effects. The

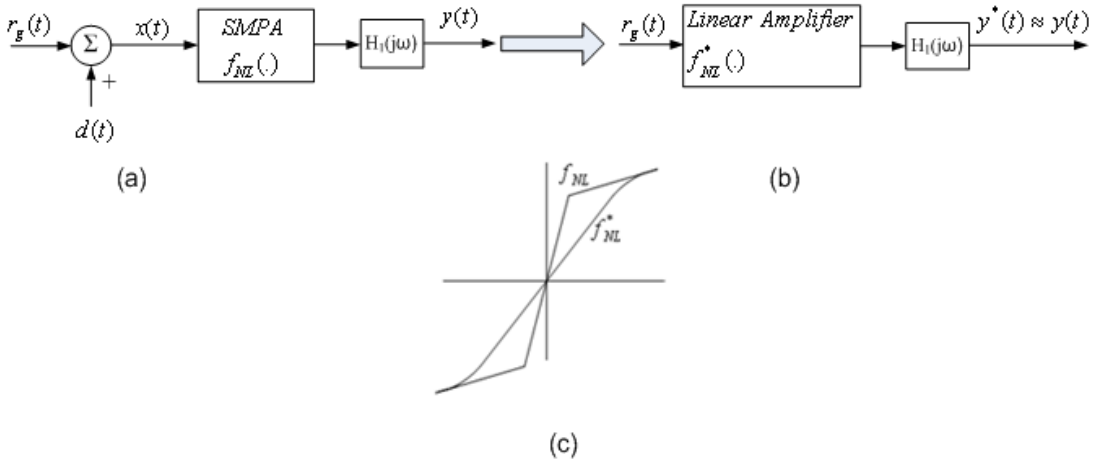


Fig. 1-1: (a): The problem of dithering, as the dither signal $d(t)$, combined with a generic input signal $r_g(t)$ is applied to an single input single output transfer characteristic $y = f_{NL}(x)$;(b): the equivalent problem formulation, and(c): the relationship between the smoothed equivalent function and original function

goal is to find the effect of the dithering on the input-output characteristics and to find the conditions that must be fulfilled to satisfy this transformation. Therefore, the main problem can be stated as follows:

> Is the dithering technique a feasible solution for simultaneous improvement of linearity and efficiency?

In view of the mentioned problem, the following questions can arise:

1. How can a generic theoretical framework be developed to formulate the linearity and efficiency parameters of the dithered system?
2. What are the effects of the system parameters on the dithered performance?, i.e.:
    a. What is the effect of the amplifier slope gain on overall performance?
    b. What is the effect of the process technology related reactive loss on the overall performance?
    c. Which circuit topologies show promising performance under dithering?
3. Which kinds of signals (e.g. sinusoids, random, ramp, etc.) can be used as dithering for linearity-efficiency improvement?
    a. What is the effect of the dither probability distribution on linearity and efficiency?
    b. What is the effect of frequency content of the dither on linearity and efficiency?
    c. What is the effect of dither frequency on linearity?
    d. What is the effect of the dither level on the linearity-efficiency performance?
    e. Are there any optimum frequency allocations for dither, for best linearity-efficiency compromise? If so, how can those optimum points be obtained?
4. Is there any general design procedure for a dithered amplifier?
5. Can the insight achieved from dithering analysis lead to new analog dithering applications?

1.4 Limitations of existing analysis methods

The status of current simulation techniques covers a wide range of studies for specific applications. In the field of power amplifiers, generally two different analysis approaches are taken, which are circuit simulation approaches and behavioral-modeling approaches, also called averaging approaches; both classes are illustrated in Fig. 1-2.

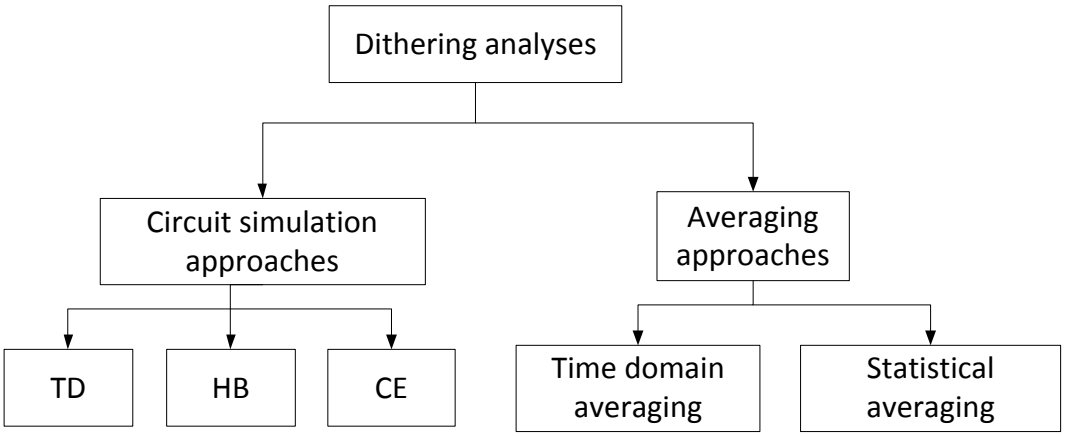


Fig. 1-2: Different approaches taken in the analyses of dithered SMPA

The circuit simulation approaches, like time domain (TD), harmonic balance (HB) or circuit envelope (CE), are numerical state of the art techniques which are suitable for any circuit topology with any kind of process technology. There are, however, many difficulties and problems in using these methods. Among them are the convergence problems, and the simulation time. In HB or CE, the number of harmonics and mixing orders should be high enough, to get accurate enough results [102], [103]. Moreover the circuit simulation techniques are not insightful regarding the intuitive effect of the dither properties on the nonlinearity.

As an alternative approach, averaging techniques are fully developed for dither problems in which the dither frequency approaches infinity; the limits imposed on the dither frequency are abstract and somehow unrealistic, but in this thesis we will show that they can be extended to be applied to real scenarios, for linearization of switched mode power amplifiers.

1.5 Aim of the project

The main objective of this thesis is to investigate new dithering based techniques and topologies, in order to linearize switched mode amplifiers and at the same time improve their linearity-efficiency trade-off.

The effect of the dither frequency content and its statistical properties on linearity and efficiency of the dithered amplifier will be investigated. Behavioral modeling of the linearity metrics versus the dither level will be performed for general applications, including random input signals. Also an effort will be made in order to find the generic nonlinear metrics of a dithered system for wireless applications, like adjacent channel power ratio and error vector magnitude. Moreover design procedures are investigated for proper topologies, and for real applications.

1.6 Proposed approach

The approach taken in this thesis is the averaging-based technique to describe the transformation and the second order effects of the dither on nonlinear systems. The averaging techniques are based on the method developed by Bussgang and Zames et.al. in [34], [93] and later on used by Gelb et.al [4] to develop the describing function theory.

The idea of equivalent nonlinearity in nonlinear control theory will be applied to dither frequencies which are either close to or even below the input message signal. Therefore, techniques will be developed to extract the smoothing effect of the dither in terms of realistic linearity metrics that are used for real power amplifiers in wireless applications.

1.7 Thesis outline

This thesis is structured as follows: chapter 2 introduces the idea of dither, categorizes the dither based on its frequency content compared to the message signal, and develops the idea of equivalent nonlinearity. Fourier series and statistical averaging methods are introduced to extract the equivalent function.

Chapter 3 introduces the idea of describing function as a tool for correlated analysis of the nonlinear blocks. Chapter 4 presents the circuit topologies and architectures that are suitable for application of dithering to obtain a linear and efficient PA in a real scenario. Chapter 5 deals with the linearity analysis, of the dithered PA, based on describing function and orthogonalization of the output components, through which all of the important PA metrics are achieved. Chapter 6 deals with the second order spurious effect and its relationship with the frequency content of the dither, and methods to optimize the dither signal, or to minimize the resulting spurious components.

Finally, all the theoretical findings are put into test, through the systems that were realized and evaluated in chapters 7 and 8. In those chapters, two open-loop switched-mode amplifiers and one self-oscillating architecture are realized and tested, and the expectations are approved by measurement results.

Chapter 9 discusses the possible applications of dithering in future systems, and the potential of the averaging techniques for mixer analysis.

Chapter 2

Dithering

Analog dithering is an elegant way to modify hard nonlinearities. In servomechanism study in control theory, dither has been defined as a high frequency signal, compared to system dynamics, that will reduce the sector size of the nonlinear characteristic [34, 64]. This is in turn related to system characteristics such as stability and linearity. However this definition does not cover all of the possible applications of the concept for any kind of dynamics and input frequency content to the system.

In this chapter, first a general and broader definition of the dithering concept is introduced. Then the concept of 'equivalent nonlinearity' is defined. This functional equivalence explains the linearization process in terms of dithering and simplifies the analysis of the dithered system. The insight obtained from equivalent nonlinearity can be utilized to find the distortion of amplifiers.

Based on the dithering frequency, the dithering process can be divided to high and low frequency. If the dither frequency is much higher than the maximum input frequency, it is called high frequency dithering; reversely, if it is lower than the zero crossing rate of the input bandpass signal, it is called low frequency dithering.

Two approaches can be followed in parallel, to obtain the equivalent nonlinearity function, which are called Fourier series method and the statistical method. The first approach is based on Fourier expansion, the second one relies on the statistical averaging concept. The advantages and disadvantages of each method are discussed in detail.

The frequency content of the high and low frequency dithering are studied based on the generic output spectral form. A different bandwidth constraint formula is derived for each. Afterwards the statistical conceptual model is applied to high and low frequency to derive the equivalent nonlinearity.

2.1 Dithering concept

Dithering is injection of an external signal to a linear or nonlinear system to obtain several possible objectives. Among them are augmenting the linearity of the open or closed loop system, robustness, and asymptotic stability, for a general class of nonlinear apparatus, reduction of quantization noise in data convertors; and adaptive enhancement of the closed loop linearity. The dithering can also be utilized to affect the dynamic behavior of the system and stop undesired chaotic behavior or undesired limit cycle oscillations in the system, or alleviate the resonance jump phenomenon in sliding mode control applications [4].

The dithering signal may be analog or digital, and can have any statistical and spectral characteristics. It can be a random or a deterministic signal and it can be correlated or uncorrelated to the input signal. Being a random signal, its value at each moment can be dependent or independent of its previous values in time, or in the other words it can be with memory or memory

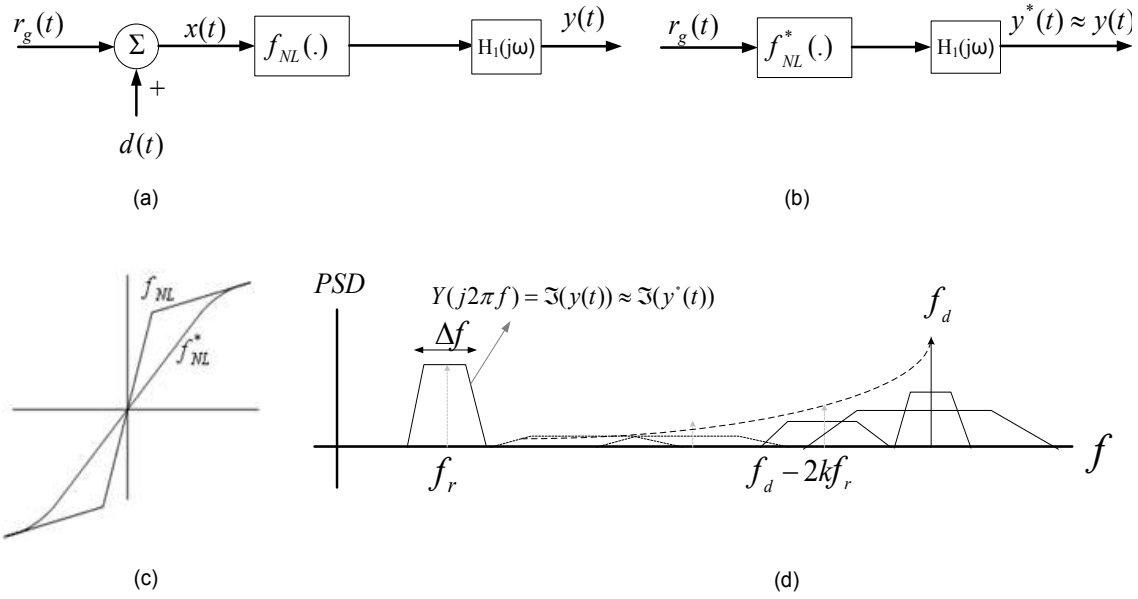


Fig. 2-1:(a) Continuous time dithering applied to a nonlinear apparatus; (b): equivalent nonlinearity concept model; (c): the shape of a hard nonlinearity f_{NL} is effectively transformed to softer one f^*_{NL}; (d): the output frequency domain content of the linear operator f_{NL}.. f^*_{NL} will generate the same baseband part as f_{NL} at the output of the filter.

less.

In case of having a nonlinear system, described with a general input output nonlinear tor $y = f_{NL}(x)$, the concept of the dithering is illustrated in Fig. 2-1-a, wherein signal $d(t)$ is the continuous time dithering, $x(t)$ is the input signal, and $y(t)$ is the output signal of the nonlinear system. The output of the system is related to the total input as:

$$y = h_1(t) * f_{NL}\big(x(t)\big) = h_1(t) * f_{NL}(r_g(t) + d(t)) \tag{2-1}$$

where $h_1(t)$ is the impulse response of the filter $H_1(j\omega)$. Having a mathematical description of the single-input single-output $f_{NL}(.)$ we can find the output response to any desired input. The only assumption is that the f_{NL} function is assumed to be memory-less, i.e. its output at each moment depends only on its input at the same instant.

2.2 Equivalent nonlinearity

The most important effect of dithering is *linearization* of hard nonlinear characteristics, i.e. the original nonlinearity is transformed to another one which has a smaller 'sector size'[1], as depicted in Fig. 2-1-c. This is due to the fact that the *dither effectively acts as a moving average filter, and applying this kind of process to a hard nonlinearity, will always make it softer*, provided that the proceeding filter H_1 is able to omit the undesirable spurious components at the output. This property is illustrated in Fig. 0-1-c, where the f^*_{NL} is *the equivalent (linearized) nonlinearity,* after applying dither signal $d(t)$ to f_{NL} and proceeding filtering of its output. From now on, this new (transformed) mathematical operator is called *equivalent nonlinearity*.

In other terms, equivalent nonlinearity is a new function, which includes the linearization effect of the dithering signal. If the input $r_g(t)$ is a base-band signal (extending from dc to maximum frequency of f_r), and the dithering frequency is a higher frequency, the output of the original nonlinearity will include a replication of the signal (with in-band distortion) and sidebands around the dithering signal frequency component and its higher order harmonics, as shown in Fig. 2-1-d.

The mathematical mechanism behind this phenomenon will be discussed more in the upcoming sections, and in chapter 3. So the definition of the equivalent nonlinearity implies that the output filter $H_1(j\omega)$ has enough out of band rejection to omit the sidebands around the dithering frequency (and its harmonics) resulting in an output signal processed by the $f^*(.)$ equivalent operator. The main advantages of the equivalent nonlinearity are:

1 The sector size is defined as the maximum angle between the line crossing origin, and the horizontal axis. Generally a system with less sector size is assumed to be smoother.

1. It is a single input single output system: the effect of the dithering signal is embedded within the new function; therefore we won't need to analyze the system for combination of two input signals.
2. The equivalent function is a softer nonlinearity. Hence, it is much simpler to analyze. The extreme case is having an ideal limiter, which is very memory-intensive to analyze with numerical methods (due to discontinuity of the output). The 'softened' or linearized version of it is of a lower polynomial order and is easier to analyze with commercial simulators.
3. The formulation of the equivalent nonlinearity is insightful to understand the dithering effect intuitively.

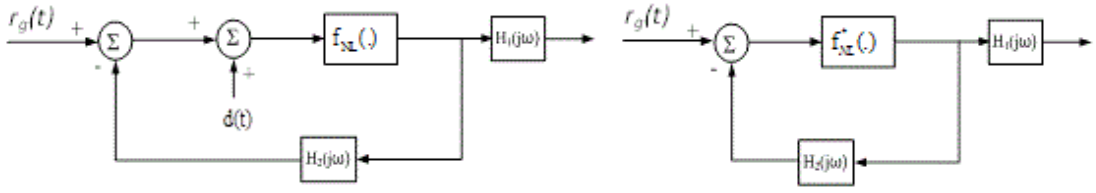
The downside of the equivalent nonlinearity model is that it does not take into account the spurious side-bands of the dither frequency that penetrate into the signal band-width. When the frequency of the dither is chosen close to the bandwidth edge, it is impossible to filter out the spurs and they affect and degrade the linearity of the system as well. This issue is illustrated in Fig. 2-1-d, where the modulated side-bands penetrate into the input signal band when we reduce the f_d.

The system in which the dithering is applied to may be placed in an environment that provides sort of feedback from output to the input, or is intentionally designed to have a feedback, as illustrated in block diagram of Fig.2-2. The same concept of equivalent nonlinearity can also be used for the analysis of dithering in a negative feedback loop, provided that the feedback filter (H_2 in Fig. 2-2) is sharp enough to effectively omit the dither component and its modulated side band spurious.

The complete analysis of the systems in Figures 2-1 and 2-2 means determination of signals in time and frequency domain in different points of the block diagram. For a linear systems analysis, everything is determined by the impulse response of the system. The output of the system is related to the input through the convolution integral.

$$y(t) = x(t) * h(t) = \int_{-\infty}^{\infty} x(\tau).h(t,\tau)d\tau \qquad (2\text{-}2)$$

or equivalently in frequency domain, $Y(j\omega) = X(j\omega).H(j\omega)$. There are also several properties attributed to the linear systems and they are considered equivalent to each other: existence



(a) (b)

Fig. 2-2 (a): Continuous time dithering applied to a nonlinear apparatus with negative feedback; (b): equivalent system, using the concept of equivalent nonlinearity.

and uniqueness of the solution for a given known input, continuous dependence of the output on the input and boundedness of the output in case of boundedness of the input.

These properties are not fulfilled even in the simplest cases of a memory-less nonlinear system. Some examples and reviews are given in [64]. Any system for which the superposition principle does not hold is defined to be nonlinear. *In this case there is no possibility of generalizing from the responses for any class of inputs to the response for any other input*. This constitutes a fundamental and important difficulty which necessarily requires any study of nonlinear systems to be quite specific. One can attempt to calculate the response for a specific case of initial conditions and input, but make very little inference based on this result regarding response characteristics in other cases.

In order to understand and be able to mathematically describe the behavior, the nonlinear system has to be described. There are several approaches to define and describe the nonlinear block performance. The analysis will be focused on the system block diagram of Fig. 2-1. The methods and necessary tools will be developed to find the response of the open loop system to some classes of input signal and the results obtained will be used for the nonlinear feedback system of Fig. 2-2. From now on, for the sake of simplicity, we limit the scope of discussion to memory-less nonlinearity, i.e. the output of the nonlinear system can only depend on its input at the same time and f_{NL} is a static single valued function. The memory effect model and analysis will be presented in section 5.3.

2.3 High and low frequency dithering

The dithering signal frequency can be classified to two different modes: dithering frequencies which are higher than the input signal frequencies, which we call high frequency dithering (HFD) and those which are below the input signal frequencies and are called low frequency dithering (LFD).

The low frequency dithering can be used for linearization of a nonlinear system, that process band-pass input signals. The band pass signals are defined as those signals which have no spectral components below a certain frequency. High frequency can be used for any kind of input

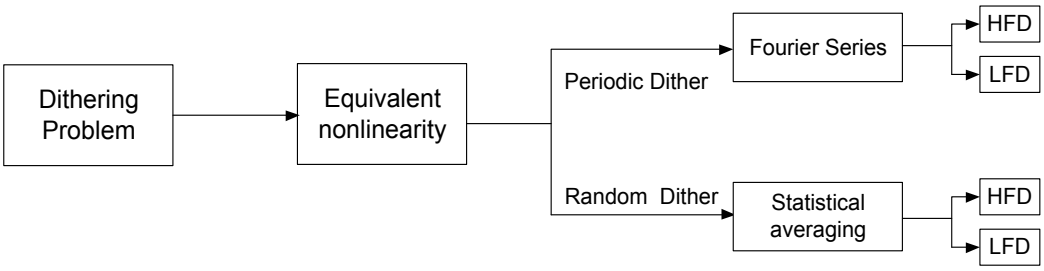


Fig. 2-3: Different approaches for random, high and low frequency dithers

signal including DC, below the dithering frequency. The main difference in formulation of equivalent nonlinearity for high and low frequency dithering is that for high frequency, the rate of variations of the dither is usually much higher than the input signal, therefore the equivalent nonlinearity is obviously time-invariant, and high frequency fluctuations are averaged out simply by a low pass filter placed at the output. On the other hand, for low frequency dithering, the dither signal dynamics is slower with regards to the signal value, but should be much higher than the envelope bandwidth. In case of low frequency dithering, the averaging process is performed on the complex envelope of the band-pass input signal. Hence in terms of instantaneous value, the system is time variant and therefore the equivalent nonlinearity versus value is meaningless. Due to this basic difference, the equivalent nonlinearity is defined versus value in high frequency and versus envelope value in low frequency dithering, as will be explained and formulated mathematically in 2.5. The spectral distribution for the high and low frequency cases imposes two different estimations of the 'linear bandwidth'[2], and those estimations are given in section 2.4.

There are two basic methods to calculate the equivalent nonlinearity, which are namely Fourier series expansion approach (assuming a periodic high or low frequency dither) or time domain averaging and statistical averaging approach.

The first approach is based on multi-dimensional Fourier expansion of the output versus input, for periodic input, while the second one is applicable to any kind of dither signal, under certain mathematical assumptions. The assumption made about the dither in the latter is weaker than the periodicity and the dither should only be 'repetitive', i.e. its value probability distribution function should repeat itself versus time. A good example of repetitive signal is a two tone signal, when the two tones are not harmonically related. By this definition all of the periodic signals are repetitive but *not* vice versa. The advantage of statistical view is that it is generic in terms of input signal, and it is applicable to a broad family of signals, including periodic signals.

The drawback of the statistical view compared to the Fourier series expansion is that it overlooks the spurious sidebands around the dithering frequency and its harmonics. These components can be harmful to the signal integrity, but sometimes are unavoidable, especially when the dither frequency is close to the signal, as illustrated in Fig. 2-1-d. When the modulated spurious sidebands penetrate into the signal band, the linearity is always compromised. On the other hand, calculation of the Fourier coefficients for a general input signal and a general periodic dither can be very time consuming, tedious and memory-intensive, especially when the number of the frequency components grows large. An alternative approach to find the equivalent nonlinearity is developed in chapter 6.

In the following parts, first an intuitive understanding of the smoothing mechanism, based on rotating vector representation, for sinusoidal dither, is introduced. Then the Fourier series based approach for memory-less nonlinearities is explained, for high and low frequency. Afterwards the statistical point of view is developed for these two modes and different formulas

[2] Linear bandwidth is the frequency range in which the spurious are low enough and the overall linearity is good.

for equivalent nonlinearity are derived, based on the value for high and envelope for low frequency dithering. Fig. 2-3 sums up the order and distinction of the two approaches to dithering problem. The memory effect can be super-imposed to the analysis on both of the approaches, and is discussed detail in chapter 5.

2.4 Rotating vector representation

An intuitive understanding of the dithering effect for sinusoidal dither can be obtained through the following expansion of the entire complex envelope around carrier frequency ω_r:

$$x(t) = \left|r_g(t)\right| \sin\left(\omega_r t + \theta_r(t)\right) + Asin(\omega_d t)$$

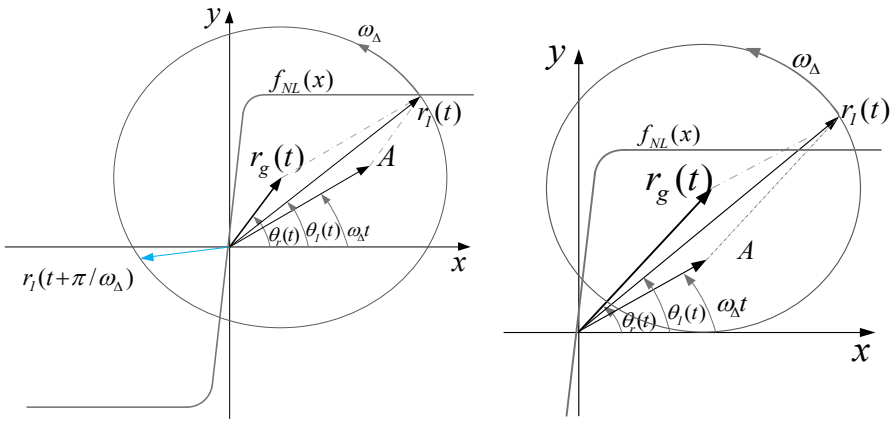
$$= r_1(t) \sin\left(\omega_r t + \theta_1(t)\right) \qquad \text{(2-3-a)}$$

while r_1(t) is the vector superposition of the phasors of the input complex envelope $r(t)$ and the dithering phasor $Aexp(j\omega_\Delta t)$, as follows:

$$r_1(t) \triangleq \left|\left|r_g(t)\right| exp\left(j\theta_r(t)\right) + Aexp(j\omega_\Delta t)\right| \qquad \text{(2-3-b)}$$

and $\omega_\Delta = \omega_r - \omega_d$.

Provided that the rotation speed of the dithering is much higher than that of the input signal



(a) (b)

Fig. 2-4: Illustration of sinusoidal low frequency dithering effect on envelope r. The effective complex envelope vector rotates around a circle with a frequency much higher than the signal bandwidth (a): Linear averaging as the superposition vector sees the negative and positive values with proportion to the signal; (b): saturated averaging, in which the time duration experienced by summation is limited to either positive or negative y axis.

complex envelope bandwidth (i.e. $\omega_d \gg \Delta\omega$), we can assume that the vector $\bar{r_g}(t)$ is not moving in time and the dither vector is rotating around it with an angular speed of ω_Δ. Then after the averaging process (through a band-pass filter around ω_r or a low pass filter from zero to frequency ω_r) the system would be effectively time invariant with respect to the input envelope $r_g(t)$.

The averaging process is depicted in the diagram of Figs. 2-4-(a, b) in the x-y plane, in which x and y represent the input and output signals of the nonlinear block respectively ($y = f_{NL}(x)$), and the imaginary part of the output complex envelope. The tip of the superposition vector $r_1(t)$ (sum of rotating A, and $r_g(t)$) moves along a circle. This circle is centered at point $r_g(t)$ and its radius is the dither amplitude A.

Depending on the relative amplitudes of the dither and signal vectors, two different situations can be distinguished as follows:

1. Linear operation: For $|r_g(t)| < A$, as illustrated in Fig. 2-4-a, the dither component acts like a moving average filter and the average of the rotating vector will be proportional to the input vector $r_g(t)$, as long as the mapping of $r_1(t)$ on the y axis passes through both positive and negative y. Intuitively, the average of the projection on the y axis will be proportional to the amplitude of the input signal $r_g(t)$ and thus the dithering makes the hard saturation function linear.

2. Saturation: When the value of $r(t)$ becomes larger than A ($|r_g(t)| \geq A$), the superposition vector $r_1(t)$ will be entirely projected on the positive (or entirely negative depending on the input sign) side of y, as shown in Fig. 2-4-b, which drives the nonlinear system into positive or negative saturation.

Hence the saturation threshold is a function of r_g/A ratio. The linearization effect will also depend on the average time spent in positive and negative sides of the x axis, which is not uniform for sinusoidal dither.

It should be noted that the same interpretation is true for the real part of the output envelope, either if the superposition signal is projected on the x axis and x is a saturation function of y instead, or using the same chart as Fig. 2-4, for another vector orthogonal to the original one. This intuitive demonstration is valid for both HFD and LFD sinusoidal ditherings.

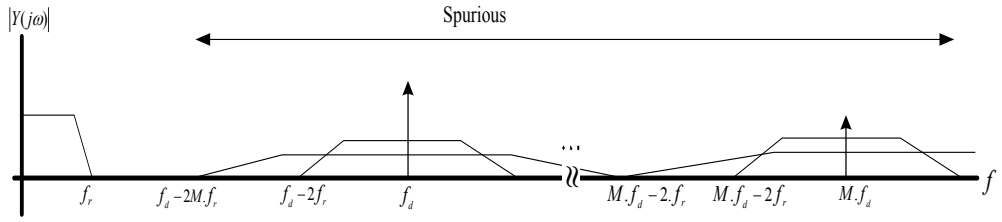


Fig. 2-5 Frequency content, the output of the nonlinear component after a high frequency dithering, with a single frequency f_d.

2.5 Fourier series approach

As long as the dithering signal is periodic, two-dimensional Fourier series expansion in combination with time domain averaging is a viable approach to extract the equivalent nonlinearity. We need to assume that the dither and signals frequency are non-commensurable, to have two degrees of freedom in Fourier series. Another way to express that condition in practical situations is to assume that the greatest common divisor of the two frequencies is much smaller than both of them: $\gcd(f_d, f_r) \ll f_d, f_r$ provided that both of the frequencies are integers. This should be true for both HFD and LFD.

2.5.1 High frequency dithering

In high frequency case, the dither signal, denoted as $d_H(t)$ is assumed to have a frequency much higher than the maximum frequency component of the input signal $r_g(t)$. Usually the fundamental frequency of $d_H(t)$, or the minimum frequency component of its Fourier transform $D_H(\omega)$ is much higher than the input signal frequency.

The dithering signal $d_H(t)$ can be expressed as:

$$d_H(t) = \sum_{m=1}^{p} D_m . \sin(m\omega_d t + \varphi_m), \quad while\ \omega_d \gg \omega_r \tag{2-4}$$

in which subscript H denotes high frequency as expressed by the condition. The output of the nonlinear operator is a function of the signal $x(t)$, which has a combination of the input signal frequency and dithering frequency. f_{NL} can be expanded in a two dimensional Fourier series as:

$$y(t) = f_{NL}\left(r_g(t) + d_H(t)\right) = \sum_{m=0}^{\infty} g_m(r_g).\sin(m\omega_d t + \varphi_m) =$$

$$g_0(r_g, D_1, D_2, \dots, D_P) + \sum_{m=1}^{\infty} g_m(r_g, D_1, D_2, \dots, D_P).\sin(m\omega_d t + \varphi_m) \tag{2-5}$$

where $g_0(r)$ is the transformed nonlinearity characteristic, shaped (linearized) by the high frequency dither d_H or the equivalent nonlinearity defined in section 2-2. There are averaging methods to achieve this term of the Fourier series which will be explained in the coming sections.

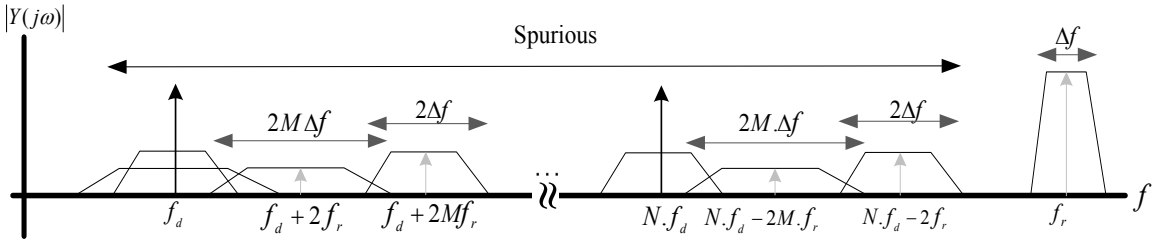


Fig. 2-6 Low frequency dithered frequency content, the output of the nonlinear component, with a single frequency f_d.

Under assumption of odd nonlinear characteristics for f_{NL}, Fig. 2-5 shows the output spectral content for a general nonlinear function f_{NL} in which the right hand term of (2-5) is truncated to 2M+1. As we see from the figure, the closest modulated sideband of the output of the nonlinearity had a widened and up converted version of the input, with intermodulation order of 2M.

2.5.2 Low frequency dithering

The injection of a dither component with the main frequency lower than the input band pass signal (f_r) can again modify and linearize the nonlinear characteristics. The dither is called d_L as:

$$d_L(t) = \sum_{m=1}^{p} D_m . \sin(m\omega_d t + \varphi_m), \quad while\ \omega_d < \omega_r$$

and the input is a band pass modulated signal around a central frequency f_r:

$$r_g(t) = Re\{\tilde{r_g}(t).\exp(j\omega_r t + \varphi_r(t))\} = |\tilde{r_g}(t)|.\cos(\omega_r t + \varphi_r(t)) \qquad (2\text{-}6)$$

As $\omega_r = 2\pi f_r$ and $\tilde{r_g}(t)$ is the complex envelope of the signal. The output Fourier series expansion can be written as:

$$y(t) = f_{NL}\left(r_g(t) + d_L(t)\right) =$$

$$\sum_{m,n=0}^{\infty} g_{mn}\left(\tilde{r_g}(t), D_1, D_2, \dots, D_P\right).\sin(m\omega_r t + \varphi_r(t) + n\omega_d t) =$$

$$g_{10}\left(\tilde{r}_g(t), D_1, D_2, \dots, D_P\right) + \sum_{m,n=1}^{\infty} g_{mn}\left(\tilde{r}_g(t), D_1, D_2, \dots, D_P\right).\sin\left(m\omega_r t + \varphi_r(t) + n\omega dt\right) \quad (2\text{-}7)$$

while again $g_{10}(r, D_1, D_2, \dots, D_p)$ is the equivalent nonlinearity f_{NL}^* defined in section 2-2 and will be derived again in part 2-6. The generic spectral domain is according to equation (2-7) is depicted in Fig. 2-6, where again like high frequency case, the odd nonlinearity order is truncated to 2M+1 instead of ∞.

If the input signal is selected '*properly*', so that the spurs don't interfere with the desired signal band, g_{10} is capable of linear amplification-processing of the input signal. This will be explained in detail in chapter 5.

When the dither frequency is selected to be much higher than the input signal, according to Fig. 2-5, the spurious sidebands won't affect the original linearized signal. This provides a way to estimate the bandwidth f_{rH}, as to avoid overlap between the M'th order sideband and original signal at the output:

$$f_d - 2Mf_{rH} > f_{rH} \quad (2\text{-}8)$$

which yields to the following equation:

$$f_{rH} < \frac{f_d}{2M+1} \quad (2\text{-}9)$$

where again the subscript H denotes high frequency dithering. By setting the M, the upper bound is derived for the bandwidth f_{rH}. The order M will depend on the order of the hard nonlinearity. Setting M=1, results in $\frac{f_d}{3}$ as the fundamental limit, which agrees with the time domain analysis in [1].

For low frequency dithering, the fundamental dithering frequency f_d has to be at least half the band-width of the input signal and the input and dithering frequencies should be incommensurable. This can be explained based on the condition of not overlapping modulated dither around input carrier at $f_r - f_d$ with the signal itself, as:

$$f_r - f_d < f_r - \frac{\Delta f_{max}}{2} \qquad \therefore \qquad f_d > \frac{\Delta f_{max}}{2} \quad (2\text{-}10)$$

The linearization process is illustrated in Fig. 2-5. The dither and its higher order harmonics will absorb the spurious cross modulations and the input signal is processed without distortion.

Based on the notation used in Fig. 2-5, a limit can be derived for the maximum bandwidth of the input band pass signal

$$\frac{m\Delta f_0}{2} < mf_d + \Delta f_{max} < f_r - \frac{\Delta f_{max}}{2} \quad (2\text{-}11)$$

while m is the integer floor function of the ratio of the two frequencies f_r and f_d, and Δf_{max} and Δf_0 are the bandwidths of the system and the output band pass filter respectively. Based on (2-10), we can write:

$$\Delta f_L = 2f_r - m\Delta f_0 \tag{2-12}$$

where L denotes the low frequency and Δf_L indicates the maximum frequency span of the input band-pass signal. Equations (2-9) and (2-12) say nothing about the optimum points for the dithering frequency. This will be dealt with in chapter 6.

2.6 Statistical approach

As explained in the previous sections, the nonlinear system characteristic effectively changes in presence of the dithering signal. The method to study and describe this phenomenon will depend on the type of the input and dithering signal and of course the nonlinear apparatus itself.

The concept of 'equivalent nonlinearity' was chosen to explain and achieve insight to the dithering effect. The terms left out of the summation, i.e. g_0 in (2-5) and g_{10} in (2-7), define the equivalent nonlinearity respectively for high and low frequency dithering. The describing function concept defines a quasi-linear gain for different cases of static (time invariant and memory-less) nonlinear blocks, but this representation will depend on the stochastic behavior of the input signal. On the other hand there are approaches that do not depend on the deterministic mathematical description of the signal that drives the equivalent nonlinearity; these approaches are based on a so called probabilistic view.

Probabilistic view aims to find the equivalent nonlinearity based on the statistical description of the dithering signal, without imposing any limitation on the mathematical expression of the input signal. The set of conditions imposed on the dithering signal and the message signal does not include anymore the periodicity of the dither signal. This periodicity is replaced with a more relaxed condition of repetitive function [34]. The concept of equivalent nonlinearity is

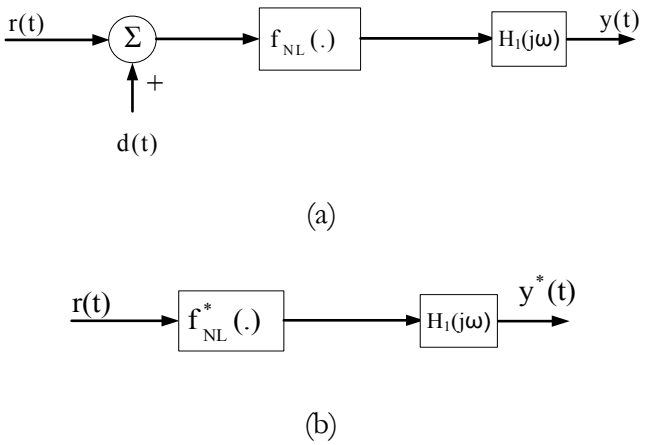


Fig. 2-7(a) Open loop dither applied to static nonlinearity; (b) equivalent nonlinearity

illustrated in Fig.2-7-(a, b).

The two systems generate the same outputs as certain conditions on frequency of the dither and filter dynamics are met, and the modified f^* function is convolution of the probability distribution of the dithering signal with the original nonlinear function as follows:

$$f_{NL}^*(r_g) = \int_{-\infty}^{\infty} f_{NL}(r_g + \xi) P_d(\xi) d\,\xi \tag{2-13}$$

in which P_d represents the value distribution function of the dither signal and ξ is the instantaneous value of the dither signal. It can be achieved by taking the derivative of the cumulative distribution function of the dither signal, noted with capital letter P, defined as follows:

$$P_d(\xi) = \frac{\mu(t \in \{t_1, t_2\}, d(t) < \xi)}{t_2 - t_1} \tag{2-14}$$

in which μ is the measure function [67], or the duration in which the function is less than a certain value ξ, in the observation interval t_1, t_2. P_d is a monotonic increasing function of its argument. It is equal to 1 for infinite argument and 0 for minus infinite argument. The value probability distribution is:

$$p_d(\xi) = \frac{d(P_d(\xi))}{d\xi} \tag{2-15}$$

The condition in which the two functions (f^* and f) generate the same output depends on the frequency content of the input and the dithering signals, and the transfer function of the successive filter ($H_1(j\omega)$). Two different cases have to be distinguished for high and low frequency dithering.

From now on the dither signal should be repetitive. Assuming ΔT_d is the period of the dither signal, or the supermum[3] of the repetition time of the $p_d(t)$, the two cases are established below.

2.6.1 Equivalent nonlinearity for high frequency dithering

If the high frequency attenuation criterion:

$$\lim_{\omega \to \infty} \left(\omega H_1(j\omega)\right) = 0$$

[3] In mathematics, given a subset S of a totally or partially ordered set T, the supremum (sup) of S, if it exists, is the least element of T that is greater than or equal to every element of S. Consequently, the supremum is also referred to as the least upper bound (lub or LUB). If the supremum exists, it is unique.

is met, the outputs of the two systems in Fig. 2-6 are identical, if the dither period tends to zero [34, 65]:

$$\lim_{\Delta T_d \to 0} (y^*(.) - y(.)) = 0$$

while modified f* function is the convolution of the probability distribution of the dithering signal with the original nonlinear function as follows:

$$y^*(.) = f_{NL}^*(r_g) = \int_{-\infty}^{\infty} f_{NL}(r_g + \xi) P_d(\xi) d\,\xi \tag{2-16}$$

A detailed mathematical proof of this theorem is given in [34].

2.6.2 Equivalent nonlinearity for low frequency dithering

Assuming ω_r is the central (carrier) frequency of the band pass signal, and $\omega_r/2 < \omega_d < \omega_r - \Delta\omega$, where $\Delta\omega$ is the bandwidth of the band pass input signal, if the low frequency attenuation criteria are met, as stated below:

$$\lim_{|\omega - \omega_d| \to 0} \big((\omega - \omega_r).H_1(j\omega)\big) = 0$$

Then the outputs of the two systems are identical, if the ratio of the dither period to the signal period tends to zero:

$$\lim_{\Delta T_d/\Delta T_0 \to 0} \big(y^*(.) - y(.)\big) = 0$$

where $\Delta T_0 = 2\pi/\Delta\omega$. The equivalent nonlinearity as a function of the real envelope of the modulated signal can be formulated as:

$$f_{NL}^*(r_g) \triangleq \int_0^{2\pi} \int_{-\infty}^{\infty} \left(\frac{1}{\pi}\right) p_d(\xi_2).f_{NL}(r_g cos\xi_1 + \xi_2) cos\xi_1.d\xi_2.d\xi_1 \tag{2-17}$$

while $p_d(.)$ is the probability distribution function of the value of the dithering signal $d(t)$, ξ_1 represents the phase of the input sinusoid and ξ_2 represents the dither.

This theorem is similar to the correlation equation presented in [34] for low pass signals, but it formulates the envelope transfer function for low frequency dithering. It shows the smoothed shape of the nonlinearity for any kind of periodic dithering signal, under the following conditions:

1. The frequency of the dithering signal is high enough compared to the complex envelope bandwidth.
2. It is high enough compared to the filter bandwidth.
3. It is low enough compared to the carrier frequency.
4. Spurious cross modulation components of dithering and signal are negligible.

Then the two systems of Fig. 2-7-a,b become equivalent.

It is easy to apply equations 2-16 and 2-17, to various nonlinear functions and see the result of application of different dithering signals on equivalent nonlinearity.

2.7 Conclusion

In this chapter, the basic concept of the dithering was introduced. A distinction was made between low and high frequency dithering schemes, and the usable linearization bandwidth was derived for each case separately. The concept of equivalent nonlinearity was introduced which simplifies the analysis of the dither phenomena. The frequency domain Fourier approach and statistical approaches were introduced, which are capable of giving the equivalent nonlinearity for periodic and random signals. The equivalent nonlinearity was derived through Fourier expansion and also related to the statistical properties of the dithering signal and shape of the original memory-less nonlinearity.

Chapter 3

Describing functions

The main motivation for describing function (DF) techniques is the need to understand the behavior of nonlinear system. The DF definition is based on the simple fact that many systems are nonlinear except in limited operation regimes. Nonlinear effects can be beneficial (many desirable behaviors can only be achieved by a nonlinear system, e.g., the generation of useful periodic signals or oscillations), or they can be detrimental (e.g., chaotic behavior). The mathematics required to understand nonlinear behavior is considerably more complicated than that needed for the linear case.

There is one additional theme underlying all the developments: describing function approaches allow one to solve a wide variety of problems in nonlinear system analysis and design via the use of direct and simple extensions of linear systems analysis tools. In fact, the mathematical basis is generally different (not based on linear systems theory); however, the application often results in conditions of the same form which are easily solved.

Finally, we note that the types of nonlinearity that can be studied via the DF approach are very general – nonlinearities that are discontinuous and even multi-valued (like hysteresis) can be considered and the order of the system is also not a serious limitation. The DF approach has its own limitations on the other hand, as mentioned in [4], and among them are uniqueness of the response, uncertainty about the single kind input (i.e. one has to *assume* what kind of input is present) and accuracy in the determination of the response.

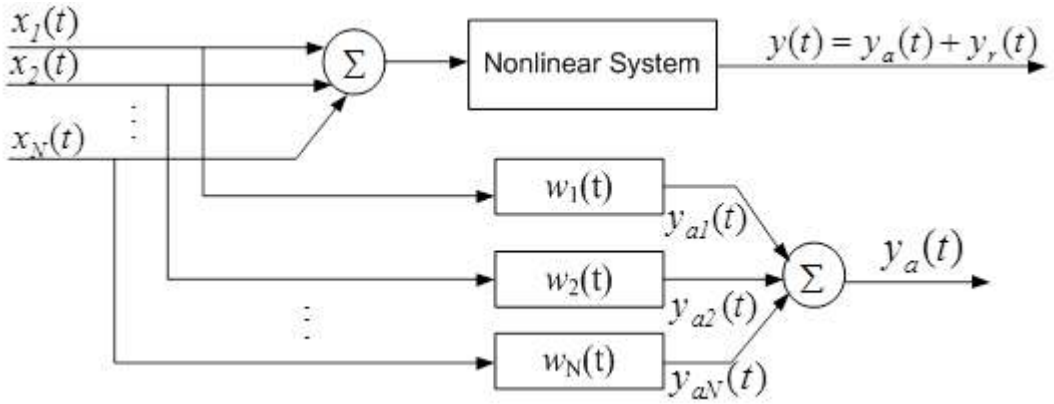


Fig. 3-1 The optimum linear approximator theory for a combination of input signal classes $x_i(t)$, versus the real system.

The small-signal linearization can only explain the effects of small variations about the linearization point, and, perhaps more importantly, it can only reveal linear system behavior. This approach is thus ill-suited for understanding phenomena such as nonlinear oscillation or for studying the limiting nonlinearity effects.

The basic idea of the describing function (DF) approach for modeling and studying nonlinear system behavior is to replace each nonlinear element with a *quasi-linear* describing function, whose gain is a function of input amplitude. The functional form of such an operator is governed by several factors: the type of input signal, which is assumed in advance, and the approximation criterion, e.g., the minimization of the mean squared error.

This technique is dealt with very thoroughly in a number of texts for the case of nonlinear systems with a single nonlinearity ([4], [59]); for systems with multiple nonlinearities in arbitrary configurations, the most general extensions maybe attributed independently to [61] and

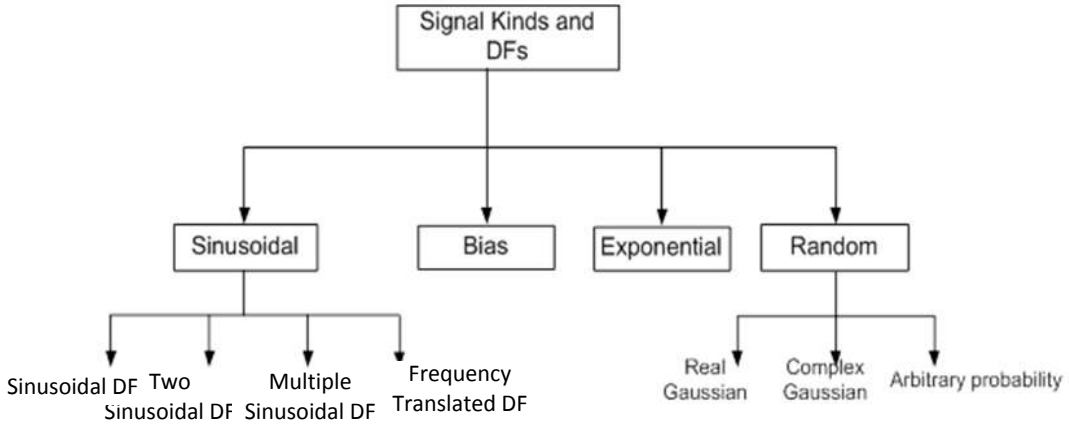


Fig. 3-2 Common signal types and their associated describing functions

[66] in the case of random-input DFs (RIDFs) and jointly to [62] for sinusoidal-input DFs.

The process of rms error minimization is illustrated in Fig. 3-1, where different types of input signal denoted as $x_1(t)$ to $x_N(t)$ are combined to enter the nonlinear block as $x(t)$. The approximated sum of linear weighted inputs forms the approximated output $y_a(t)$, and the goal is to find the best combination of $w_i(.)$ elements to make the best output $w_i(.)$ operators denote the impulse response of the block number 'i' in the parallel filter bank. If the branch number 'i' is static, then its impulse response will be its static gain. In other words the problem is transformed to optimum design of a bank of parallel operators, while

And assuming orthogonality between input components, it is proven in [93] that the following equality must hold for all 'i' and all τ_1:

$$\overline{y_a(t)x_i(t-\tau_1)} = \int_0^\infty w_{oi}(\tau_2)R_{ii}(\tau_1-\tau_2)d\tau_2 = \overline{y(t).x_i(t-\tau_1)} \tag{3-1}$$

while the over-bar denotes the time domain averaging and R_{ii} is the auto-correlation function of branch number 'i', and w_{oi} is the optimum impulse response of branch number 'i'.

$$R_{ii}(\tau)=\lim_{T\to\infty}\frac{1}{T}\int_0^T x_i(t)\,x_i(t-\tau)dt$$

In simple terms, equation 1 shows that: "The cross-correlation of the output of the approximating system and the input signals (left), has to be equal to the cross correlation of the output of the original nonlinear system and the input. The approximated output is also called

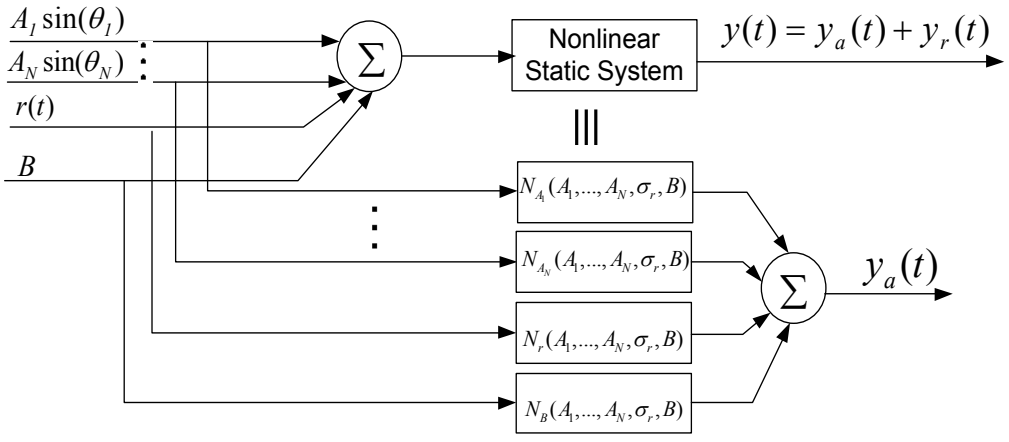


Fig. 3-3: The assignment of DFs as the gains for common classes of the input signal, namely multi-sine, random and dc bias (B) input.

the correlated output. Based on Fig.3-1, the approximated output is:

$$y_a = \sum_{i=1}^{N} w_i(t) * x_i(t)$$

And the auto correlation of the output of the original system is:

$$R_{yy} = \sum_{i=1}^{N} R_{y_{ai}y_{ai}} + R_{y_r y_r} = R_{y_a y_a} + R_{y_r y_r}$$

In the other words, the output of the original nonlinearity is equal to sum of a 'fully correlated' output , which is obtained by DF approximation and 'fully uncorrelated' output. DF approximator can be found for any kind of nonlinearity and any subset of the input signals which are uncorrelated.

In this chapter, the DF concept is singled out for three types of input signal type i.e. single Sinusoidal (and its combinations), random Gaussian signals, Bias or DC and exponential signal. This differentiation and nomenclature is illustrated in Fig. 3-2. Fig. 3-3 illustrates the DF concept for a static nonlinear apparatus, subject to common input signal types, in which w_i elements won't be a function of time and are the same as N elements, where the subscripts A_1 to A_N, r and B denote the input signal type for each particular Gain N.

3.1 Sinusoidal DF

In the following sections, first SIDF is derived and methods of calculation are discussed. Then multiple sinusoidal input signal describing functions is introduced and generically formulated and important formulas are recited based on literature

3.1.1 Single sinusoidal DF

For a sinusoidal input, based on equation, the left hand side of equation (3-1) is ($w_{oi}(t) = w_A(t)$):

$$\int_0^\infty \frac{A^2}{2} w_A(\tau_2)\cos\left(\omega(\tau_1 - \tau_2)\right) =$$
$$\frac{1}{2}A^2\left[\cos(\omega\tau_1)\int_0^\infty w_A(\tau_2)\cos(\omega\tau_2)\,d\tau_2 + \sin(\omega\tau_1)\int_0^\infty w_A(\tau_2)\sin(\omega\tau_2)\,d\tau_2\right] \qquad (3\text{-}2)$$

and the right hand side of 3-2 leads to:

$$\overline{y(t)x_i(t-\tau_1)} = A.\cos(\omega\tau_1)\,\overline{y(0).\cos(\theta)} - A.\sin(\omega\tau_1)\overline{y(0).\sin(\theta)} \quad (3\text{-}3)$$

And the following $w_A(.)$ function satisfies the equality of 3-2 and 3-3:

$$w_A(\tau) = \frac{2}{A}\overline{y(0)\sin(\theta)}\,\delta(\tau) + \frac{2}{A\omega}\overline{y(0)\cos(\theta)}\,\delta'(\tau) \quad (3\text{-}4)$$

The complex frequency domain (Laplace transform) of the transfer function of the *DF* is sum of proportional and derivative paths as follows:

$$N_A \triangleq W_A(s = j\omega) = N_p + jN_q \quad (3\text{-}5)$$

while:

$$N_P = \frac{2}{A}\overline{y(0)sin\theta} \quad (3\text{-}6)$$

$$N_q = \frac{2}{A}\overline{y(0)cos\theta} \quad (3\text{-}7)$$

For any odd single valued nonlinearity, the quadrature gain N_q is zero [4], and the same is true for any combination of a sinusoid and another statistically independent signal. It is proven that the same complex gain minimizes the root mean square error between the real nonlinear block and the quasi-linear approximated *DF*.

There is another more intuitive point of view to approach the concept and that is through Fourier series representation of the output. The DF philosophy is simply to replace the system nonlinearity by a linear gain, chosen in such a fashion that it renders similar responses to the same sinusoidal [4]. In this approach, we observe that if the output of the nonlinearity, defined in the differential equation form $g(x,\dot{x})$ is excited by a pure sinusoidal input like $Asin(\omega t)$, then the output is expressible through the following Fourier series expansion [37]:

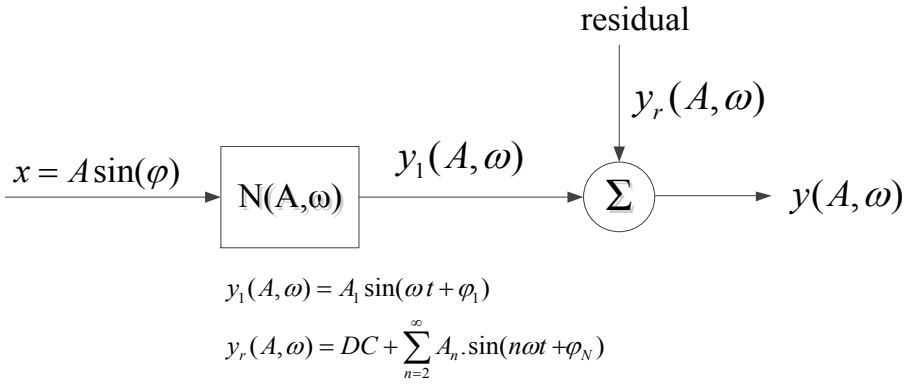


Fig. 3-4 Illustration of the concept of SIDF, residual y_r and correlated part y_1; The total output is sum of correlated and uncorrelated parts

$$y\big(Asin(\varphi), A\omega cos(\varphi)\big) = \sum_{n=0}^{\infty} A_n(A,\omega)\sin\left(n\omega t + \varphi_n(A,\omega)\right), \varphi = \omega t \tag{3-8}$$

and the complex sinusoidal input describing function, denoted $N(A,\omega)$ is defined as:

$$N(A,\omega) = \frac{output\ phasor\ at\ freqeuncy\ \omega}{input\ phasor\ at\ frequency\ \omega} = \frac{A_1(A,\omega)}{A} e^{j\varphi_1(A,\omega)} \tag{3-9}$$

In the other words, a SIDF *is the fundamental complex gain of nonlinearity in presence of a driving sinusoid*. The relationship between the fundamental output, SIDF and the residuals is depicted in Fig.3-4.

It should be noted that despite the apparent quasi-linearization, linear superposition is not valid. Among different kinds of nonlinearities, there are two types that we are especially interested in: relay, ideal and non-ideal and quantizer. The closed form formulas derived for various kinds of DF for these nonlinearities is in [4].

3.1.2 Two sinusoidal input DF

For repetitive but highly non sinusoidal input signals, the SIDF approach renders invalid. One example of this scenario is combination of two input sinusoids. The input is assumed to have the form:

$$x(t) = Asin(\omega_A t + \theta_A) + Bsin(\omega_B t + \theta_B) \tag{3-10}$$

The statistical independence of the two sinusoids at the input must be taken care of. Since each sinusoidal component is characterized by an amplitude and frequency which are deterministically fixed, and by a phase angle, the independence of the input components is established if the phase angles can properly be described as independent random variables. There are a number of important situations in which these phase angles are not independent. If one sinusoid were harmonically related to the other, the periods of the sinusoids would be commensurate, and a consistent phase relation would exist between them. The nature of the nonlinearity output would depend on this relative phase, and the quasi-linear approximator should reflect that dependence. In that case, with two sinusoidal inputs, only one phase angle could be treated as a random variable with a uniform distribution over one cycle; the other phase angle would be deterministically related to the first.

The interpretation of these describing functions as the amplitude and phase relation between each input component and the harmonic component of the same frequency in the nonlinearity output can be employed for describing function calculation:

$$N_A(A,B) = \frac{output\ phasor\ at\ frequency\ \omega_A}{input\ phasor\ at\ frequency\ \omega_A}$$

$$N_B(A,B) = \frac{output\ phasor\ at\ frequency\ \omega_B}{input\ phasor\ at\ frequency\ \omega_B}$$

This phasor gain representation is the direct result of equation (3-1), after simplification of the correlation for two non-commensurable input frequencies. This interpretation is not always valid; for example the cross modulation of two tones might lie on the third one at the output, but it is not correlated with the same frequency at the input of the block. When the origin of the two sinusoids is different, then the probability of the two frequencies being commensurable is zero, because the set of integer and fractional numbers is of zero measure [68] which results in zero probability of random occurrence.

Situations in which the frequencies of the sinusoidal components at the nonlinearity input are *not* related harmonically thus satisfy the assumption of independence which led to the uncoupled expression for the optimum quasi-linear approximator and its specialization to a sinusoidal input component in the presence of any other uncorrelated inputs as follows:

$$N_A(A,B) = \frac{2}{A}(\overline{y(0)sin\theta_A} + j\overline{y(0)cos\theta_A}),\ N_B(A,B) = \frac{2}{B}(\overline{y(0)sin\theta_B} + j\overline{y(0)cos\theta_B}) \quad (3\text{-}11)$$

If we have a static single valued nonlinearity, then the imaginary part of both functions will be zero and averaging can be expressed in terms of the following functional integrals:

$$N_A(A,B) = \frac{1}{2\pi^2 A}\int_0^{2\pi} d\theta_B \int_0^{2\pi} y\big(Asin(\theta_A) + Bsin(\theta_B)\big)d\theta_A \quad (3\text{-}12\text{-a})$$

$$N_B(A,B) = \frac{1}{2\pi^2 B}\int_0^{2\pi} d\theta_A \int_0^{2\pi} y(Asin(\theta_A) + Bsin(\theta_B))d\theta_B \quad (3\text{-}12\text{-b})$$

while the probability of random variables θ_A and θ_B is assumed to be uniform $(\frac{1}{2\pi})$. After Fourier expansion of the output, we achieve:

$$y\big(Asin(\theta_A) + Bsin(\theta_B)\big) = \sum_{m=0}^{\infty}\sum_{\substack{n=-\infty(m\neq 0)\\ n=0(m=0)}}^{\infty}[P_{mn}\sin(m\theta_A + n\theta_B) + Q_{mn}\cos(m\theta_A + n\theta_B)] \quad (3\text{-}13)$$

where P_{mn} and Q_{mn} are to be found through multiplication to the same sinusoid and integration [4]. Having a single valued static nonlinearity, the following properties apply:

$$Q_{mn} = 0\ for\ m + n = odd \quad (3\text{-}14\text{-a})$$

$$P_{mn} = 0\ for\ m + n = even \quad (3\text{-}14\text{-b})$$

and Q_{mn}=0 for odd nonlinearities. For irrational ratio of the frequencies, TSIDF is achieved as:

$$N_A(A,B) = \frac{P_{10}}{A}, N_B(A,B) = \frac{P_{01}}{B} \quad (3\text{-}15)$$

And if the ratio is rational ($\gamma = \frac{\omega_B}{\omega_A}$), we look for the components of y(t) at frequency $\omega_A = m\omega_A + n\gamma\omega_A$, which will be of the form $P_N \sin(\omega t + \theta_N)$ and hence

$$N_A(A,B) = \frac{P_N(A,B,\gamma)}{A} . e^{j\theta_N(A.B,\gamma,\theta)} \quad (3\text{-}16)$$

which means that the DF for each of the sinusoidal *will depend* on the ratio of the frequencies. TSIDF can be related to the concept of equivalent nonlinearity, for two tone input signal, as explained in chapter 2 as:

$$g_{10}(A,B) = A.N_A(A,B)$$

There are many functions in communication blocks that require frequency translation, for example mixers, and frequency multipliers.

3.1.3 Multiple sinusoidal input DF

When there are more than two sinusoids, the integrals will be as follows:

$$N_{A_i}(A_1, A_2, \dots, A_N) = \frac{2}{(2\pi)^N} \int_{\theta_1,\theta_2,\dots,\theta_N=0}^{2\pi} y(\sum_{n=1}^{N} A_n \sin(\theta_n)).\sin(\theta_i) d\theta_1 d\theta_2 \dots d\theta_N \quad (3\text{-}17)$$

However calculation of this integral is very difficult and in many cases doesn't result in a closed form formula. Therefore we need to use additional statistical properties of a multi-sine with a large number of tones, as we will see in section 3.2.

3.1.4 Frequency translated DF

Black box modeling of frequency translating components, including frequency multipliers and mixers, has been subject of many research papers. There are two methods for that: Volterra series and describing functions. The Volterra input output polynomial (VIOP) approach fails to converge to the measured data [54] for hard nonlinearities and is generally a subcategory of describing function approach. It is proven that VIOP does *not* include all of the possible polynomial powers in its formulation. On the other hand artificial neural network methods fail to predict the soft nonlinearities and have a very long convergence time and training period, including numerical complexities.

Considering the Fourier series representation of equation (3-14), assuming we have *TWO non-commensurable input* frequencies, the describing function gain relating the intermodulation order m,n to the input in each frequency is as follows:

$$M_{m,n,A} = \frac{P_{mn}+jQ_{mn}}{A}, M_{m,n,B} = \frac{P_{mn}+jQ_{mn}}{B} \quad (3\text{-}18)$$

For the two frequencies, being non commensurable is a crucial assumption that *must* hold, for the validity of this approach. Similar to the approach introduced in appendix I, a new formulation can also be given based on frequency domain transform of the nonlinear function:

$$M_{m,n,A}(A,B) = \frac{j}{\pi A}\int_{-\infty}^{\infty} Y(ju)J_m(Bu)J_n(Au)du \quad (3\text{-}19)$$

$$M_{m,n,B}(A,B) = \frac{j}{\pi B}\int_{-\infty}^{\infty} Y(ju)J_m(Au)J_n(Bu)du \quad (3\text{-}20)$$

It should be noted that this gain is not a *"Correlated DF"* within the frame work of the introduction, and the classical definition of DF based on fully correlated approximation is not valid. However this approach can be utilized in order to explain the linear behavior of nonlinear components. The major problem is to find a functional form for nonlinear frequency translating block ($y(.)$), which can be a delicate job for practical blocks. In many cases the function y(x) is not an analytic function and this will be discussed in detail in Chapter 9.

3.2 Random input describing function

According to central limit theorem [68], when we have a large number of uncorrelated input tones, the statistical behavior approaches a Gaussian distribution. This property is used to drive Random Input DF.

Gaussian processes have two types: real and complex: real Gaussian processes, like the additive white Gaussian noise, have a Gaussian distribution for their value in time domain. A complex Gaussian process is an orthogonal summation of two real Gaussian processes. A famous example of this type of signal is a time domain multiplexed WCDMA downlink, in which a lot of traffic channels are multiplexed into the same bandwidth, and each channel has a quadrature modulation.

3.2.1 Real Gaussian input DF

Assuming that the input is sum of a bias, a sinusoid and a real Gaussian Process, as follows:

$$x(t) = B + r(t) + Asin(\omega t + \theta)$$

which is the most general input form used in [4], and $r$is a Gaussian random variable with zero mean and variance ${\sigma_r}^2$, and θ is uniformly distributed between 0 and 2π, then the joint distribution of the phase θ and r is $\frac{1}{2\pi}.\frac{1}{\sigma_r\sqrt{2\pi}}e^{-\frac{r^2}{2\sigma^2}}$ and the mathematical expectation is to be taken

with respect to both of these random variables. Similar to equation 6, the following relations hold for sinusoidal and random part describing functions:

$$N_A(A,\sigma_r)=\frac{2}{A}\overline{y(x(0))\text{sin}\,(\theta)} \qquad N_r=\frac{1}{{\sigma_r}^2}\overline{y\big(x(0)\big)r(0)} \tag{3-21-a}$$

And using the joint probability, we obtain the following DF for random part:

$$N_r(A,\sigma_r,B)=\frac{1}{(2\pi)^{3/2}{\sigma_r}^3}\int_0^{2\pi}d\theta\int_{-\infty}^{\infty}y\big(B+r+Asin(\theta)\big)re^{-\frac{r^2}{2\sigma^2}}dr \tag{3-21-b}$$

There are closed form answers to the integral, but in general, numerical integration techniques like trapezoidal must be used to evaluate the random gain.

3.2.2 Complex Gaussian DF

When the input signal is complex Gaussian, i.e. the base band complex envelope has Gaussian real and imaginary parts as r variable above, then the problem would be different. Assuming that the input complex envelope is $\tilde{r}=r_1+jr_2$, while the input signal is modulated in the form:

$$r=real\big(\tilde{r}e^{j\omega t}\big), \qquad \tilde{r}=r_1+jr_2$$

and $\sigma_{r1}=\sigma_{r2}=\frac{\sigma_r}{\sqrt{2}}$, where r_1 and r_2 are in-phase and quadrature parts of the input signal and both are real zero-mean Gaussian variable, then the in-phase and quadrature equivalent nonlinearities can be achieved through two dimensional Fourier expansion as follows:

$$g_{0I}(r_1,r_2,A)=\frac{1}{2\pi^2}\iint_0^{2\pi}y(r_1\cos(\theta_1)+r_2\sin(\theta_1)+Asin(\theta_2))\cos(\theta_1)\,d\,\theta_1 d\theta_2 \tag{3-22}$$

$$g_{0Q}(r_1,r_2,A)=\frac{1}{2\pi^2}\iint_0^{2\pi}y(r_1\cos(\theta_1)+r_2\sin(\theta_1)+Asin(\theta_2))\sin(\theta_1)\,d\,\theta_1 d\theta_2 \tag{3-23}$$

And for the sinusoidal part the second term of the integrand is $sin(\theta_2)$, and all of the above is written again for static single valued nonlinearity. After statistical averaging on the in-phase and quadrature gains, the following transfer functions are derived for the two parts:

$$N_I(\sigma_r,A)=\frac{1}{\sigma\sqrt{\pi}}\iint_{-\infty}^{\infty}g_{0I}(\frac{\sigma_r}{\sqrt{2}}r_1\,,\frac{\sigma_r}{\sqrt{2}}r_2,A).e^{-\frac{({r_1}^2+{r_2}^2)}{2}}dr_1dr_2 \tag{3-24}$$

$$N_Q(\sigma_r,A)=\frac{1}{\sigma\sqrt{\pi}}\iint_{-\infty}^{\infty}g_{0Q}(\frac{\sigma_r}{\sqrt{2}}r_1\,,\frac{\sigma_r}{\sqrt{2}}r_2,A).e^{-\frac{({r_1}^2+{r_2}^2)}{2}}dr_1dr_2 \tag{3-25}$$

For an odd nonlinearity, $N_I=N_Q$, and for all other situations the gain will be complex [37].

3.3 Conclusions

In this chapter a brief survey of the describing function approach was provided. Describing function is the gain assignment to a general nonlinear block, relating the correlated output to the according input signal. The describing function gain will depend on the type of input signal. The approach was based on the methods formulated in [4], [58] and an extension to that for complex Gaussian process and frequency translating nonlinear phenomena. The formulas and concepts introduced will be used in the following chapters for analysis and simulation.

Chapter 4

Architectures and topologies

Dithering is applicable to any nonlinear system, to enhance linearity. We normally use the dithering to linearize the switched mode power amplifiers, while benefiting from good efficiency. The system architectures can be in many different forms: open or closed loop (with negative feedback), tracking of supply voltage or load impedance, and power combining with common mode dither. The dither can also be applied to different points of the system, depending on its frequency and the system architecture.

Common mode dithering is a power combining technique that enables us to get more power with acceptable linearity, while needing a softer output filter to omit the dither component,

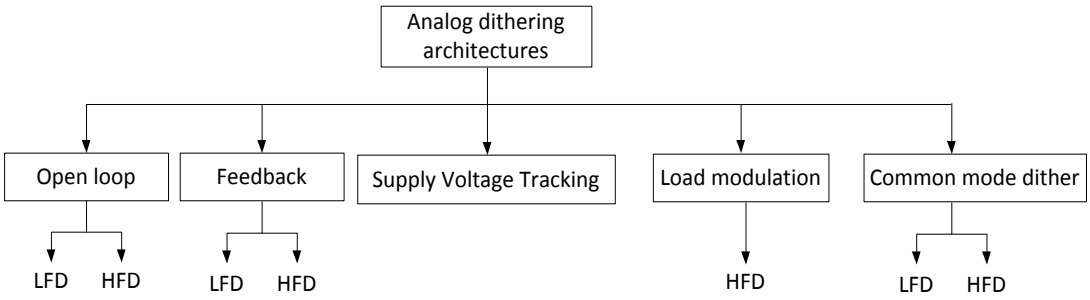


Fig. 4-1: Possible switch mode architectures that can be used with dithering, tracking can be used with LFD, HFD and common mode dithering.

and reconstruct the amplified signal.

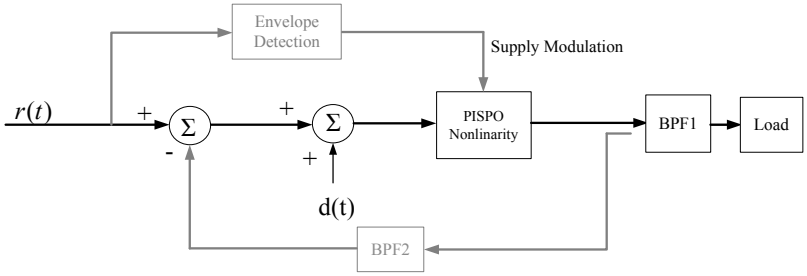
Envelope modulation can also be combined with dithering to improve the linearity-efficiency compromise. Load modulation is applicable to a tunable matching networks, in order to improve the linearity, while supply modulation can enhance the efficiency in the output power back off. Fig. 4-1 is an overview to the different system architectures that we can use in combination with dithering.

In this chapter, first of all, all of the system architectures that conventionally have been used in combination with a dither signal will be introduced. Then the various hard nonlinear components are investigated at circuit level, with special interest to power amplifiers.

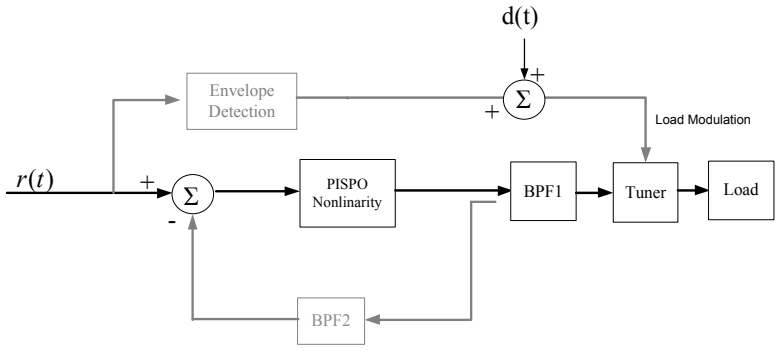
From now on we assume that all the systems we deal with are *Periodic In Same Periodic Out (PISPO)* [77], which means that we are excluding the oscillating and chaotic systems, and therefore the fundamental frequencies at the input and output of the nonlinear block are the same.

4.1 Architecture level considerations

In discrete and continuous time power amplifier systems, open and closed loop architectures



(a)



(b)

Fig.4-2 (a): A generic nonlinearity, with dithering, envelope tracking and negative feedback; (b): load modulation with voltage controlled tuner

are feasible. In power amplifiers, the efficiency can be enhanced by envelope tracking. Envelope tracking is also applicable to the load and supply voltage. Therefore the architectures can be categorized as closed and open loop, and with or without envelope modulation. All the options for a linearized quantizer are depicted in Fig. 4-2. The system may be used as a modulator or a power amplifier, depending on the device characteristics and impedance levels, i.e. if the output is high power they system is a linearized switched mode PA, but if the nonlinear block is a binary quantizer, at low power, it is only a time domain encoder.

4.1.1 Open-loop

This method includes the forward path of Fig. 4-2-a. The linearity issues will be discussed in chapter 5. Proper selection of the dither level and frequency can satisfactorily linearize the forward path.

4.1.2 Closed-loop

Although it is not necessary to have a feedback path, having a feedback enhances linearity, adjusts the loop bandwidth and de-sensitizes the performance for the component variations. For example power supply rejection ratios of the order of 90 dB are achievable in closed loop designs [78]. Proper design of the loop order in closed loop architecture enables us to reduce the distortion. The downside is that unwanted limit cycles and chaotic behavior may arise due to feedback. Implementation of the feedback can be hard at high frequencies.

Obviously, a closed loop structure always uses a negative feedback. A special case of a closed loop system is autonomous dithering, in which the dithering is a limit cycle oscillation, chosen to be higher than the input frequency. When the closed loop system has a limit cycle, it is called a self-oscillating power amplifier, and the role of the oscillation is the same as dithering. For frequencies other than the input frequency, the feedback is always negative.

4.1.3 Tracking

All switched mode power amplifiers, implemented as PISPO in Fig. 4-2, are active components, or transistor circuits, with input output characteristics like a relay. The supply voltage determines the quantizer step voltage. Furthermore the power loss of the power amplifier will depend on this supply voltage (as the total loss is the value of the dc supply voltage times the dc current drawn from that). Therefore it makes sense to modulate the supply voltage to keep the ratio between the output power and the PA power loss (normally identified as output efficiency) constant. A more detailed analysis and measurement results on a real prototype class-D PA will be given in chapters 5 and 7.

4.1.3.1 Tracking with open loop

It is proven in appendix V.I that when we modulate the supply voltage of a PA with the amplitude (real envelope) of the input signal, we need to modulate the gain correspondingly, to keep it linear. Therefore, with and without feedback and with envelope modulation, we have to modulate the amplitude of the dither signal:

$$d(t) = D_0(1 + \alpha|\tilde{r}(t)|) \quad (4\text{-}1)$$

Any time difference between the supply modulation and dither modulation will cause additional distortion.

4.1.3.2 Tracking with closed loop

Similar condition holds for linear performance of the closed loop. A method to omit dither modulation is used in a self-oscillating class-D PA (chapter 7). In that case, the dither level, which is the sinusoidal oscillation that is automatically generated in the loop, will keep the loop linear.

4.1.4 Common mode dither

The output band-pass filter has to be able to omit the out of signal band spurious components that were described in chapter 2. For dither frequencies close to the signal frequency, it is hard to implement a sharp filter with moderate insertion loss. Another approach is to apply a common mode dither to two identical nonlinear blocks. The output dither components are then in phase (common mode), and therefore a relaxed output filter order will be required. Fig.4-3 can be extended to more than two SMPAs. Besides rejecting the common mode dither, this topology acts as a power combiner, like a balanced amplifier. This technique is shown in block diagram of Fig.4-3, and will be discussed for a particular circuit topology in 4.2.2.

4.1.5 Possible dithering locations

Dithering can be applied to the architecture in two different positions. One is the input to the amplifier as in Fig.4-2-a and another one is to the control input of the adaptive load tuner, as in Fig. 4-2-b. In the first position, high and low frequency dithering are both possible, while in the latter, only high frequency dithering can be used, to linearize the system.

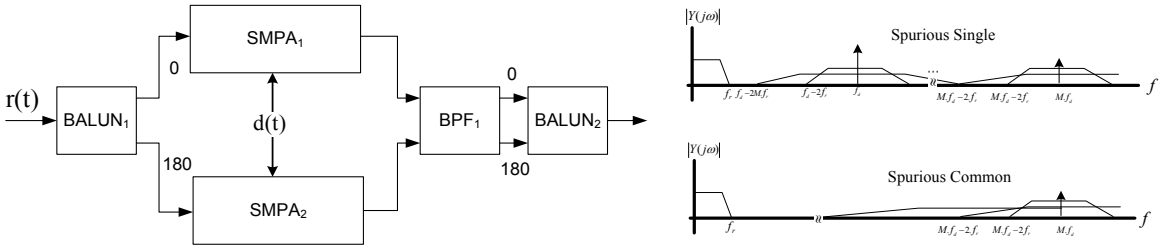
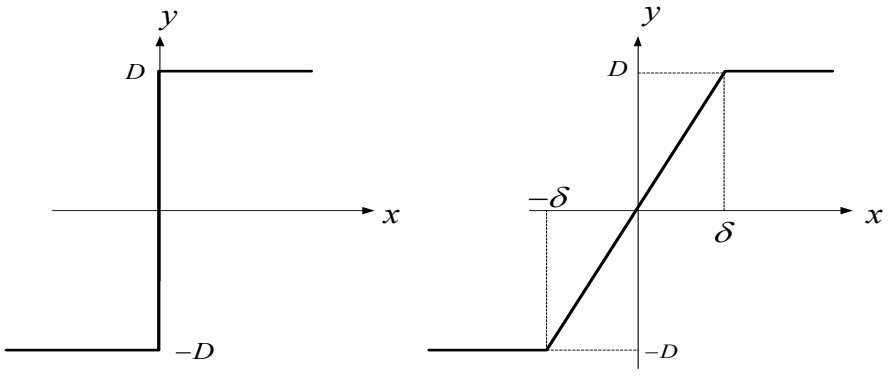


Fig. 4-3: Common mode dithering scheme, with two identical switch mode power amplifiers ($SMPA_{1,2}$) the fundamental output dither will be common mode, resulting in a relaxed filter order requirement.



(a) (b)

Fig. 4-4: Input output characteristic of (a): ideal relay; (b): limited slope limiter

4.1.6 Slope gain considerations

In power amplifier applications, dithering works fine as long as the saturation of the nonlinear apparatus happens '*fast enough*', relative to the input variations. The reason for that is that apart from linearization, dithering reduces the describing function gain, inversely proportional to the dither level.

Fig. 4-4 (a) is the ideal relay function. For the limited slope gain saturation, as shown in Fig. 4-4-b, the describing function gain is calculated in appendix I as:

$$N_B(A,B) = \frac{2D}{\pi\delta B}\int_{-\infty}^{\infty}\frac{\sin(\delta u)}{u^2}J_0(Au)J_1(Bu)du \qquad (4\text{-}2)$$

In which $\frac{D}{\delta}$ is the slope gain of the switched mode power amplifier (SMPA). Equation 2 states that the lower $\frac{D}{\delta}$ (slope gain), the lower the gain of the describing function; moreover the gain depends very much on the original slope gain. The integral of (4-2) is not a sensitive function of δ.

A higher DF gain which is equivalent to a higher voltage or power gain, in switched mode power amplifiers, lowers the power added efficiency. This is true for all operation classes of power amplifiers. Further basic trade-offs will be discussed at the end of this chapter in 4.3.

4.2 Circuit topologies

From the various switched mode topologies, two important switched mode amplifiers, are discussed in this thesis, generating either square wave output voltage or square wave output

current. Any other topology that has a satisfactory fast saturation, works fine with the dithering.

Class-D RF power amplifiers have been in use for a long time. The theoretical efficiency of a Class-D amplifier is 100%, but in practice it is lower due to reactive power loss, which will be discussed in detail in section 4.2.2.

4.2.1 Voltage mode and current mode class-D

As stated before, Class-D amplifiers are made in two ways: voltage mode (VMCD) and current mode (CMCD). The voltage mode is illustrated in Fig. 4-5-a, where the output node is switched alternatively between the supply voltage and ground, and Fig. 4-5-b shows its dual circuit, which steers a dc current between the two switch elements. As can be seen in Fig. 4-5-c and 4-5-d, in VMCD the voltage waveform is a square wave (pulse) and alternatively in its dual circuit, the current is a pulse. The current is a half wave rectified sine wave in VMCD, like the single output voltage in the CMCD. The sketched voltage and current waveforms are for ideal operation; however, in practice the parasitics make the wave-forms deviate from this ideal

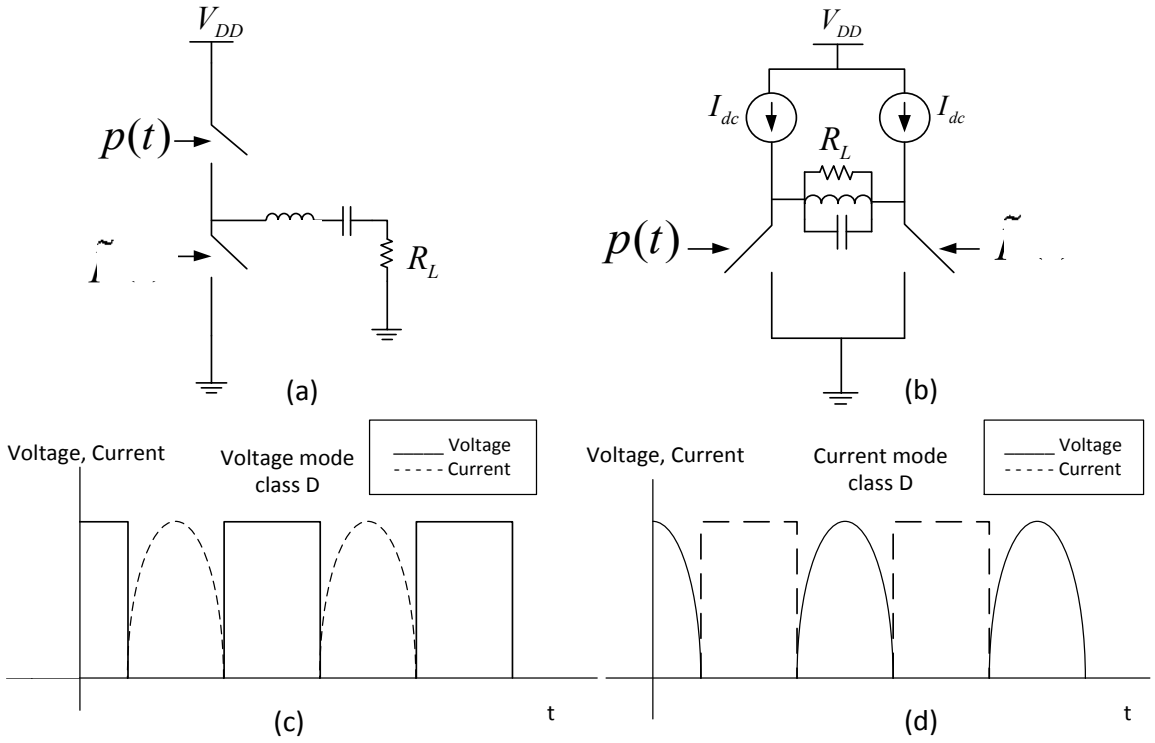


Fig. 4-5 (a,b): Voltage and current mode Class-D amplifier; (c,d): voltage and current wave forms of voltage mode and current class D amplifiers

shape.

The LC filters in the circuits of Fig. 4-5-a must provide the optimum load impedance at the fundamental frequency. In VMCD the higher order harmonics of the output square wave should terminate to open circuit, while in its dual amplifier or CMCD of Fig. 4-5-b, the higher order harmonics of the output current square wave must have short circuit termination to maximize the power efficiency.

The loss mechanisms can again be represented as dual of each other, when we consider the reactive loss. Moreover there may be moments in which both of the switches are one in VMCD, or open in CMCD, which makes the CDA to draw a high current from the supply voltage or makes big spike voltages on the output. Therefore the *proper timing of the command voltages in both CMCD and VMCD is very critical, especially at high frequencies.*

For practical circuit topologies of VMCD and CMCD important design parameters are derived versus the circuit elements, in order to model the efficiency and power. The following sub-chapters will first discuss the current model for capacitors, and a new parasitic model is proposed as in [71] which has the advantage of accurate gain prediction with quasi-linear capacitors in the model. Linear elements are approximated and finally the model is validated through simulations on CMOS CDA. The agreement between the results and foundry BSIM model validate the quasi-linear performance of the model as a two frequency gain block.

4.2.2 Design aspects of voltage mode class-D

Fig. 4-6 illustrates the most common schematic diagrams of a voltage mode class-D amplifier with FETs. The first row shows the complementary and identical transistors implementation of a single stage VMCD and the second row shows two conventional driver arrangements. Each stage might be complementary or with transformer, and different biasing for positive and negative parts of switching. Assuming the input voltage is a pulsed voltage, depending on the input level, at each moment, only one transistor will act as a switch and the other one will be open, so the output will be a pulse waveform, switching between the positive rail and ground.

Early papers on Class-D amplifiers neglected the effect of switching losses. In this section, the losses in an RF switching power amplifier and their frequency dependence will be described. The losses analyzed are the switching, conduction, and gate drive losses. The latter ones are usually ignored in lower frequency applications, but must be accounted for at the frequencies of interest in this paper (> 10 MHz).

Expressions will be derived to predict the efficiency of a Class-D power amplifier. In recent years, Class-D circuits operating with zero-voltage switching using the dead time have been introduced [39]. Zero voltage switching is theoretically impossible when we have a dithered system and the signal is not periodic [46]. At RF the dead time is very short, therefore we need to be careful with the driver design. There are also issues related to the control of that dead-time with a reasonable accuracy when the dead-time is in nanoseconds. Using a square wave gate drive to do the timing quickly becomes very difficult for gigahertz range switching frequencies. A method whereby the amplitude of the sinusoidal gate voltage controls the dead

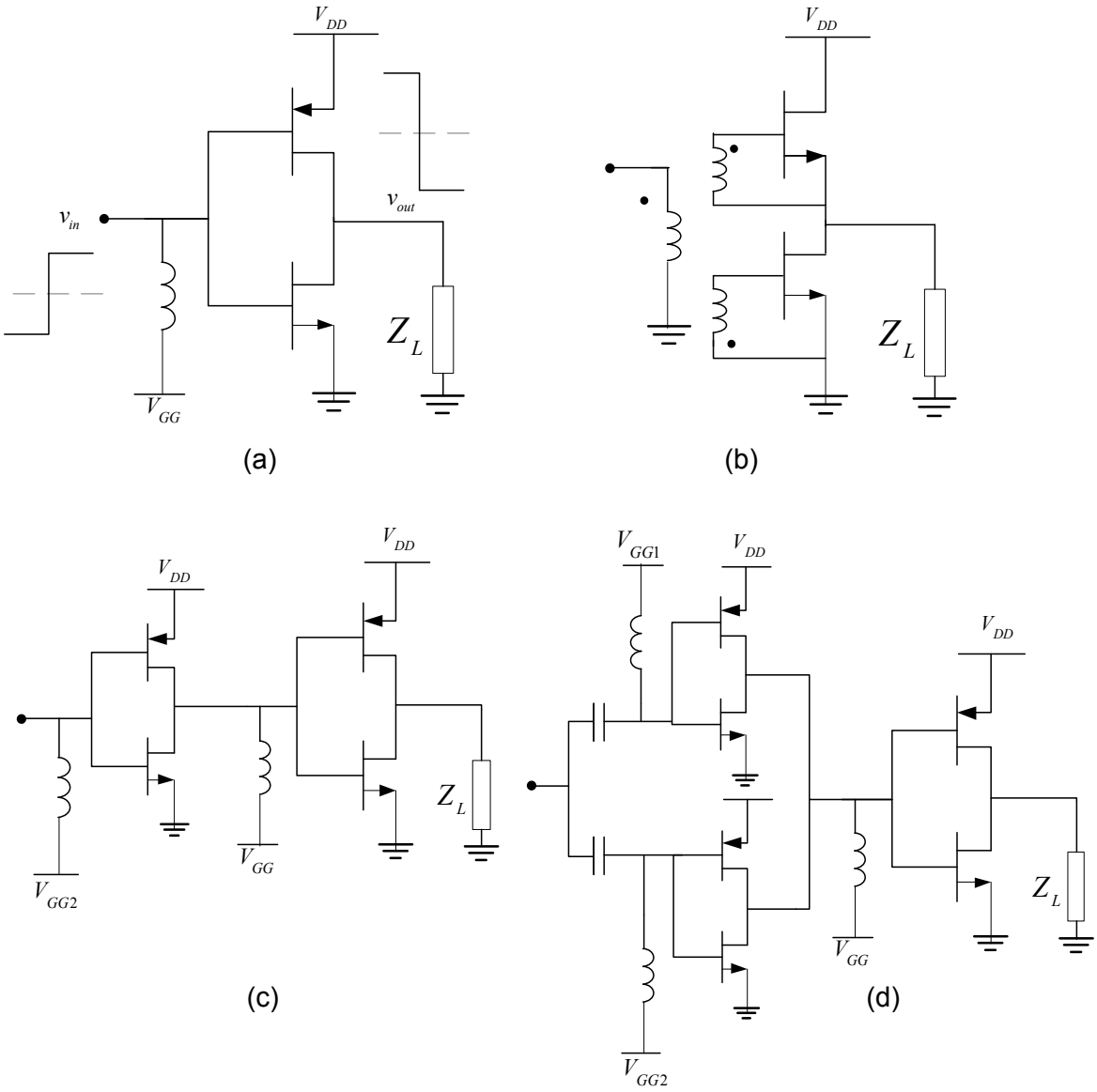


Fig. 4-6 (a): Complementary single stage VMCD; (b): identical pair with transformer; (c): two stage complementary with driver; (d): break before make driver

time is described in [48]. The design equations for the proper selection of the device width based on a given output power and crest factor in a switching Class-D will be derived in this section.

Output power

Traditional design procedure for class-D was developed by [48] for the case of single carrier applications. However, the optimum theoretical points for the load impedance to yield the maximum power efficiency are different for multi carrier (or sigma delta) and continuous wave (CW) [18].

For the CW case, the output pulse train will have a 50% duty cycle, assuming we have an ideal switch, and the output pulse amplitude is equal to the dc voltage of the supply, the output pulse can be described as:

$$v_{out}(t) = V_{DD}(\frac{1}{2} + \frac{2}{\pi}\sin(\omega t) + \frac{3}{2\pi}\sin(3\omega t) + \cdots) \quad (4\text{-}4)$$

Assuming there is a series loss-less resonator, isolating the load R_L from the device output, the fundamental harmonic delivered power to the load will be:

$$P_{out} = \frac{2}{\pi^2}.\frac{{V_{DD}}^2}{R_L} \quad (4\text{-}5)$$

Hence assuming an ideal switch ($R_{dson} = 0$), the required load is easily determined by the required power, as long as the device ratings are met, i.e. the maximum allowed current is not exceeded.

When the output pulse is with relative duty cycle value α, the pulse train has a Fourier series expansion with a fundamental frequency component amplitude of $2V_{DD}\sin(\pi\alpha)/\pi$. The switched pulse train delivers an average load power of:

$$P_{out} = \frac{2{V_{DD}}^2}{\pi^2 R_L} sin^2(\pi\alpha) \quad (4\text{-}6)$$

Coding efficiency

The coding efficiency, defined as the ratio of the intended (fundamental) harmonic output power to the entire pulse train power is:

$$\eta_p = \frac{8}{\pi^2} sin^2(\pi\alpha) \quad (4\text{-}7)$$

For example the coding efficiency of 50% duty cycle pulse train is 81%. This is the usual wave to understand the depth of modulation of RF power on the output pulse train, like the amplitude modulation index [18].

Peak current and device width

When we have a generic signal which duty cycle modulates the output pulse train, based on the definition of peak to average power ratio, the peak device current is given as:

$$I_{L,peak} = \frac{P_{out}}{V_{DD}} \sqrt{\frac{8.PAR}{\eta_p}} \tag{4-8}$$

and if the current capacity of the technology node is $I_{max}(\frac{A}{mm^2})$, the according width of the base-gate should be:

$$W_{sw} = \frac{I_{L,peak}}{I_{max}} \tag{4-9}$$

Optimum power load

Assuming that the total available power is the sum of the power dissipated in the transistor and the load power, based on solution of a second order equation, the following relationship will be achieved for practical optimum power load, versus the switch on-state resistance R_{dson} :

$$R'_L = \frac{R_L}{2}\left(1 + \sqrt{1 - \frac{4R_{dson}}{R_L}}\right) - R_{dson} \sim R_L - 2R_{dson} \tag{4-10}$$

where R_L is obtainable from equations (4-4) or (4-6). There are other considerations regarding optimum design of the output filter for zero voltage switching, i.e. switching at the moments where there is no charge or voltage on the drain-source capacitors, but those considerations are not valid for dithered circuits [70], The reason is that we cannot provide the same transient condition for a random leading and trailing edge of the output pulse. Therefore this issue is not applicable to the dithered switched mode amplifiers.

Loss mechanisms and drain efficiency

There are to different approaches to calculate the power loss regarding to a VMCD. The first one is to divide the power loss to different kinds of loss, according to their corresponding mechanism and the second one is trying to find the solution to the circuit model, without differentiation between these loss types.

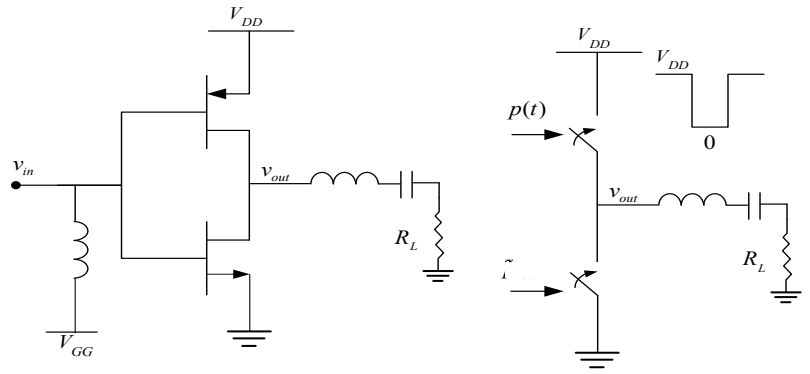


Fig. 4-7: VMCD and output series LC resonator

In the first approach, the main loss mechanism is conductive loss. This is loss due to the load current that will pass through each transistor. Part of the available power is wasted due to non-zero R_{dson}. This loss can be avoided through making a dead-time during the switching phase and break before make techniques. The second kind is capacitive loss, as each transistor charges and discharges a set of capacitances within the devices. The last kind is the loss related to simultaneous conduction of both FET devices. The loss due to charge storage and discharge in the input node is considered as driver loss and does not contribute to the major power loss of the PA.

The conductive loss is $P_c = R_{ds,on}{I_L}^2$, as long as it can be assumed that the switch can be modeled like a linear resistor.

The capacitive loss or $P_{cap} = CV^2f$ loss is difficult to formulate, because the capacitors are naturally nonlinear. A detailed analysis for HEMT class-D amplifiers is given in [18], which approximates the capacitors as linear elements. The same approach can be taken for all of FET devices and is investigated in [18] for a general band-pass sigma delta modulator, driving a voltage mode class-D amplifier. Assuming we can formulate the capacitive loss based on the frequency for a random signal [46], then the drain efficiency is:

$$DE = \frac{P_{out}}{P_{dc}} = \frac{P_{out}}{P_{cap} + P_c}$$

And at low frequencies, it can be simplified to $\frac{R_L}{R_L + R_{ds,on}}$ which means that the higher the load resistance, the higher the efficnecy would be. The required power determines then the efficiency.

The second circuit based approach is based on the assumption that the switches are modeled as voltage controlled resistors, that the sum of their resistances are constant and that each resistance changes softly between $1/g_{c0}$ and zero. It is proven in [70] that the total loss based on this second approach is as follows:

$$P_{dc} = \frac{g_{c0}D^2}{2}\left[1 - \sum_{m,n=1}^{\infty} G_{mn}(A,\sigma)Real\left(\frac{g_0}{g_0+Y_L(m\omega_r+n\omega_{LC})}\right)\right] \quad (4\text{-}11)$$

where g_{c0} is the switch conductance, Y_L is the load admittance, m, n are cross modulation indexes and G_{mn} are gains of cross modulated components of ω_r and ω_{LC} versus input. The power efficiency is achieved accordingly as the ratio of the output power to the total dc power loss.

Intrinsic parasitic capacitance effects

The intrinsic capacitive parasitics are very important, because, apart from capacitive loss, they affect the dynamic transfer function and the describing function behavior of the device. They can contribute to the memory effect discussed in chapter 6.

In a real scenario, when we need to get enough power from a CDA with a low supply voltage; we have to scale up the channel width to decrease the ON resistance of the device to make the available power higher. This introduces linear and nonlinear capacitive parasitics to the topology and its behavior won't be that of a static inverter switch any more. Especially in high frequency applications, other effects show up as frequency and amplitude dependent phase difference between the output and input of the amplifier.

These parasitics have two major effects. First they change the input impedance of the CDA that changes the input RF component to the device which in turn changes the output power. Second, because of this additional phase shift introduced, the frequency of limit cycle oscillation won't be the same as the one calculated with the static model, for self-oscillating loop, like the one approximated in [1]. From an analysis point of view, there are many convergence

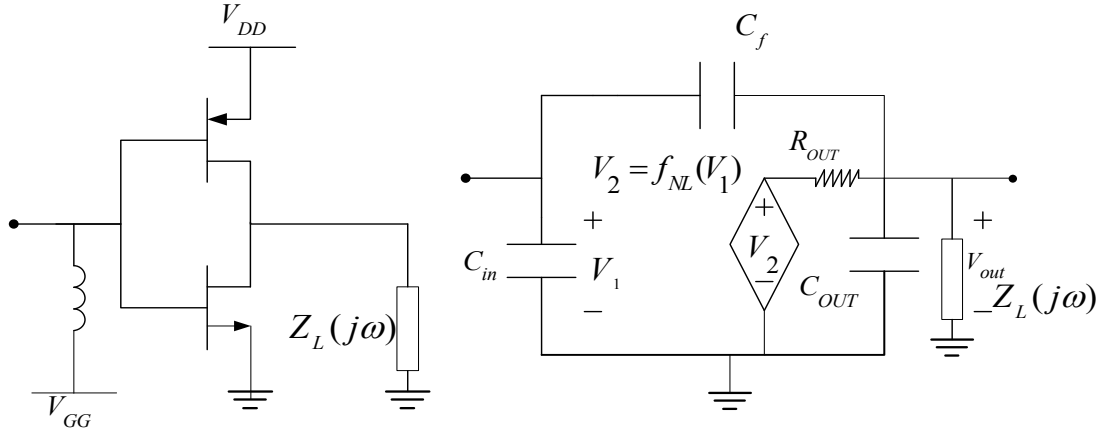


Fig. 4-8: (a) Typical Voltage Mode Class D amplifier; (b) proposed model

problems with current models for high frequency PWM applications.

Proposed nonlinear model including parasitic capacitors

Figure (4-8-a) shows the schematic diagram of a voltage mode class-D amplifier and Fig. (4-8-b) shows the proposed nonlinear behavioural model. Parameters C_f, C_{in} and C_{out} are constant linear capacitors. Rout is the output low frequency linear resistance of the device and f_{NL} is the nonlinear operator representing static transfer function of the CDA, which can be described by a linearized describing function for two different input signal types at the same time.

The static relation predicts the static and low frequency part of the input-output voltage relationship. The feedback capacitor provides an amplitude dependent hysteresis (output phase minus input phase).

The latter can affect the limit cycle frequency for different input amplitudes, within the self-oscillating loop. The proposed model is equivalent to the real device parameters in complex voltage gain and input impedance.

Parameter extraction and validation

Parameter extraction is done in two steps. The first step is extraction of $f_{NL}(.)$ and R_{out} from low frequency voltage-voltage transfer function that is fitted with a hyperbolic form $f_{NL}(x) = a.tanh(b.(x-c)) + d)$, where a resembles the supply voltage, b the slope gain at the origin, c shows the evenness of the transfer function and d is the offset due to single supply voltage. The second step is to measure the quasi-periodic gain, i.e. exciting the amplifier with two different carrier frequencies at RF and limit cycle frequency, with a source of impedance Z_S, and sweep the amplitudes within the range of the operation and measure the gain for each carrier in every sweep point. From Fig (4-8-b), the gain relations that have to be fit are written in equations (4-12).

$$G_v(A,B,\omega) = \frac{V_{out}}{V_s} = \frac{\frac{N(V_1)}{R_{out}} + Y_F}{\left[\frac{1}{R_{out}} + Y_F + Y_L\right][Z_S(Y_F + Y_{in}) + 1] - Y_F Z_S(\frac{N(V_1)}{R_{out}} + Y_F)} \quad (4\text{-}12)$$

where $N(A,B)$ is one of the two components of the vector of the static two-input linear describing functions and V_1 is the two sinusoidal input voltage vector . Equation (4-12) turns into miller capacitive effect when R_{out} is infinite (i.e.$Y_{in} = C_{in} + C_f(1-N)$).

Table 4-I: The extracted parameters

a	b	c	$c_{in}\ (pF)$	$c_f\ (pF)$	$R_{out}(\Omega)$
-0.4959	11.3	-0.0938	5.04867	5.880	0.21

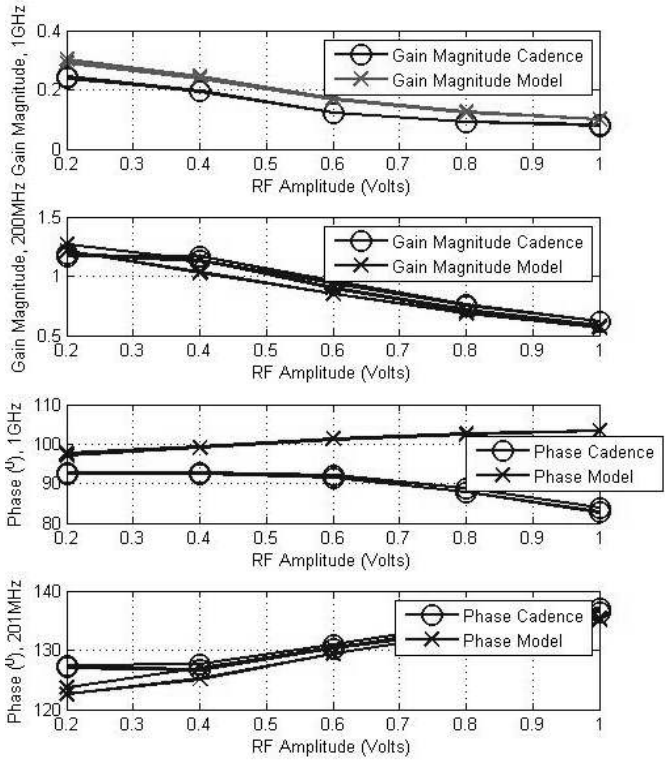


Fig. 4-9: Magnitude and phase of voltage gain for 200MHz (signal) and 1GHz (dither) frequency.

The function f_{NL} and R_{out} are extracted from the low frequency input-output voltage characteristics of the CDA (for resistive output termination) and afterwards the parameter extraction is minimization of the following error functions (EF):

$$EF_{RF} = \sqrt{\sum_{i,j}\left(\left|G_{mRF}(A_i,B_j)\right| - \left|G_{RF}(A_i,B_j)\right|\right)^2 + \left(\angle G_{mRF}(A_i,B_j) - \angle G_{RF}(A_i,B_j)\right)^2} \qquad (4\text{-}13\text{-a})$$

$$EF_{SW} = \sqrt{\sum_{i,j}\left(\left|G_{mSW}(A_i,B_j)\right| - \left|G_{SW}(A_i,B_j)\right|\right)^2 + \left(\angle G_{mSW}(A_i,B_j) - \angle G_{SW}(A_i,B_j)\right)^2} \qquad (4\text{-}13\text{-b})$$

SW and RF denote the two PWM frequencies; the subscript m means measurement (or simulation with foundry models) and the gains without subscript m are the gains achieved based on the proposed model.

The extraction was performed based on data obtained from a QPSS analysis of Cadence Spectre™ with TSMC 65nm process technology. The designed CDA had 30 parallel NMOS transistors and 60 parallel PMOS transistors, each having 32x6um gate fingers. After low frequency simulations and extraction of the nonlinear static part, the error function is minimized with MATLAB through the Newton method, in 32 iterations. Due to very low magnitude of R_{out}, C_{out} will not affect the results and is effectively bypassed, and is omitted in calculations. It could be used for efficiency calculations.

Table 4-I shows the extracted model parameters. The magnitude and phase of the model gain and circuit simulation gain are plotted in Figure 4-9-a to d for a load resistance of 5 ohms at an RF frequency of 200 MHz, and open circuit termination for high frequency dither at 1 GHz. Switch and RF signal amplitudes are swept in the range of 0.5 to 1 volt. The maximum error is 15 per cent for the phase and 10 percent for the gain.

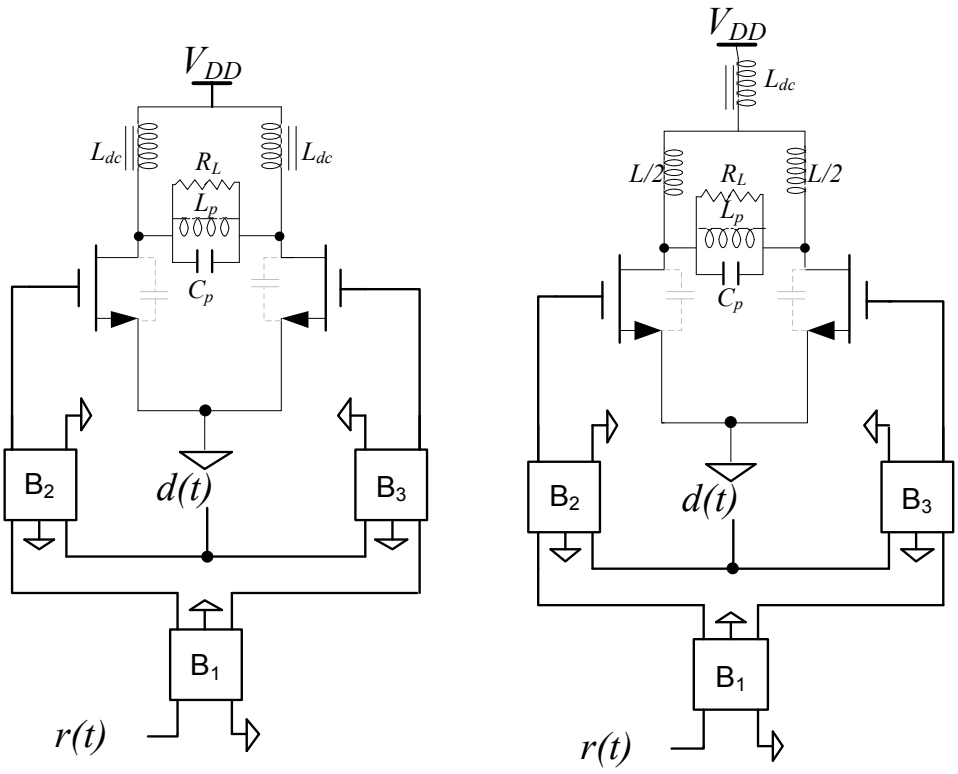


Fig. 4-10(a): ordinary CMCD; (b): CMCD with center tap inductor, to compensate the power loss in the second harmonic wherein the even order output voltage is tuned out with inductors from each drain to VDD. Inductors with double vertical bars are radio frequency chokes (RFC denoted as L_{dc}). In both cases the dithering is applied in common mode at the input.

4.2.3 Design aspects of the current mode class-D

A current mode class-D topology is based on steering a fixed current in two different directions, using two switches. Topologically, it can be assumed to be a dual circuit of the voltage mode.

The main difference is that each transistor will conduct a pulse shaped current wave-form, while the drain voltage will remain highly sinusoidal, for moderate quality factors of the LC tank.

The CMCD architecture exhibits a number of benefits over the Class-E, Voltage Mode Class-D, and F architectures. In each case, the CMCD has performance benefits in terms of either maximum frequency of operation, maximum power output, or transistor utilization. For a given transistor, CMCD produces more power than any other design including voltage mode class-D). Additionally, there is no fundamental limit on the value of the shunt capacitance in CMCD, as it is included in the tank circuit; this can be seen in Figs. 4-10-(a,b) in which Cp is effectively shunted with series connection of the transistor C_{ds} capacitors. The difference between 4-10-a and 4-10-b is that the latter has the capability of tuning the load impedance for the even output harmonics.

A tradeoff may be considered however for very large devices (high C_{ds}) between the Q of the tank and the output power. Because there is no restriction on C_{ds}, the maximum usable frequency of the CMCD is much higher than for Class E, given the same transistor. Limits on usable frequency do exist however, in the form of the transition frequency of the device, etc.

Another topologic advantage of CMCD to VMCD is that the switch capacitors, which are present especially in integrated designs, can be absorbed into the parallel tank.

Parasitic capacitances

There are two models used for intrinsic and extrinsic parasitics of the switch mode devices [80], which are shown in Fig. 4-11-(a,b). The first one is more suitable for discrete components while the second one can precisely model the integrated transistors.

Power and efficiency

The same basic types of power loss as in VMCD, exist here, but the main contributor to the loss is inductive loss (Li^2f), instead of capacitive. Like VMCD, there are two different approaches to find the voltage current waveforms of this kind of amplifier and eventually calculate the power loss, gain and efficiency.

The first approach is Fourier expansion of the drain voltages and currents of each device. Ideally the voltage is a half wave rectified sinusoidal and the current is a pulse wave-form, but

practically none of these assumptions is valid and the results achieved are very different from the practical measurements [80].

The second approach based on circuit analysis, applied to the expansion of the intrinsic drain current for all of the possible harmonics (infinite number of harmonics), and solution of the differential equation of the circuit at the output nodes with mode matching. The efficiency based on this approach is fully investigated in [81], based on the circuit model of Fig. 4-11-c, with the parasitic series inductor neglected (L_d=0). The results are:

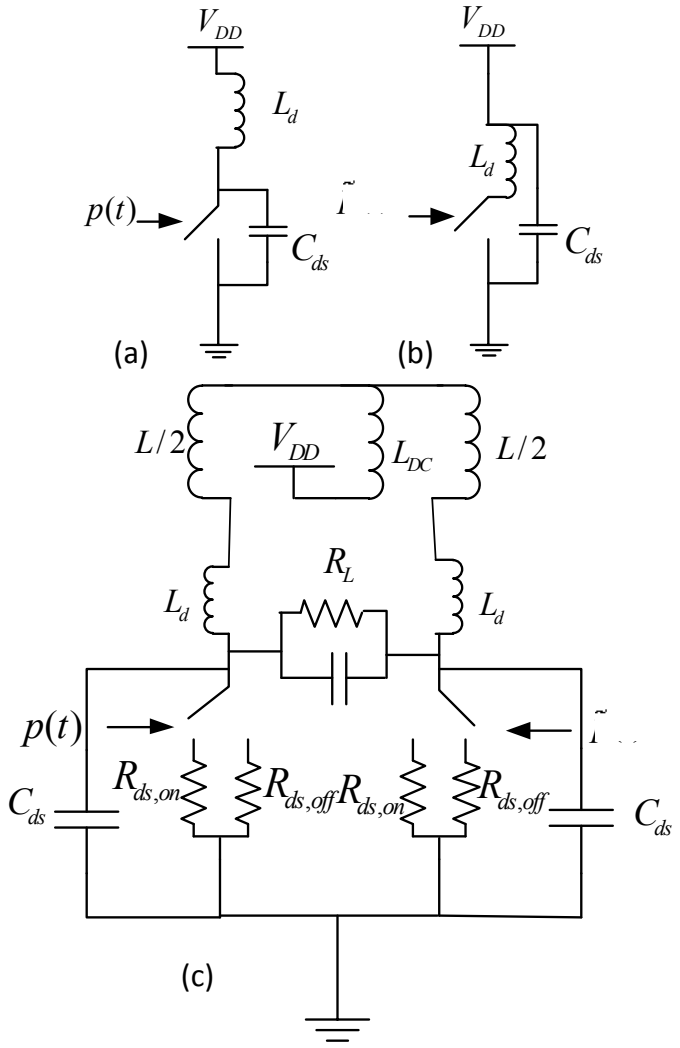


Fig. 4-11(a): Model for parasitic capacitor, for packaged transistor; (b): model for the parasitic capacitors of the IC transistor; (c): equivalent circuit including parasitic capacitances for integrated center tapped CMCD.

$$P_{out} = R_L(p^2 + q^2) \tag{4-14}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{R_L}{2R_{ds,on}}\left[\frac{p^2+q^2}{V_{DD}(V_{DD}-\frac{q}{\pi})}\right] \tag{4-15}$$

where p and q are the solutions to the following equation:

$$\begin{bmatrix} u & v \\ v & w \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{-2V_{DD}}{\pi} \end{bmatrix} \tag{4-16}$$

and u, v and w are functions of the circuit elements and the device width. The calculation details are very laborious and are given in appendix III

Design aspects

For discrete systems, the design phase consists of selection of high Q inductors and capacitors based on the required bandwidth of the system, and selection of good radio frequency chokes. The device parasitics cannot be completely compensated and optimization should be performed to maximize the efficiency, for the intended output power level.

The design of an integrated CMCD consists of two steps, which are optimization of the device width and optimization of the LC tank values. Assuming that $R_{ds,on}$ and C_{ds} are varying in form of k_1W and k_2/W, where W is the device width, then equation 4-14 results in an optimum of efficiency, for a given selection of the passive elements. This is reported in [80]. The optimum is very mild, and efficiency is not very sensitive to the device width. The next step is the selection of L and C.

The parallel LC tank always has to resonate at the fundamental frequency. For integrated passive components, the most important issue is that the higher order harmonics are not ideally short circuit terminated. Assuming that the only loss is due to the leakage of the higher order harmonics, the drain efficiently is inversely proportional to the quality factor of the capacitor [Kobayashi] ($\omega_r C R_L$) where ω_r is the signal frequency. This justifies the selection of a capacitance as high as possible (narrower bandwidth). In case of using transformers, an upper limit is put on the maximum useable capacitor.

4.3 Dithering limitations

As explained in 4.1.6, the feasibility of dithering of a nonlinear block depends on the zero input slope gain of the block. Therefore, any kind of switched mode PA, that has a high 'enough' slope gain can be dithered. If the gain is not enough the dithered gain may drop a lot due to dithering, which will decrease the power added efficiency. Therefore, it can be understood that dithering doesn't work quite well with linear PA classes like A, AB, C or J.

The second issue, besides slope gain is the dithering frequency versus process technology. For a specific PA, application of HFD will always lower the efficiency compared to the undithered state. This is because the higher frequency determines the zero crossing frequency of the output voltage or current and CV^2f ($or\ LI^2f$) loss will increase. On the other hand performing LFD on a specific PA will effectively reduce the switching frequency depending on the frequency and level of the dither. Thus LFD is always beneficial in terms of *reactive* power loss.

This issue is explained in Fig. 4-12, in which the zero-crossing frequency is plotted versus the ratio between the dither amplitude (A) and signal amplitude (r) [22]. This Figure shows that as the dither amplitude A increases, the switching frequency will drop effectively and thus will the CV^2f loss. The decline in loss value will depend on the capacitor (or inductor) value which is in turn a function of process technology (C and V). Hence the more parasitics we have in a given process technology, the more improvement in the reactive power loss we get through LFD.

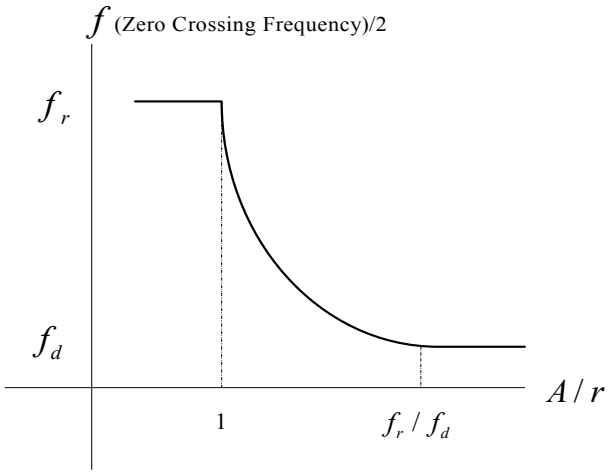


Fig. 4-12: The zero crossing frequency of the sum of two sinusoids at frequencies f_r and f_d , with amplitudes r and A, representing signal and dither amplitudes, versus A/r.

4.4 Conclusion

In this chapter, system architectures and circuit topologies that can be used in combination with dithering were investigated. It is shown that a dithering topology can be implemented in forward and closed loop architecture, with and without an auxiliary envelope tracking, to enhance linearity and average efficiency. It was shown that dithering might be implemented in the forward, feedback, load network as well as in tracking paths.
It was proven that the slope gain of the switching amplifier plays a crucial role on the performance of a dithered system and low frequency dithering can significantly decrease the reactive power loss and consequently increase the efficiency in combination with linearity. The voltage

and current mode Class-D amplifiers where shown to be the best candidates for the realization of the required switching amplifier because of the highest slope gain among other PA classes.
It is shown that the equivalent circuit for CMCD has enough accuracy, and the models are accurate enough for predictions, but that is not the case for VMCD. Therefore a new parasitic model for fast and accurate simulation of VMCD was proposed and its parameters were extracted.
The insight achieved in this section will be used in the coming chapters to design and optimize VMCD, SOPA and LDMOS CMCD in the chapters 7 and 8.

Chapter 5

Linearity analysis

Modern wireless communication systems utilize sophisticated modulation techniques to achieve higher data rates or improvements in overall system capacity. Amplitude variations in the modulated waveforms give rise to distortion products when applied to nonlinear components of the transmitter. Distortion emissions from mobile handsets are restricted to prevent system degradation and interference to users in adjacent cells. Thus when designing a power amplifier component, it is important to quickly determine the distortion generated by the circuit when a modulated signal is applied.

Consequently, only approaches that yield accurate results in a short amount of time are useful in the design process. Methods that yield higher accuracy, but take a long amount of simulation time are not useful in the first design phase and development of new products. Thus, tradeoffs are made when selecting an analysis method to assist in the assessment of transmitter linearity and efficiency.

Furthermore, the dithered system that is studied in this thesis is much more complicated than an ordinary class AB amplifier and two different kinds of distortion exist, which can be categorized as spurious distortion and inherent distortion, originating from an equivalent nonlinearity function. Different system configurations like open loop, closed loop with negative feedback and self-oscillating closed loop have slightly different regimes of behavior and different analysis types should be distinguished for different system architectures and input statistics.

The existing analysis methods have many shortcomings and limitations. Moreover classical nonlinearity metrics such as harmonic level for single sinusoidal excitation level, or P_{ndB}, can be achieved based on existing theories [1] but they fail to provide the necessary information for linearity analysis of a generic modulated input signal with an arbitrary crest factor, because digitally modulated signals are far more complicated than a two tone signal.

The linearity analysis approach provided in this chapter is a three step approach based on correlated and uncorrelated analysis of the output signal and orthogonalization of the output with respect to the input signal. Therefore, in-band distortions can be distinguished from the total distortion power, which can be utilized to find the co-channel types of nonlinearity required to find metrics like EVM and SNDR.

The chapter is organized as follows: In section 5. 1, existing analysis methods and their shortcomings are introduced, to clarify the need to have a generic analysis approach. In 5.2 the signal types being used in the analysis are introduced. In 5.3 the proposed method is introduced and explained in detail for distortion analysis of a normally dithered open or closed loop and self-oscillating systems, and nonlinear metrics are derived. Moreover the memory effect models are studied in depth and a memory model is applied to the dithered system for wide-band signals.

5.1 Existing methods and shortcomings

State of the art analysis methods, like Transient, Harmonic Balance or Circuit Envelope method, which are fully developed in the current commercial simulator engines, are powerful but not insightful regarding the mechanisms of nonlinear behavior of the topology and the individual block contributions on overall nonlinearity metrics like spectral re-growth and Error Vector Magnitude (EVM). Moreover they have convergence problems, especially for self-oscillating systems, which are autonomous so that the oscillation frequency is mostly unknown for the simulator at the beginning.

Series expansion and time domain analysis of the output PWM signal [9], [84], [11],[81] is used to predict the modulation sidebands around the limit cycle frequency but is still unable to give the in-band distortions for a generic modulated input signal to a self-oscillating power amplifier (SOPA). Moreover in a real scenario, the output waveform of a SOPA is not an ideal PWM modulated pulse train. Memory effects of the amplifier are not addressed in the series expansion and the distortion results are not complete and don't address complicated digital modulations.

Describing function approach is another way to analyze the behavior of these systems. The Two Sinusoidal Input Describing Function (TSIDF) approach gives the linear parameters of the system like gain and oscillation frequency for a sinusoidal input signal, in a straightforward way.

An extension to the harmonic linearized TSIDF method for SOPA, is given in [1] which employs the value of the third order harmonic with single tone excitation, based on series expansion of the describing function, to approximate the output Multi-Tone-Power-Ratio (MTPR). The two tone characterization of nonlinearity cannot accurately address all of the nonlinear metrics required to characterize a dithered PA, such as ACPR and EVM and memory effects. The same method can be generalized to address the multisine input signals [81], at the cost of exceedingly increased computational complexity regarding describing functions of a generic n-tone input as well as higher order partial derivative calculations for each input tone, when the input amplitude is increased. Another issue is that the in-band nonlinearity is overlooked and it is not possible to orthogonalize the output signal to correlated and uncorrelated parts, in order to derive EVM. Moreover, the assumption in simple SIDF approach underlies memoryless or static performance of the amplifier. This assumption is not generally valid, especially not for wideband input signals.

5.2 Signal specifications

In this section, different kinds of signal distributions that are used for signal modeling in the linearity analysis are discussed and methods of modeling those signals using Multisine are explained.

5.2.1 Probability distributions

For clarity, we categorize the signals statistically: real and complex Gaussian signals. The former is described with the following PDF:

$$p(r) = \frac{1}{\sigma_r\sqrt{2\pi}} \exp\left(-\frac{r^2}{2{\sigma_r}^2}\right) \tag{5-1}$$

where r is a Narrow Band Gaussian Noise (NBGN) on itself or being carrier modulated. The latter is a complex Gaussian signal, as a quadrature sum of two independent zero means real signals as follows (5-2):

$$\tilde{r}(t) = i(t) + jq(t) \tag{5-2}$$

where i and q have PDF's of the form of (5-1).

The real Gaussian signal can represent a multi carrier signal for a large number of carriers, according to the central limit theorem. The complex Gaussian signal models a large number of frequency-multiplexed traffic channels around a single carrier, when the complex envelope of the modulated signal mimics a Gaussian process, like a WCDMA forward link [85].

5.2.2 Multisine representation of signals

A multisine signal consists of a sum of several simultaneously generated sinusoids (tones). Equation (5-3) presents a typical multisine signal:

$$r(t) = \sum_{i=1}^{N} A_i \sin(\omega_i + \theta_i) \quad (5\text{-}3)$$

where A_i is the amplitude and θ_i is the phase of the kth sinusoid, N is the number of sinusoids, and $\omega_i = \omega_0 + (i-1)\,\omega_{res}$, with ω_0 being the frequency of the first tone and ω_{res} the constant frequency separation between them. By changing the relative phase between each of the frequency components in the multisine, we are able to change the time-domain envelope associated with the multisine. Fig. 5-1 illustrates a 802. 11.g signal and its 52 tone multisine representation.

There are at least five reasons to use multisine signals in design and test:

- It is straightforward to change the statistics of multisine signals by changing the relative phase between their components. Using algorithms such as the one presented in subsection 5.1.2, we can readily synthesize different types of excitations that can mimic digital modulations of interest.
- Multisines are periodic signals. Periodic signals are straightforward to generate and measure by using many instruments commonly used to characterize band pass modulated signals such as vector signal generators, spectrum analyzers, vector signal analyzers, and large-signal network analyzers (LSNAs). In fact, some instruments such as the LSNA require the use of periodic excitations.
- It is possible to build a multisine with a few frequency components, which can model the

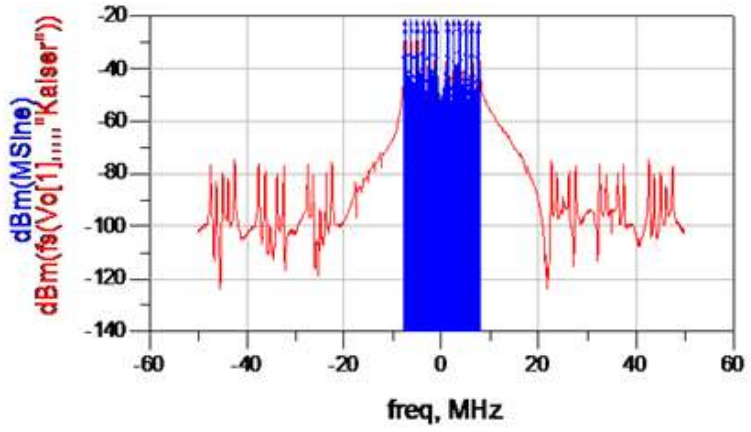


Fig. 5-1: A 802.11g signal and its multisine approximation

exact statistics of the intended signal. This issue can hugely reduce the test and simulation time.

- Multisine is composed of sine waves; it is a relatively straightforward task to characterize the harmonic distortion in the excitation signal by a simple fit to ideal sine waves.
- Finally, when carrying out common wireless system measurements such as harmonic distortion, intermodulation distortion, frequency-selective fading, or other tests where phase plays a role, knowledge of the phases at the input and output of the system under test can give insight into distortion-causing mechanisms. The use of sine waves facilitates this.

The drawback of using multisine can be accuracy of simulation, depending on the type of multisine that is extracted. There are two major methods to design a multisine, which are discussed in the following sections, namely DFT method and statistical method.

5.2.3 DFT method to extract multisine

One goal of multisine signal analysis is to extend the analytic simplicity of two-tone nonlinear system analysis to more complicated signals. However, the two questions that quickly arise when designing multisine signals to accurately represent wireless communication signals are:

1. How many sinusoids should be used? and
2. How should the amplitude and phase of each sinusoid be determined?

One straightforward approach to answering both questions is to consider a Fourier series representation of the communication signal, since it defines the signal as a sum of sinusoids. In practice, a DFT is used to obtain Fourier series coefficients of a complex signal of finite time duration [26]:

$$r[n] = IDFT\big[R[k]\big]$$

$$= \frac{1}{N}\sum_{k=0}^{N-1} R[k].\exp\left[\frac{j2\pi kn}{N}\right] = \frac{1}{N}\sum_{k=0}^{N-1} A_k.\exp\left[\frac{j2\pi kn}{N} + \theta_k\right] \quad (5\text{-}4)$$

where $IDFT$ is the inverse DFT operator, and A_k and θ_k are obtained from a DFT of the desired time domain signal. The DFT generates N Fourier coefficients for N time samples. The signal length is defined in the time domain by the time of the end sample minus the time of the start sample. This is inversely related to the frequency resolution of the DFT. The longer the signal length, the finer the frequency resolution. A simple solution to minimize the number of sinusoids is to simply remove the frequencies that are outside the bandwidth of the desired signal. In practice, the truncated bandwidth should be larger than the actual signal bandwidth by approximately 20% to minimize any error between the original signal and the truncated multisine representation of the signal [86]. In this way the number of tones will be:

$$N_{tones} = 1.2\frac{\Delta f}{f_{res}} = 1.2\Delta fT \quad (5\text{-}5)$$

This method maintains high accuracy in representing the amplitude, phase, and bandwidth characteristics of the original signal; however, there may be cases where the signal length of interest generates too many tones to be practical for circuit simulations or analytical techniques. This motivates the need to investigate alternative techniques for generating compact multisine representations with the characteristics of practical communication signals for nonlinear circuit analysis.

5.2.4 Statistical synthesis methods

For a memory-less nonlinearity, first-order statistics such as the PDF and its associated moments are sufficient for describing the integrated value of distortion power. There are several ways to synthesize a desired multisine PDF. One useful technique involves an algorithm that automates the procedure of generating a multisine PDF to approximate the PDF of previously synthesized noise sequences [77], [17].

This approach starts with the synthesis of a noise signal, with a prescribed PDF, and a multisine, with prescribed number and frequency position of tones. Then it recursively tries to replace the time samples of the multisine with those of the synthesized noise, to form it corresponding to the required PDF. This approach can effectively reduce the number of tones, compared to *DFT* method, but for systems with high memory effects, higher order statistics should be matched to the information signal [17]. The details can be found on [86], [77] and are not brought here. The method used in this thesis is the DFT method.

5.3 Proposed method

Having an accurate, fast and insightful behavioral model is of invaluable importance for any kind of dithered nonlinear system, especially in the initial design phase. To tackle the above shortcomings, this chapter presents a new analytical method to accurately characterize all of the required spectral metrics caused by a dithered class-D amplifier (CDA), excited by a ran-

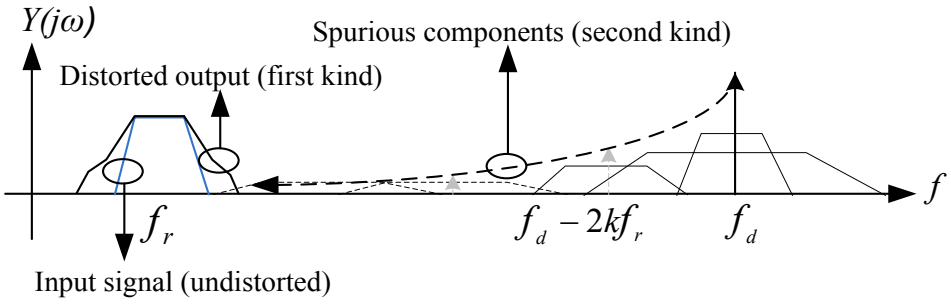


Fig. 5-2: The output spectrum, consisting of first and second kind nonlinearities, arising from equivalent nonlinearity and spurious distortion components, the spectral density is for HFD, a similar plan exists for LFD.

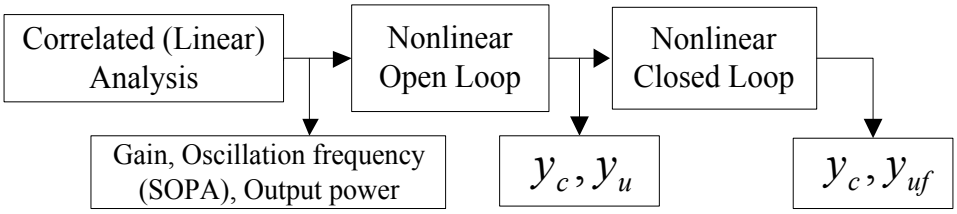


Fig.5-3: Three major steps in nonlinear statistical analysis of a dithered power amplifier, for analysis of the first kind of nonlinearity

dom input signal, with Gaussian statistics, in a time-efficient way.

As described in chapter 2, and illustrated in Fig. 5-2, there are two types of distortion in the output of dithered systems:

1. Distortion that is caused by the nonlinearities of the equivalent nonlinearity function (chapter 2), and that is normally in the same band as the message signal and cause co-channel and adjacent channel distortion, and
2. Distortion components that are originated by the spurious sidebands around the dither frequency and its harmonics.

The analysis method given in this section is suited for the first kind of nonlinearity, based on describing function and equivalent nonlinearity. The behavioral model for spurious components for a generic random signal will be presented in chapter 6.

The objective of the linearity analysis is to find the distortion and signal to distortion ratio. Having the autocorrelation function of the output signal enables us to find the output spectrum.

As mentioned before, the linearity analysis in this section is divided into two distinctive parts, namely finding correlated and uncorrelated outputs, where the total output can be written as:

$$y(t) = y_c(t) + y_u(t) \tag{5-6}$$

and the auto-correlation of the signal that is sum of the autocorrelations of y_u and y_c.

The analysis is based on three steps as illustrated by Fig. 5-3:

- The first step is a correlated analysis, or finding y_c in equation (5-7) with describing function method for real and complex Gaussian signals. The objective of this step is to calculate the amplitudes of the desired output signal (which is totally correlated with

the input). The term "Correlated Analysis" is the process of finding the correlated output part of the system (with the input signal), and is different from small signal analysis. For the closed loop systems, the problem is that the correlated input to the CDA is not known. Moreover for a SOPA, the exact frequency of operation and the exact limit cycle amplitude is not given a priori. Correlated analysis should be able to find these quantities. The gain of the system will be known by this step.

- The second step uses the desired signal autocorrelation from the previous step to predict the open loop output autocorrelation (R_{yy}) of the CDA. The goal is to write the output in-band autocorrelation of the CDA, based on the input signal statistics.
- The last step separates the output autocorrelation into correlated and uncorrelated parts (y_u and y_c), with the input signal (orthogonalization), i.e. the series expansion should be able to distinguish between the correlated and uncorrelated parts of the output spectral density. The correlated part remains intact and the impact of the negative feedback on the in-band uncorrelated part is calculated, to obtain the nonlinear behavior of the loop.

These three steps are explained in sections 5.4 to 5.6.

5.4 Correlated analysis

The objective is to find all of the input-correlated signals (y_c in equation (5-6)) in various part of a general dithered system. The results will be used in 5.5 for nonlinear analysis.

5.4.1 Open loop

The open loop is illustrated in Fig. 5-4-a. The describing function approach, introduced in chapter 3, can easily be applied to find the output parts correlated with corresponding inputs. For Fig. 5-4-a, the correlated output is composed of a sinusoid and a random signal that is totally correlated with the input signal $r(t)$:

$$y_c(t) = N_r(A, \sigma_r).r(t) \tag{5-7}$$

where $N_r(A, \sigma_r)$ is the random input part DF and was introduced in chapter 3.

5.4.2 Closed loop

The block diagram of the open and closed loop dithered relay power amplifier is illustrated in Fig. 5-4-(a,b). In a closed loop system, filters H_1, H_2, subtraction G_s and forward gain block G_F, provides a negative feedback loop combined with a class-D amplifier.

The output reconstruction filter H_3 separates the desired part of the output signal spectrum from the rest and also performs the impedance matching to the optimum CDA load impedance. The CDA itself may be a single or multi-stage voltage or current mode class-D and it is

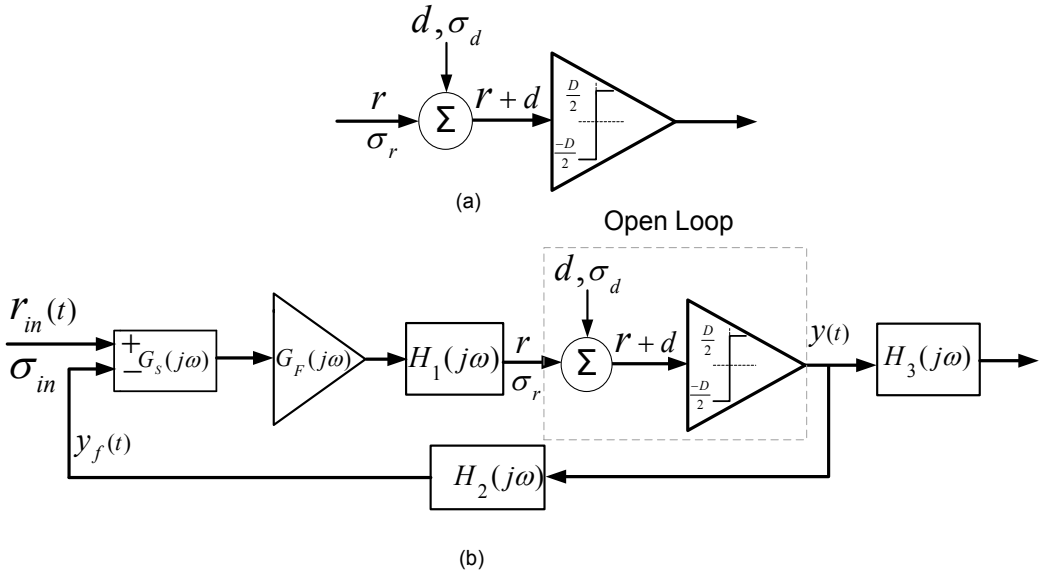


Fig.5-4(a): open loop system; (b): externally dithered closed loop CDA, the dashed box is the open loop part of the system

assumed that the amplifier is memory-less and is described by a static nonlinear relation-ship for output voltage versus input voltage.

The correlated part and uncorrelated output parts are denoted by y_c and y_u. The correlated part is the linear transformation of the input signal while the uncorrelated part arises from the distortion of the equivalent nonlinearity.

For the closed loop system, the problem is that the part of the random input signal that reaches the CDA input, is not known. If we call the input rms voltage to the CDA σ_r, then according to the notation of Fig. 5-4-b we can write:

$$H(j\omega, A, \sigma_{in}) = \frac{\sigma_r}{\sigma_{in}} = \left| \frac{H_1.G_{S.}G_F(j\omega)}{1+H_1H_2.G_{S.}G_F(j\omega).N_r(A,\sigma_r)} \right| \tag{5-8}$$

where σ_{in} is the standard deviation of the input Gaussian signal to the loop and $N_r(A, \sigma_r)$ is the random DF. The random excitation can be either complex or real Gaussian, as discussed before in chapter 3, and in each case the corresponding DF should be used. The solution of (5-8) does not result in any closed form formula and an iterative method numerical method should be taken to find σ_r for each σ_{in}.

For the self-oscillating loop, the dither component is generated by the system limit cycle. The main difference in correlated analysis of the SOPA and normally dithered loop of Fig. 5-4-b is that the amplitude of the limit cycle or dither is a function of the input amplitude. The block diagram of a SOPA is shown in Fig. 5-5 where the signal d(t) is the limit cycle, generated autonomously.

The Barkhausen criteria, which are round trip loop gain one and round trip phase of zero are:

$$real\left(G_F.G_s.H_1.H_2(j\omega_{LC}).N_A(A,\sigma_r)\right)=-1 \quad (5\text{-}9\text{-a})$$

$$imag\left(G_F.G_s.H_1.H_2(j\omega_{LC}).N_A(A,\sigma_r)\right)=0 \quad (5\text{-}9\text{-b})$$

These equations have three unknowns: oscillation frequency: ω_{LC}, oscillation amplitude A and signal rms-value σ_r at the input of the CDA. The third equation that can be used is equation 8. Therefore correlated analysis for the Gaussian transfer function requires knowledge of the signal rms value and dither amplitudes at the input of the CDA, obtained from the solution of equations (5-9 a-b and 5-8). This solution doesn't have an analytic way and only numeric approaches can be taken for a given input rms value, in a recursive way: first two values are assumed for input rms voltage σ_r and A in a range between ground and supply voltage; Idle mode oscillation amplitude is a good starting point for A. Based on (5-8) and (5-9-a), a new value is calculated for σ_r and A and used to replace the old values, and this process is recursively repeated to achieve a certain accuracy.

Fig. 5-5 shows the extracted σ_r and A values versus the input rms voltage σ_{in}, for a limit cycle loop, with one percent iterative accuracy. As illustrated in Fig.5-6, the limit cycle amplitude decreases by increasing the input voltage, and at some level, the oscillations will quench, due to insufficient loop gain.

For the ordinary (non-autonomous) system of Fig. 5-4-a, only equation (5-8) is valid, which is enough to find σ_r from σ_{in}. For the SOPA, continuation of oscillation puts an upper limit for the input range, i.e. for equal limit cycle and input rms value we can write:

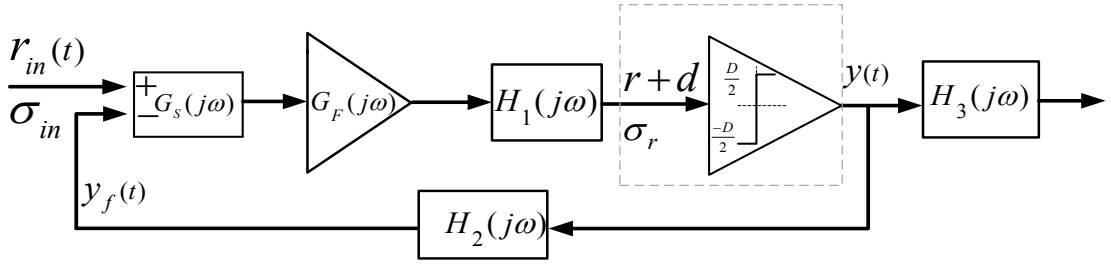


Fig.5-5: Self-oscillating closed loop dithering, in which the limit cycle oscillation plays the role of the dither *d*. In both diagrams, the dashed box represents the open loop structure

$$\sigma_{in,max}=D\sqrt{\frac{1}{2\pi}}\left|H_2(\omega_r)+\frac{G_L(\omega_{LC})}{G_F(\omega_r)}\right| \quad (5\text{-}10)$$

where $G_L(\omega_{LC})$ is the gain of the loop except CDA at the limit cycle frequency. Equation (5-10) is achieved based on the oscillation conditions of equations 5-9-a,b.

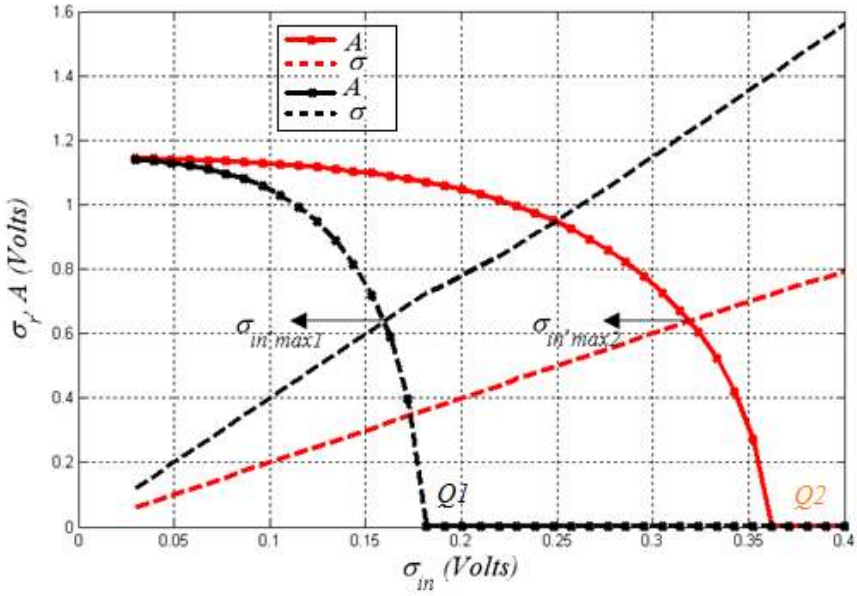


Fig. 5-6: The CDA input and limit-cycle amplitude versus input rms level; $D = 3\ Volts, G_f(\omega_r) = 2{,}4$, maximum input level for linear performance is illustrated by $\sigma_{in,max1,2}$, and the quenching thresholds are denoted by *Q1* and *Q2*.

After finding the correlated solution for σ_r, either for the system of Fig. 5-4-b or the SOPA in Fig. 5-5, the linear transfer function from loop input to loop output can be obtained as follows:

$$T(j\omega, A, \sigma_{in}) = \frac{\sigma_{out}}{\sigma_{in}} = \frac{H_1.G_S.G_F(j\omega).N_r(A,\sigma_r)}{1+H_1.H_2.G_S.G_F(j\omega).N_r(A,\sigma_r)} \tag{5-11}$$

which is the closed loop voltage gain.

Considering the limit cycle component as a dither signal, means that from now on the systems of Fig. 5-4-b and Fig. 5-5 are equivalent, assuming the dither is independent of the input signal amplitude. Therefore from now on, we have two kinds of systems: closed and open loop, both with external dither signal $d(t)$ at the summing point as shown in Figures 5-4-(a,b). Again it should be emphasized that, as illustrated in Fig. 5-6, there is a point for SOPA in which the dither and signal amplitudes become equal and after that, the dither amplitude will abruptly decline, and the oscillation will quench at some point (Q_1 and Q_2 in Fig. 5-6).

5.5 Nonlinear analysis

As mentioned before the first step in the linearity analysis is the correlated analysis, as discussed in the previous chapter. With that, the open loop results are derived, which will in the next step discussed in this chapter be used to obtain the closed loop distortion in a generic closed loop dithered architecture.

5.5.1 Open loop real Gaussian

As stated so far, the objective of nonlinear analysis is to write the output autocorrelation versus the input one. According to Fig. 5-4, the latter is assumed to be a linear transformation of the loop input signal autocorrelation $R_{rin,rin}(\tau)$. This auto-correlation can be written versus the loop input autocorrelation as follows:

$$R_{rr}(\tau) = (\frac{\sigma_r}{\sigma_{in}})^2 . R_{rin,rin}(\tau) \tag{5-12}$$

For real Gaussian signals, the effect of the dithering linearization on the CDA can be explained and quantified with a set of coefficients, relating the output autocorrelation to the input auto-correlation function of the CDA. Equations (5-13),(5-14) below show this relationship:

$$R_{yy}(\tau) = \sum_{k=1}^{\infty} c_k^2 R_{rr}^k(\tau) \tag{5-13}$$

$$c_k(A, \sigma_r) = \frac{(2\pi)^{-\frac{3}{2}}}{\sigma_r \sqrt{k!}} \int_{-\infty}^{\infty} e^{-\frac{r^2}{2}} H_k(r) g_0(\sigma_r r, A) dr \tag{5-14}$$

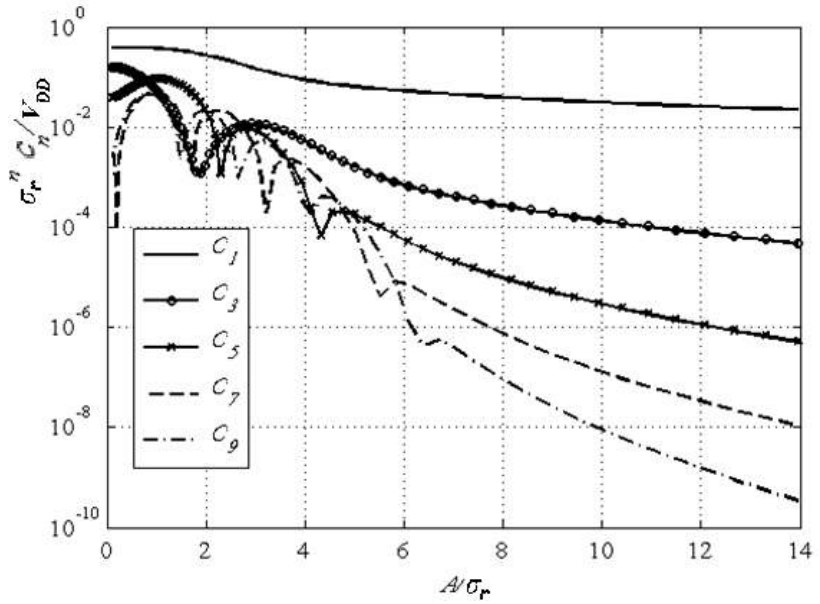


Fig. 5-7: Universal normalized coefficients, versus A/σ_r.

where $H_k(r)$ is the k'th order Hermite polynomial [9] and its orthogonal properties are discussed in [4]. Equation (5-13),(5-14) are based on orthogonal expansion of the output auto-correlation of a static nonlinearity for a real Gaussian input, and making use of orthogonality property of Hermite polynomials [4], [9], [69].

For first order auto-correlation, $c_1(A, \sigma_r)$ is the same as the random input describing function $N_r(A, \sigma_r)$ for real Gaussian signals. Closed form formulas are obtainable for the coefficients when the nonlinear block is an ideal relay; the results are plotted in Fig. 5-7.

Equation (5-13) can be expressed in frequency domain, as a summation of autocorrelations as:

$$S_{yy}(\omega) = S_{ycyc}(\omega) + S_{yuyc}(\omega)$$

$$= \mathcal{F}(\sum_{k=1}^{\infty} c_k^2 R_{rr}^k(\tau))$$

$$= \sum_{k=1}^{\infty} c_k^2 . S_{rr}^{k*}(\omega) \quad (5\text{-}15)$$

where S_{rr} and S_{yy} are the power spectral densities and $k*$ operator denotes the k'th order self-convolution of the operand and

$$S_{yy}(\omega) = \mathcal{F}(R_{yy}(\tau)) \, , S_{rr}(\omega) = \mathcal{F}(R_{rr}(\tau))$$

S_{ycyc} and S_{yuyu} are the first term and the rest of the summation of equation 5-15 respectively. Based on (5-13),(5-14), the nonlinear analysis of the structure is reduced to the calculation of a weighted sum of self-convolutions of the input signal spectral density to the CDA.
For a modulated real Gaussian signal, the linear analysis steps are the same as the Gaussian

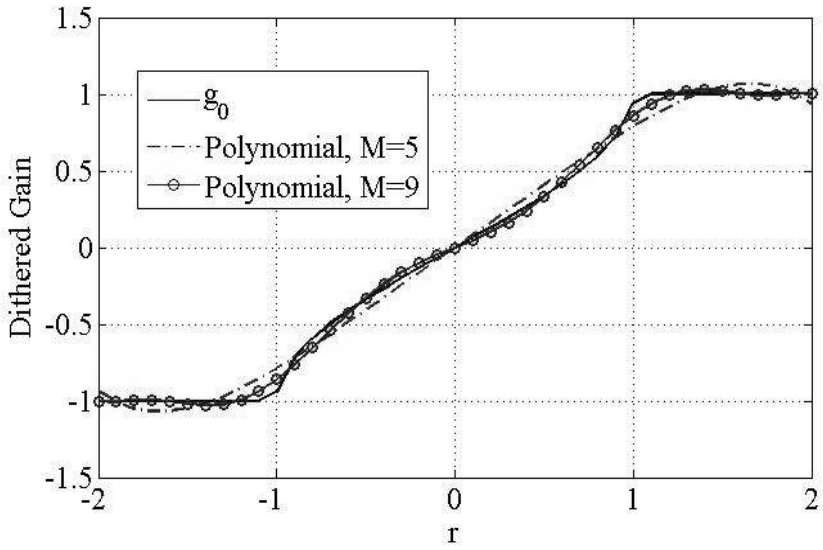


Fig.5-8: Normalized dithered Gain of the in-phase component ($g_{0I}(r, 0, A)$ function and two polynomial fits, versus input value, for hyperbolic CDA versus curve fitting.

value analysis method. The correlation coefficients for real envelope can be derived from the following integral:

$$C_k(A, \sigma_r) = \frac{(2\pi)^{-\frac{3}{2}}}{\sigma_r \sqrt{k!}} \int_{-\infty}^{\infty} g_{0I}(\sigma_r r_1, 0, A) \, H_k(r_1) . \exp\left(-\frac{r_1^2}{2}\right) dr_1 \quad (5\text{-}16)$$

where g_{0I} is the equivalent nonlinearity as introduced earlier in chapter 2. The uppercase coefficient C_k is used to differentiate between the real amplitude modulated Gaussian signal. The output autocorrelation can be written as follows:

$$R_{yy}(\tau) = \sum_{k=3}^{\infty} \left(C_k^2 R_{ii}^k(\tau) \right) \tag{5-17}$$

Therefore the autocorrelation of a real modulated Gaussian is readily calculated in a manner similar to the open loop real Gaussian. For full proof, see [69].

5.5.2 Open loop complex Gaussian

The closed form expression of (5-15) is only valid when the cross correlations of different orders of in-phase and quadrature parts of the signal are zero which is not a valid assumption in general. Therefore the same approach can't be extended in closed form for complex Gaussian envelope. The solution proposed in this part is based on the polynomial expansion of the zonal nonlinear transfer function and derivation of the output autocorrelation versus input one.

Using the transfer function in (5-8), the amplifier input complex envelope can be obtained as follows:

$$\tilde{r} \triangleq i + jq = \tilde{r}_{in}.\frac{\sigma_r}{\sigma_{in}} \tag{5-18-a}$$

The equivalent nonlinearity for the real signal can be expanded in Taylor series as:

$$g_0(r, A) \approx \sum_{k=1}^{M} b_k(A).r^k \tag{5-18-b}$$

$$r = \sqrt{i^2 + q^2}\sin\left(\omega_r t + tan^{-1}\left(\frac{q}{i}\right)\right) = Real\left(\tilde{r}.e^{j\omega_r t}\right). \tag{5-18-c}$$

As illustrated in Fig. 5-8 the truncated polynomial results are in good agreement g_0 for orders higher than 5, for a hyperbolic CDA.

In order to reduce the sampling rate of the modulated narrow-band signal r, which is at least 2 times f_r for high frequency dithering, or to the complex envelop bandwidth (the same as i and q bandwidth) and to separate the in-band distortion of the output-envelope versus input-envelope auto-correlation, we will write the series expansion of equation (5-18-b) in terms of complex envelope as follows:

$$G_{\omega_c}\left(\tilde{r}(t)\right) = \sum_{k=0}^{\frac{M-1}{2}} \tilde{b}_{2k+1}\,\tilde{r}^{k+1}\,[\,\tilde{r}^*]^k \tag{5-19-a}$$

Where $G_{\omega_c}(.)$ is the equivalent nonlinear polynomial for complex envelope and $\tilde{b}_{2k+1}$ is:

$$\tilde{b}_{\,2k+1} = \frac{b_{2k+1}}{2^{2k}}\binom{2k+1}{k+1} \tag{5-19-b}$$

For a general quadrature modulated signal, the output autocorrelation is derived from the following equations in time domain:

$$\tilde{R}_{yy}(\tau) \triangleq \lim_{t\to\infty} \frac{1}{2T} \int_{-T}^{T} G_{\omega_c}\big(\tilde{r}(t)\big)\, G^*_{\omega_c}\big(\tilde{r}(t)\big) dt \tag{5-20-a}$$

while:

$$G_{\omega_c}\big(\tilde{r}(t)\big) G^*_{\omega_c}\big(\tilde{r}(t)\big) = \sum_{k=0}^{\frac{M-1}{2}} \sum_{l=0}^{\frac{M-1}{2}} \frac{\tilde{b}_{2k+1}\tilde{b}_{2l+1}}{2^{2(l+k)}} \binom{2k+1}{k+1} \binom{2l+1}{l+1} \tilde{r}_1^{n+1} (\tilde{r}_1^*)^n \tilde{r}_2^{l} (\tilde{r}_2^*)^{l+1} \tag{5-20-b}$$

and $\tilde{r}_1 = \tilde{r}(t)$, $\tilde{r}_2 = \tilde{r}(t+\tau)$. (5-20-c)

After substituting (5-20-b) in (5-20-a) and application of the theorem of the moments of complex Gaussian variables, according to the previous works on band-pass nonlinearities in [6], we can write:

$$\tilde{R}_{yy}(\tau) = \sum_{k=1}^{M} \tilde{R}_{yy}^{2k+1} \tag{5-21-a}$$

$$\tilde{R}_{yy}^{2k+1} \triangleq \left| \sum_{n=k}^{\frac{(M-1)}{2}} \frac{\tilde{b}_{2n+1}.(2n+1)!}{2^{2n}(n-k)!} \tilde{R}_{r0}^{\,n-k} \right| \frac{\tilde{R}_{rr}^{k+1}[\tilde{R}_{rr}^*]^k}{k!(k+1)!} \tag{5-21-b}$$

While $\widetilde{R}_{r0} = \widetilde{R}_{rr}(\tau = 0)$ and $\check{R}_{rr} = R_{ii+}R_{qq} - j2R_{iq}$[6]. The only difference between the current formulas and previous work is that the coefficients here are a function of the dithering signal. Equations 5-21-(a, b) give the output autocorrelation, directly versus input autocorrelation of different orders. For ideal relay, the analytical expression for coefficients $\tilde{b}_k$ can be derived from Taylor expansion of the g_0, which is inverse sinusoid of the input value [69].

5.5.3 Closed loop distortion

Fig. 5-9 illustrates the adopted nonlinear analysis approach for the closed loop system. The difference between the open and closed loop is the effect of the feedback loop on nonlinear intermodulation. The output can be decomposed in two different parts with respect to the input signal: correlated and uncorrelated. For the correlated part, which is the first term of the series in (5-13), the loop performance is completely linear and everything is taken care of in equations (5-8),(5-9),(5-10), but the uncorrelated part will be subsequently processed by the feedback loop, and then appear in the output terminal [87], which is modeled as the summing point for the distortion in Fig. 5-9.

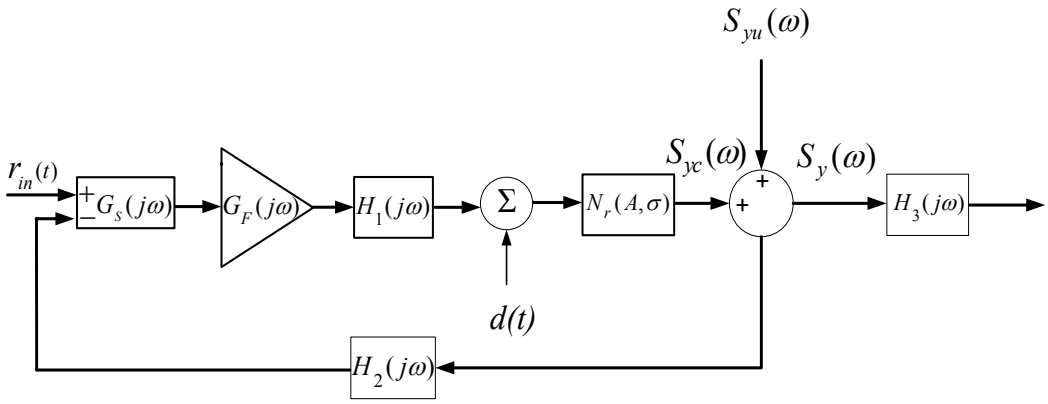


Fig.5-9: The nonlinear analysis in the closed loop structure

From now on, the frequency dependent part of the loop gain should be used according to the frequency of the distortion. The output of the open loop part can be decomposed to two correlated and uncorrelated parts as follows:

$$S_{yy}(\omega) = S_{yuyuf}(\omega) + S_{ycyc}(\omega) \tag{5-22}$$

$$S_{ycyc}(\omega) = \mathcal{F}(|N_r(A,\sigma_r)|)^2 R_{rin,rin}(\tau) \tag{5-23}$$

$$S_{yuyuf}(\omega) = \left(\mathcal{F}\left(R_{yy}(\tau)\right) - S_{ycyc}(\omega)\right).\left|\frac{1}{1+G_L.N_r(A,\sigma_r)}\right|^2 \tag{5-24-a}$$

$$G_L = G_s G_F H_1 H_2 \tag{5-24-b}$$

where $\mathcal{F}$ denotes the Fourier transform operator. The second term in multiplication of (5-24-a) shows the effect of the loop gain on the total distortion power, and the subscript f in S_{yuyuf} refers to the (negative) feedback effect.

5.5.4 Nonlinear metrics calculation

Equation (5-24-a) can be used to find the in-band nonlinear components for any Gaussian excitation and to study the effect of various system parameters (e.g. supply voltages, forward and feedback gain and frequency response) on the output distortion. EVM can be calculated in terms of the ratio of un-correlated co-channel distortion over correlated signal power, as stated below [72]:

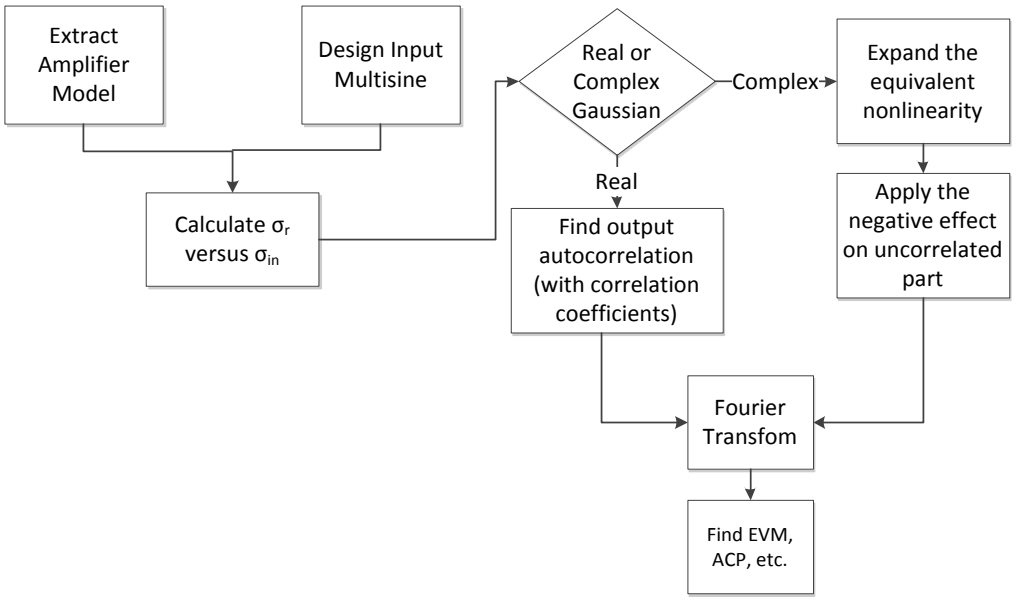


Fig. 5-10: Flowchart of the statistical linearity analysis method.

$$EVM \stackrel{\text{def}}{=} \frac{\int_{f_r-\frac{\Delta f}{2}}^{f_r+\frac{\Delta f}{2}} S_{yu}(\omega)d\omega}{\int_{f_r-\frac{\Delta f}{2}}^{f_r+\frac{\Delta f}{2}} S_{yc}(\omega)d\omega} \tag{5-25-a}$$

and ACPR is the ratio of the adjacent channel power to the co-channel power:

$$ACPR \stackrel{\text{def}}{=} \frac{\int_{<Adj>} S_y(\omega)d\omega}{\int_{f_r-\frac{\Delta f}{2}}^{f_r+\frac{\Delta f}{2}} S_y(\omega)d\omega} \tag{5-25-b}$$

Having the uncorrelated distortion at the output of the amplifier, it is possible to calculate all other system nonlinearity metrics like SNR, Noise Power Ratio (NPR), etc. The flowchart of Fig. 5-10 sums up the entire nonlinear analysis method.

5.6 Memory effects

In the framework of system identification theory, the PA is described by a system operator that maps a function (or vector of functions) of time $x(t)$ (the input signal) onto another

function (or vector of functions) of time $y(t)$ or the output. This way, the input–output map of our PA can be represented by the following forced nonlinear differential equation:

$$f(y(t), \frac{d(y(t))}{dt}, \dots, \frac{d^M(y(t))}{dt^M}, x(t), \frac{d(x(t))}{dt}, \dots, \frac{d^N(x(t))}{dt^N}) = 0 \tag{5-26}$$

System identification results have shown that, under a broad range of conditions [89] (basically; operator causality, stability, continuity, and fading memory), such a system can also be represented with any desirable small error by a non-recursive, or direct, form, where the relevant input past is restricted to the so-called system's memory span [88]:

$$y[n] = f_D(x[n], x[n-1], x[n-2], \dots, x[n-Q]) \tag{5-27}$$

Equation 5-27 is derived from 5-26 with time sampling (at finite time instants nT_s) and this nonlinear extension of the finite impulse response (FIR) digital filters (nonlinear FIR) is again the general form to which a direct behavioral model should obey.

5.6.1 Volterra series

If the Taylor expansion is applied to the equation (5-27), the resulting description is called Volterra series:

$$\begin{aligned} y[n] = f_D(x[n], x[n-1], x[n-2], \dots, x[n-Q]) = \\ \sum_{q=0}^{Q} a_1(q)x[n-q] \\ + \sum_{q_1=0}^{Q}\sum_{q_2=0}^{Q} a_2(q_1, q_2).x[n-q_1]x[n-q_2] + \cdots \\ + \sum_{q_1=0}^{Q} \dots \sum_{q_N=0}^{Q} a_N(q_1, q_2, \dots, q_N).x[n-q_1]x[n-q_2] \dots x[n-q_N] \end{aligned} \tag{5-28}$$

Note that the model looks like a power series model. However, each term in the Volterra series model is a Q-fold convolution (and not a $q'th$ power) of the input signal with a N-fold impulse response kernel $a_N(q_1, q_2, \dots, q_N)$. A low-pass equivalent version of the model can be derived but it is exceedingly complex. Models based on Volterra series can model almost any nonlinear system, but their complexity increases quickly (exponentially in some cases) with memory and model order, making them difficult to implement [88] especially when we are dealing with high degrees of nonlinearity, such as delays, it is nearly impossible to extract the required number of the kernel. Moreover it is not possible to separate different types of input signal, such as dither.

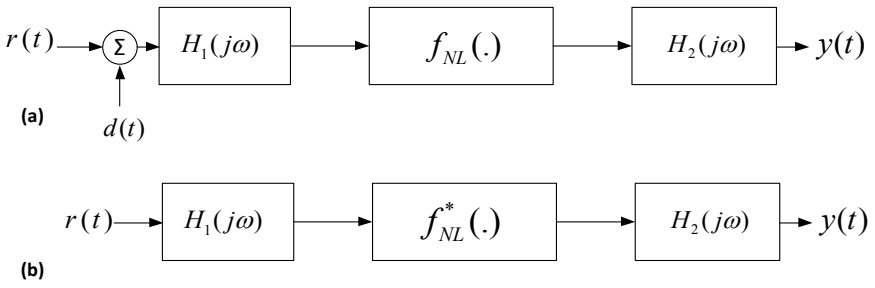


Fig. 5-12 (a): WH model with dithering; (b): Equivalent nonlinearity in WH model, resulting from dithering of f_{NL} and $d(t) * h1(t)$.

5.6.2 Wiener-Hammerstein models

Wiener–Hammerstein (WH) offers more parsimonious representations of many nonlinear systems [74]. These models contain a memory-less nonlinearity cascaded between two linear FIR filters, as shown in Fig.5- 11-a. This model is capable of representing nonlinearities with short memory effects. WH systems can be identified by examining responses to a series of

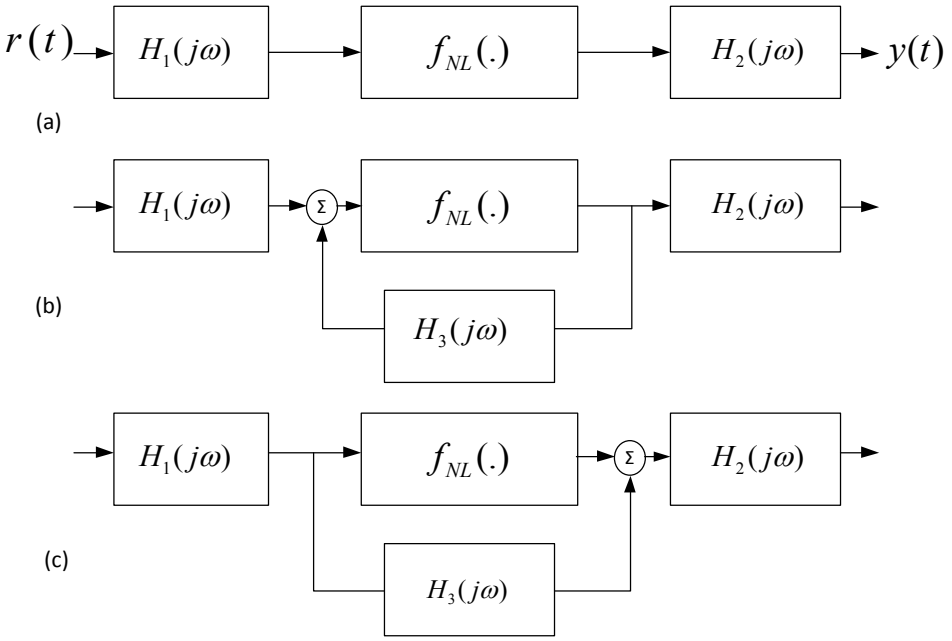


Fig.5-11: WH model is a memory-less nonlinearity, sandwiched between two linear filters. (a): ordinary model; (b): feedback; (c): feed-forward.

single and two-tone excitations in the log-frequency domain [74].

A richer class of systems can be modeled with the addition of a feedback or feed-forward path to the WH system (see Fig. 5-11-b,c). Assuming that the $f_{NL}(.)$ function is an invertible one, the systems of Fig. 5-11-b,c can be inverse of each other [75], [74], which means that replacing the blocks of Fig. 5-11-b by its inverse blocks and change the input-output positions, the system should have the same transfer function.

In the ordinary WH model, the coefficients of filter H_1 are nonlinearly coupled at the output. Assuming that $h_1[n]$ is an input FIR filter, then the sampled time output will be:

$$y[n]=\sum_{l_1=0}^{N_2} f_{NL}\left(\sum_{l_2=0}^{N_2} h_1(n-l_2-l_1)r[l_1]\right) h_2(n-l_2) \tag{5-29}$$

and the extraction process is finding h_1 and h_2 coefficients. This process is very complicated. Briefly said, it is based on swept power and frequency two tone excitation of the nonlinear block and fitting of the third order intermodulation [74].

The parasitic VMCD model presented in chapter 4, can be thought of two single tap (RC) filters, before and after the saturation function, and thus is a WH memory model. For very wide band input signals, the narrowband assumption of chapter 4 is not valid and a full extraction procedure of the WH model for CDA should be undertaken. The advantage of the WH model for dithering is that dither and signal are separately filtered and applied to the CDA and thus again the equivalent nonlinearity concept can be utilized for WH parameter extraction, as illustrated in Fig. 5-12-a,b. The effective dither is applied to a memory-less nonlinearity after passing the input FIR filter.

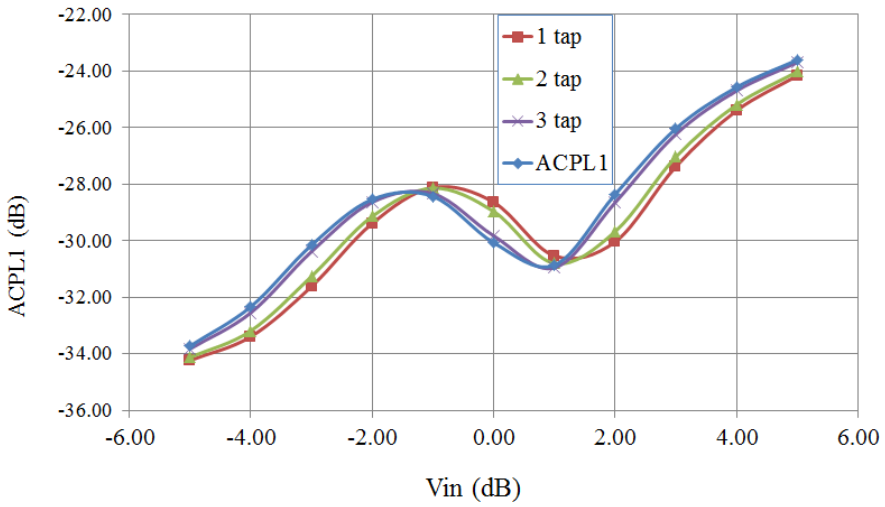


Fig.5-13: adjacent lower channel power, for two carrier 802.11g at 200MHz, for three WH model orders, versus real value of ACPR. The frequency offset is 20 MHz for ACPR calculation

For single carrier application in the majority of wireless standards, the switched mode amplifier memory span is negligible and can be modeled with a single tap filter (like a capacitor parasitic), but for wide band switched mode applications (roughly more than 20MHz in CMOS), the difference between the first order WH model and circuit level simulations can be considerable. As an illustration, a WH model up to order 3 is extracted for a CDA with log-frequency method, dithered with a 1GHz signal, the ACPR results for a three 802.11g carriers, around 200MHz frequency. The input spectrum covers the range from 160MHz to 240MHz. The calculated ACPL1 values are plotted in Fig. 5-13 for 1,2 and 3 taps and real device simulation result. In all of them the DFT synthesis method was used to create a 52 carrier multisine for each input signal.

The process of linearity analysis will remain the same in presence of memory effects and the memory will only affect the linear part of the signal architecture in both closed and open loop (forward loop filters are cascaded with the memory filters).

5.7 Conclusion

In this chapter, a generic and systematic, three-step approach was presented for linearity analysis of closed and open loop dithered nonlinearities. The approach is partially based on the describing function concept and orthogonalizes the output auto-correlation function using Hermite polynomials. The approach is applicable to a general class of real and complex Gaussian random signals and is insightful towards the nature of the nonlinearity of these systems. The memory effect was also introduced as a second order issue, which will show up for wideband applications of the dithered CDA. The method is applicable to autonomous self-oscillating power amplifiers as well as HFD and LFD.

Chapter 6

Spurious analysis

Amplification of a modulated signal in the presence of a large dither in a nonlinear medium such as switch mode power amplifiers facilitates linear performance of the transmitter since most of the nonlinearity is experienced by the dither signal. Therefore, the potential for a promising compromise between linearity and efficiency in these structures is especially attractive for RF power amplifier designers.

Fig. 6-1 shows the two kinds of nonlinearities. The distortion analysis presented in chapter 5 was meant to analyze the first kind of distortion, which was associated to the equivalent nonli-

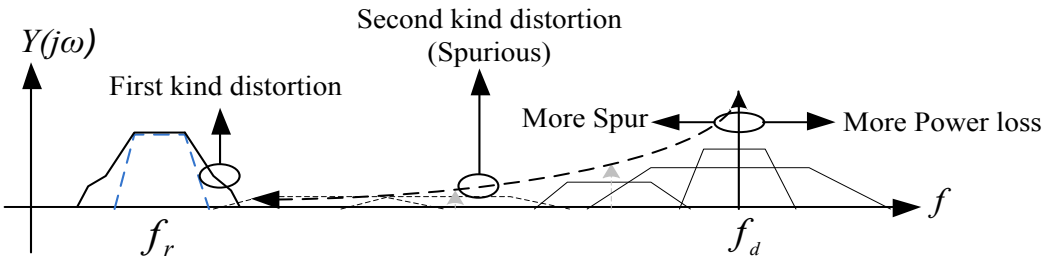


Fig.6-1: The illustration of first and second kind of distortion, or spurious, the second kind will be characterized in this chapter.

nearity. The results of chapter 5 are valid if and only if the spurious amplitude in the band of interest is negligible, compared to the first kind of distortion. The frequency f_d may be below or above f_r respectively for low or high dithering system. In a case of high frequency dithering reducing f_d will reduce the input signal bandwidth, while in both cases reducing f_d is always favored for good efficiency performance, due to the reduction of parasitic reactive power loss.

For high frequency dither, the switching frequency will be close to f_r while for the case when $f_d < f_r$, the switching frequency will be close to f_r. In both HFD and LFD cases, the switching frequency will be proportional to f_d.

In HFD case, reducing f_d will make the spurious components penetrate to the band of interest and interfere with the in-band and thus increase the distortion, while for LFD, reducing f_d will reduce the available input signal linear bandwidth, while in both cases reducing f_d is always favored for good efficiency performance; this will be explained in detail in the following sections.

This chapter, based on a novel method inspired by a quasi-Frobenius equation, will show that *unlike the prevailing perception in the literature that lower dithering frequency should result in higher distortion, there are sweet spots wherein the spurious components are negligible in the signal bandwidth.*

A novel method is proposed to quantify this effect for generic signals based on combinatorial optimization. Frobenius-like equations are written for extracted multisine representation of the input stimuli along with the dither signal. It will be shown that in-band distortion can be minimized by optimizing the first order norm of the cross modulation.

An algorithm is developed to optimize the dither frequency in order to obtain minimal uncorrelated distortion. An optimum search method based on linear programming optimization is proposed to find the optimum switching frequency. Finally, theoretical findings are verified by measured results of a prototype design.

6.1 Existing analysis methods and problems

As mentioned in chapter 2, based on Fourier series expansion of the output signal or the dithered relay (assuming it is quasi-periodic with switching frequency quasi period), we can expand the output:

$$y(t) = f_{NL}\big(A\cos(2\pi f_d t) + r(t)\big)$$

$$= g_0(r,A) + \sum_{m=1}^{\infty} g_m(r,A)\,.\cos(2\pi.m.f_d t + \varphi_i), \qquad \text{(6-1-a)}$$

where f_{NL} is the nonlinear voltage-voltage transfer of the amplifier, g_0 indicates the linearized term of the output signal, which relates the output duty cycle to input value, and other g_m terms represent the spurious side bands of the switching frequency and its harmonics. For a mono-polar width modulated pulse train, with instantaneous duty cycle $\alpha(t)$ and instantaneous phase shift $\varphi(t)$, Raab [79] has expanded the two dimensional Fourier series of equation (6-1-b) as follows:

$$y(t) = \alpha(t) + \frac{2}{\pi}\sum_{m=1}^{\infty}\left[\frac{(-1)^m}{2m}\sin\big(2m\pi\alpha(t)\big)\cos\big(2m\omega_s.t + \varphi(t)\big) + \frac{(-1)^{m+1}}{2m-1}\sin\big((2m-1)\pi\alpha(t)\big)\cos\big((2m-1)\omega_s.t + \varphi(t)\big)\right] \quad \text{(6-1-b)}$$

where ω_s is the instantaneous switching frequency, which is a function of the ratio between the signal and dither amplitudes. When we have a general random signal, which modulates the pulse train, all of the parameters α, ω_s and φ will be a function of time.

When a random signal modulates the width and phase of the carrier, each of the three components of α, ω_s and φ can be represented in a time variable Fourier series, depending on the input multi-sine. Moreover frequency ω_s would be modulated in time for a dithered system and will depend on the frequencies f_d and f_r (which may be time varying), as well as $r(t)$ or instantaneous signal amplitude. So it is not feasible to find a general formula in closed form to predict the spurious side-band amplitudes, for any kind of input signal, but from equations 1-a,b, the following conclusions can be drawn:

1. The spurious phase of the modulated signal side-bands around the switching carrier has a random phase and a uniformly decreasing amplitude ($\propto 1/2m$) and
2. The spurious components for a generic random signal, modulated around higher order switching carriers, can be added to the first spurious harmonic (the two terms in the summation of 1-b), depending on the frequency components of $\alpha(t)$ and $\varphi(t)$.
3. Therefore, it is expected that the trend of variation of the spurious tail around f_d, depend on f_d, and there is no analytic way to characterize that for a generic modulated signal.
4. Finding the dithering frequency points, in which the spurious power in the band of interested is negligible, is of importance; hence, we are only interested in the dithering frequencies which minimize the spurious power.

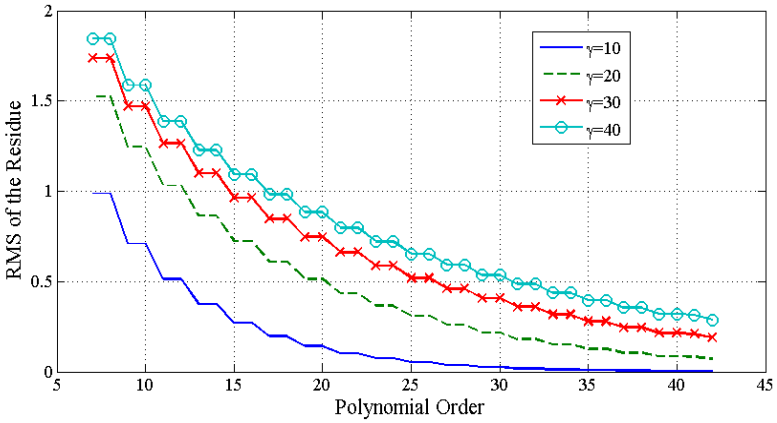


Fig. 6-2: Fitting polynomial order error versus polynomial order N, for different slope gains, The error increases with increasing the slope gain.

There are a few analytical models proposed so far, for spurious characterization, that are only valid for a single tone input signal. Among them are [10] and [79]. They try to put absolute limits on the minimum possible switching frequency, for error free high frequency or RFPWM modulation. A new work published by Garcia et. al [Fundamental error free], discusses the condition for a normal PWM, for error free transmission, but it still doesn't characterize the behavior of the spurious level versus the switching frequency.

It goes without saying that using a circuit simulator to characterize the behavior of the spurious variations versus dithering frequency is next to impossible. This is because in dealing with such hard nonlinearities such as a CDA even extremely high orders of nonlinearity can remarkably contribute in overall distortion. Thus truncating the number of mixing orders at relatively small numbers will result in huge loss of accuracy. Fig. 6-2 shows the relative error in polynomial characterization of a hyperbolic relay CDA model ($y = \tanh(\gamma x)$), for different values of slope gain γ, versus the order. It is observed that for values of γ like '30', even the distortion of order '43' is not enough to accurately model the distortion.

This extremely high mixing order, required for either the Harmonic Balance or Circuit Envelope method, and the FFT size required for the transient method, will immediately render the simulator out of memory. Therefore, an analytical approach is essential to theorize this effect and systematically produce the relevant set of conditions and algorithms to fine-tune the sampling frequency for optimum linearity, especially when relatively lower sampling frequencies (e.g. in SOPA or naturally sampled PWM or LFD) are employed. This chapter, based on [49], for the first time, adds to the previous sets of conditions by setting a condition on the dithering frequency for minimum distortion.

6.2 Proposed optimization approach

The original problem of spurious characterization is inherently a nonlinear problem. If a shortcut could be found to avoid the nonlinearities, like linear algebra methods, in order to find the

pattern of spurious power behavior in terms of the dithering frequency, it saves a lot of time and memory.

The tuning mechanism introduced in this work will optimize the dithering frequency in order to minimize the distortion caused by the second term of (6-1-a,b). The proposed solution employs a somewhat generalized version of the Frobenius or coin problem [41] to minimize the in band intermodulation components of a set of sinusoidal tones consisting of a multisine representation of the input stimuli and the switching component by optimizing the frequency of the switching component.

The main difference between this situation and the general linear algebra problem formulation is that the coefficients *are not necessarily non-negative*. As the first step the input signal should be represented by multisine. There are several approaches to obtain the multisine components. One of them is the DFT method which is also used in this work.

Naming the input multisine frequencies f_1 to f_N, the cross modulation frequency (f_{CMD}) of different orders of the sampling frequency and the input frequencies (multi-sines) can be described as:

$$f_{CMD} = \sum_{i=1}^{N} m_i f_i + m_d f_d;\ f_r - \frac{\Delta f}{2} < f_i < f_r + \frac{\Delta f}{2} \tag{6-2-a}$$

where Δf is the desired bandwidth, and coefficients m_i and m_d represent the order of individual multisine and dither harmonics at the output of the nonlinearity. We are looking for the m_i's that satisfy two inequalities as follows:

$$f_L \leq f_{CMD} \leq f_H \tag{6-2-b}$$

As mentioned before, the difference between this problem and original linear algebra problem is that the m_i's can also get negative values as well. The main goal is *to determine the proper dithering frequency so that the minimum orders of cross modulation components landing in the desired frequency band are as high as possible, hence minimizing their amplitude.*

The intuitive reason behind this assumption is the nature of Fourier transform of 6-2-a,b series in which the higher orders of nonlinearity rapidly decrease in value, or in other words, lower orders have higher values and a dominant effect on the overall distortion. Equation (6-2-b) can be written for any kind of nonlinearity and the only parameter that is affected is the maximum values allowed for the coefficients m_i in (6-2-a).

In order to minimize the intermodulation components that fall in the desired signal band, L_1 norm function of the coefficients is defined as follows

$$\|CMD\|_1 = \sum_{i=1}^{N} |m_i| + |m_d|, \qquad m_d \neq 0 \tag{6-3}$$

Optimizing the function of (6-3) through changing the dither frequency will result in minimum distortion. Besides, the trend of variations of the minimum norm satisfying (6-2-b) will give a picture of distortion variations versus the switching frequency.

6.3 Optimization technique for multi-sine

The number of required tones mimicking the behavior of a digitally modulated signal grows large and a systematic method is needed to optimize the norm. Otherwise, the number of arrangements would be so enormous that it would make it impossible to find an optimum solution. For instance, for 32-sines, considering maximum order of 15 for each input tone, the number of states that should be investigated directly is of the order of 10^{46} (i.e. having 31 components, including negative frequencies and dc, makes the number of possible states 32^{31}).

In fact, this is a problem of Mixed Integer Linear Programming (MILP) and the variables are the coefficients. Conversion of the integers to binary format, makes it possible to employ the well-known Branch and Bound algorithm to find the optimum [8]. Available binary integer programming routines in MATLAB can be used with some modifications.

The difference between the classical MILP method and this problem is that the coefficients are assumed to be positive. Therefore in order to be able to use the conventional techniques, positive and negative frequencies should be both considered, which doubles the number of the unknown coefficients. The utilized coefficient vector is defined as follows:

$$M = \left[m_{1p}, m_{2p} \dots, m_{Np}, m_{dp},\ m_{1n}, m_{2n} \dots, m_{1n}, m_{2n}, \dots, m_{Nn},\ m_{dn}\right]^T \tag{6-4}$$

while all of the coefficients will be represented in Q bit binary form (varying from 0 to $2^Q - 1$), with p, n denoting positive and negative frequency coefficients. The frequency vector is defined as follows:

$$F_1 = [f_1, 2f_1, \dots, 2^{Q-1}f_1, f_2, 2f_2 \dots, 2^{Q-1}f_2, f_N, 2f_N, \dots, 2^{Q-1}f_N, f_d, 2f_d, \dots 2^{Q-1}f_d] \tag{6-5-a}$$

$$F = [F_1, -F1]^T \tag{6-5-b}$$

$$f_{CMD} = M^T F \tag{6-5-c}$$

where F_1 includes positive frequencies and F is the entire band frequency grid; the matrix equation 6-5-c denotes all possible intermodulation frequencies. The cross modulation norm objective function is rewritten as:

$$\|CMD\|_1 = \sum_{i,d} \left| m_{ip} + m_{in} \right| \tag{6-6}$$

After formulation of 6-4 to 6-6, the number of unknowns is $2(N+1)Q$. The branch and bound technique can easily be used to maximize (6-6), to find the dominant distortion order, for each switching frequency [41], [27].

6.3.1 Discussion

Optimization of equation (6-6) will result in a set of optimum points and it is expected that the trend of variation of the cross modulation error function resembles the variation of the spurious power in the bandwidth of interest. Four issues should be considered:

1. The optimum points for the spurious (minimum spur power) should coincide with maximum norm values of $\|CMD\|_1$ and vice versa, i.e. the maximum spurious powers should correspond to minimum $\|CMD\|_1$ points.
2. The $\|CMD\|_1$ value does not give any information regarding the absolute value of the spurious power. It is just a linear means to characterize the spurious behavior versus dithering frequency, and find the optimum points.
3. The place of the optimum points is constant with respect to frequency. Their absolute spurious power is a function of the input amplitude while the trend of variation of the spurious power versus frequency doesn't depend on the amplitude. The exact value of the spurious will depend on the amplifier and frequency, and measurement should be done in order to find that.
4. The process of optimization of $\|CMD\|_1$ *does not depend on the process technology, temperature or even the amplifier*, as long as it is assumed to be a switched mode amplifier.

The flowchart of Fig. 6-3 sums up the steps required to tackle the problem of minimization of

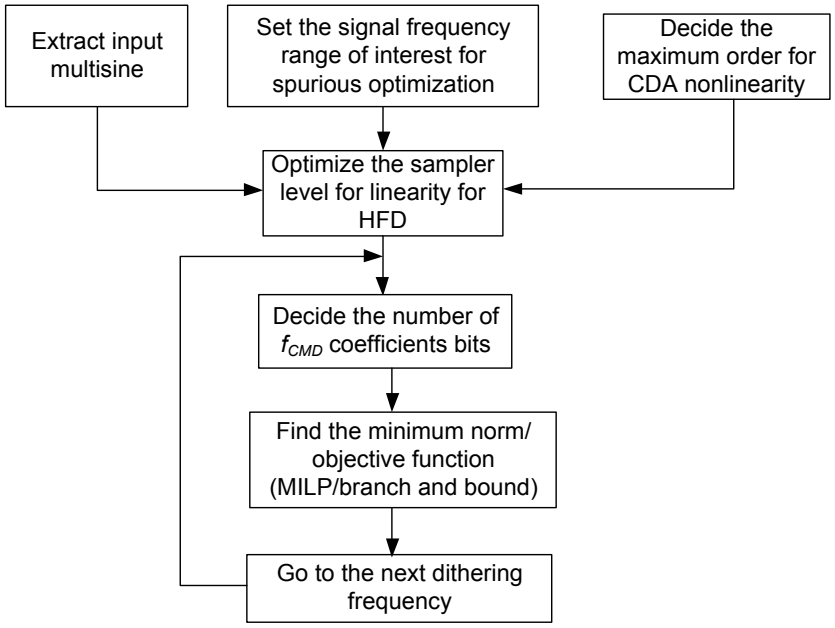


Fig.6- 3: Flowchart of the analysis approach

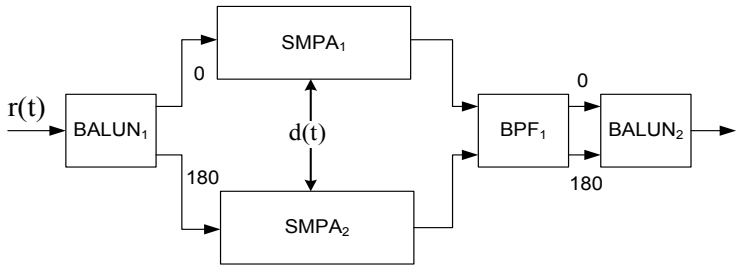


Fig. 6-4: Common mode dithering at the input, with a relaxed filter order at the output

the first order cross modulation norm.

6.3.2 Common mode dithering topology

For the filter-less power combining scheme, introduced in 4.1.4, and shown in Fig. 6-4, the dither component and its cross modulation with even input orders would be in-phase at the output. Therefore, the maxima of the equation (8-a) would be meaningless in many points. One way to avoid unwanted solutions to the equation is using a modified cross modulation norm, excluding the cross modulation of the odd input products and even dither products.

If all of the existing intermodulations are of odd order, then the new CMD norm should be as follows (setting $m_i = 2K_i + 1$ and $m_d = 2K_d$ in equation 6-3):

$$\|CMD\|_1 = \sum_{i=1}^{N} |2K_i + 1| + |2 * K_d|$$

and the maximum of this quantity in a given range will correspond to the intended minimum of the distortion.

6.3.3 Harmonic multi-tone dither effects

As explained in chapter 2, the dither signal can be multi-harmonic. For example a saw-tooth waveform can be used as dither signal, and having a uniform value pdf, it generates a linear equivalent nonlinearity function.

Unfortunately there is a trade-off between the number of higher order dither harmonics and the spurious level (Fig. 2-6, section 2.3.2). The effect is the reduction in the norm, or equivalently increased spurious amplitude.

In case of having an M harmonic tone dither signal, applied to an ordinary CDA, the following cross modulation component will exist at the output (m_d converted to $i.m_{di}$) :

$$f_{CMD} = \sum_{i=1}^{N} |m_i f_i| + \sum_{i=1}^{M} |i.m_{di} f_d|, \qquad m_{di} \neq 0$$

And the corresponding norm will be defined as:

$$\|CMD\|_1 = \sum_{i=1}^{N} |m_i| + \sum_{i=1}^{M} |m_{di}|, \qquad m_{di} \neq 0$$

Because of $M-1$ more degrees of freedom, this new function will have lower local minima than in the case of single-tone dithering.

6.4 Case studies and validations

As mentioned before, Harmonic balance or other simulation techniques are inefficient in order to see the spurious behavior with a real digital modulation, consisting of many sinusoids. Therefore, a simple two tone test signal is generated and the result of HB simulation, with "enough" number of harmonics and mixing order, is compared to the maximum CMD norm order achieved from LP. First a two tone signal at 200 MHz is generated and applied to a CMOS CDA, in Cadence environment. The tone spacing is chosen to be 4 MHz, and the output distortion power to the 9'th order intermodulation (at 202MHz +28MHz=230Mz).

The output spectral densities for the dithering frequencies of 1.3 and 1.5 GHz are plotted in Fig. 6-5-a,b in order to illustrate the sensitivity of the spurious level on the f_d, as the two frequencies are relatively close to each other, but the spurious response in the former is far worse than the latter. The results of IMD power and norms are plotted in Fig. 6-5-c,d versus the dithering frequency swept from 10 MHz to 2GHz, for single mode and common mode dithering (Fig. 6-5-c). As expected, many of the spurious sweet spots are widened for common mode compared to the single mode.

In Agilent ADS™, the HB simulator was used with 11 harmonics for each frequency (including dither) and mixing order of 12. The HB simulation time largely depends on the number of tones and in many cases it doesn't converge for more than 4 input tones. In the MILP routine implemented in MATLAB, 9 bits was used for each coefficient and the convergence doesn't have any problem for very large number of tones.

It should be noted that this simulation is *not* representative for a general modulation, and the data and the sweet spots achieved are not the same for a digitally modulated input signal. For a general modulation, the practical measurements of spurious distortion versus dithering frequency will be presented in chapters 7 and 8 for HFD and LFD, for both ACPR and in band distortion (NPR) of a complex digital modulations.

6.5 Applications in linearity-efficiency trade-off

Referring to Fig. 6-5-c,d it is understood that the sweet spots and undesirable points exist in the frequency grid, which can be very close to the intended signal bandwidth or below that, in

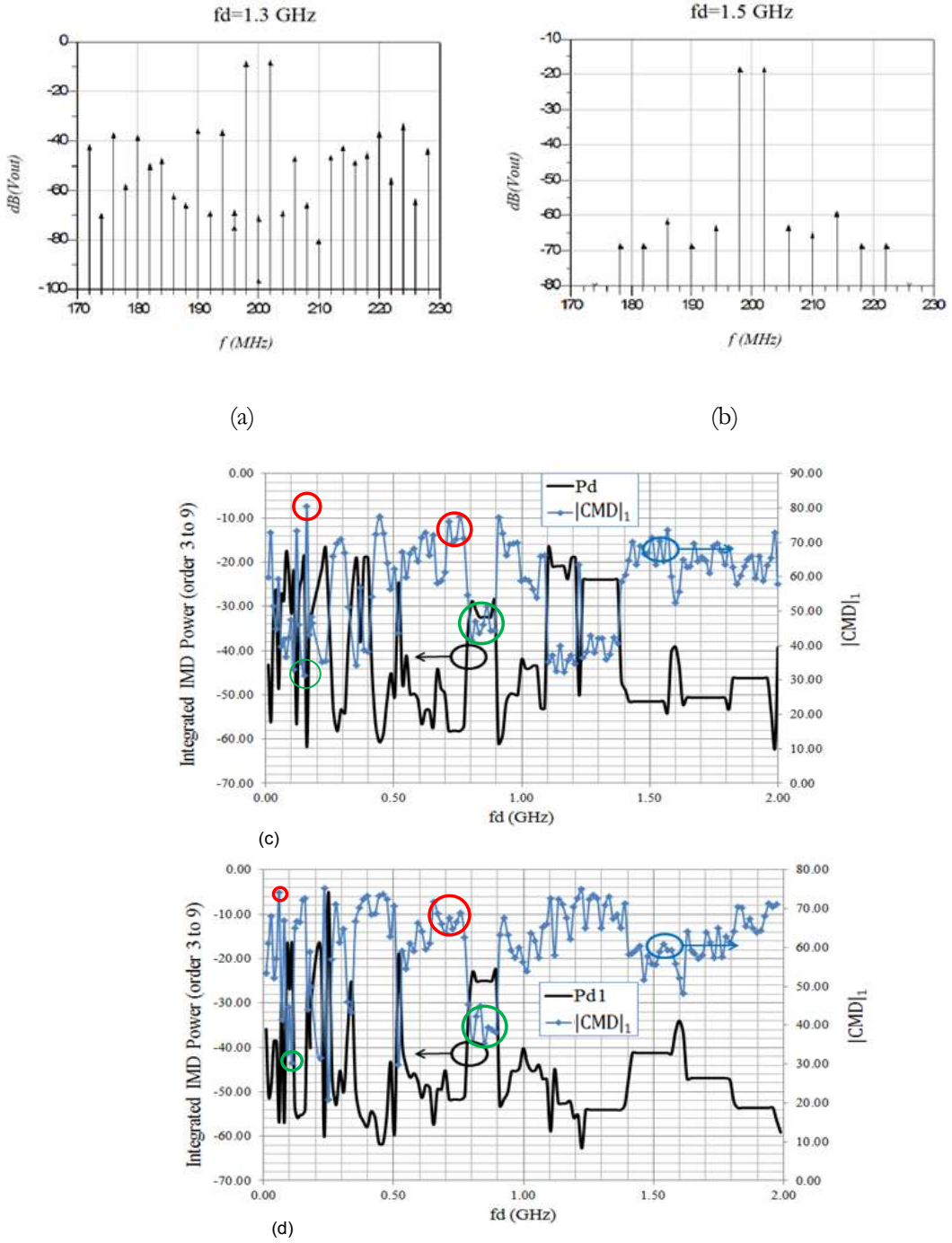


Fig. 6-5: (a),(b): output spectrum for two tone input signal at 198 and 202 MHz, for dither frequency at 1.3 and 1.5 GHz respectively; (c): Total IMD power (order 3 to 9) and CMD 1 norm versus f_d; (d): the same for Common mode dithering topology; all of the maximums of CMD_1 coincide with the minimums of total IMD power and vice versa for minima of CMD and maxima of IMD power. Two sample sweet spots and nearby undesired points are marked by red and green circles are specified.

which the first order cross modulation norm is high enough, or equivalently the spurious level is low enough. As mentioned in the introduction, these points are favored in terms of linearity. Two sample sweet spots and their close by undesired point are marked on Fig. 6-5-c,d, by red color and green colors respectively.

Three issues should be considered here:

1. For a given bandwidth, the sweet spots or the points with high norm, that are low 'enough' in frequency, are always favored, in design of efficient power amplifiers. The exact spurious level should always be determined with simulation/measurement.
2. The sweet spots can have adjacent points with very undesirable linearity. Therefore enough care should be taken to place the dithering frequency, exactly in the point that it should be located. Two examples are given based on the figures:

    a. Fig. 6-5-a,b show two close-by spurious results, for two frequencies of HFD: 1.3 and 1.5 GHz, the former can't be used for linearity, but is favored for efficiency, compared to the latter. It has even a better spurious performance than higher dithering frequencies, like 2GHz.

    b. For LFD, 170MHz, compared to the very close-by frequency of 160 MHz, give very different spurious results; therefore the first should be chosen (30dB difference in spurious power). The optimum is as good as the points above 1GHz, but with much higher power efficiency.

3. Frequency stability of the dithering becomes very important, when we tune the dithering frequency in a very narrow sweet spot, like that marked on Fig. 6-5-c,d for LFD. A frequency control scheme should be utilized in that case.

The general mathematical approach, based on linear algebra can characterize the spurious level versus the dithering frequency, for any kind of signal, for LFD and HFD, and also predict the frequency sensitivity of the optimal points. The selection process of the optimum dithering points will depend on the efficiency required, as well as the intended signal bandwidth.

6.6 Conclusion

A generic, fast and insightful method to predict and optimize the spurious components behavior of a dithered nonlinear block, versus dithering frequency, was presented. The proposed method is based on the solution of a set of linear in-equalities and linear algebra techniques were used to optimize a linear error function, called the cross modulation norm. Branch and bound techniques are viable to find the optimum of this error function for each dithering frequency.

The approach *does not depend on the process technology and temperature* and does not give the exact spurious level, and can be used to find a trade-off between the intended linearity and efficiency, based on the achieved sweet spot locations. All of the important maxima and minima of the distortion metrics coincide with the results of the approach. The approach can be applied

to any kind of input signal represented by multisine and for any kind of periodic switching signal. The approach will also be validated in chapters 7 and 8 for a complex modulated signal in LFD and HFD scenarios.

Chapter 7

High frequency dithering

Based on the analysis introduced in chapter 4 about important dithering parameters, the most important ones are the slope gain and the parasitic capacitances of the device. The former maintains the dithered gain high enough for efficient and high gain operation, while the latter is proportional to the frequency dependent reactive power loss.

Test circuits have been made for HFD verification, based on the architectures and circuit topologies introduced in chapter 4. As mentioned before, the technological requirements are that the device must have high gain, and for high frequency dithering, should have small enough parasitics, to reduce the reactive power loss (CV^2f or Li^2f).

The design methodology, for all of the class-D amplifiers was discussed in chapter 4, for different VMCD and CMCD complementary topologies. In this chapter, the design and realization of a single ended VMCD will be discussed and the simulation and calculation results will be plotted against the achieved results.

Next as an example of the closed loop architecture, a self-oscillating power amplifier, oscillating at 1 GHz limit cycle frequency, have been realized with the same CMOS technology, and again the calculation results based on the analysis methods. In chapter 5, will be compared with and validated through the measurements.

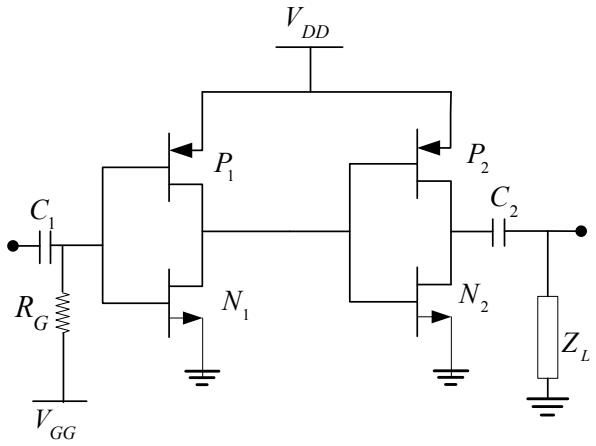


Fig. 7-1: The circuit topology of the realized integrated $VMCD$ in CMOS.

7.1 Open loop VMCD

The goal is to amplify a signal with a carrier frequency of 200 MHz, with a class-D PWM amplifier switching at 1GHz. The open loop single voltage switched class-D topology, selected here to be realized is one of the topologies, discussed in subsection 4..2.2, biased by a high value resistor, and depicted in Fig. 7-1.

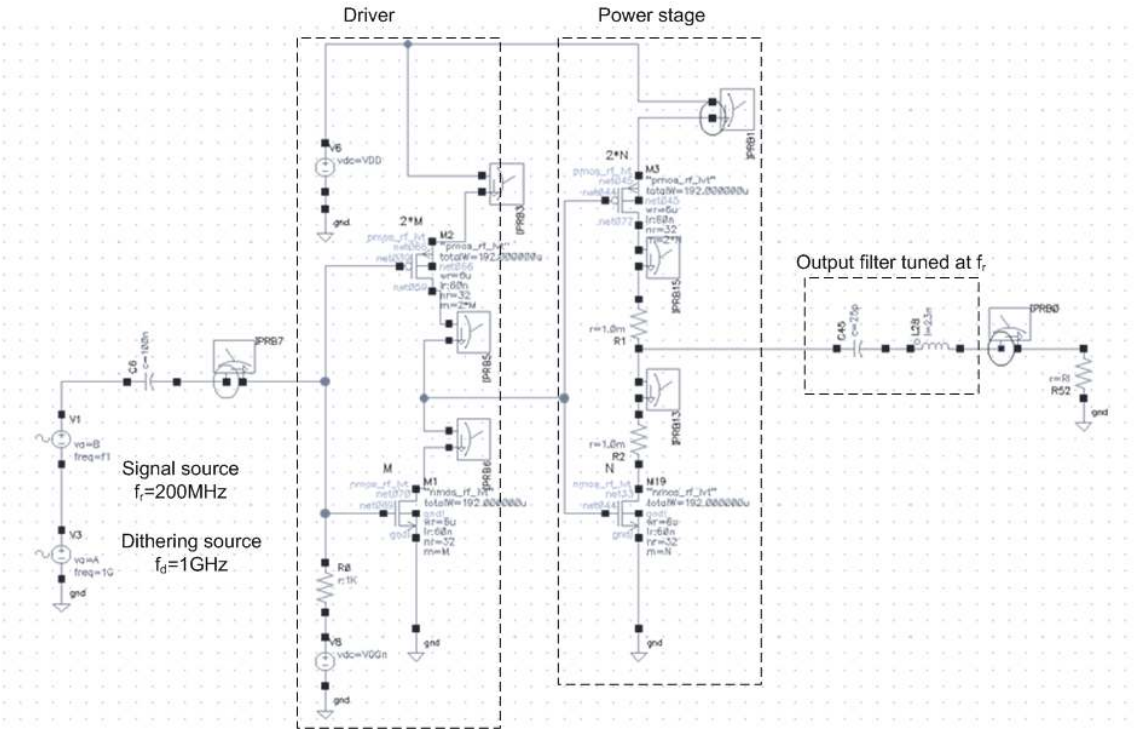
The driver stage P_1, N_1 excites the power stage P_2, N_2, which delivers the required power to the load impedance Z_L. The relationships between the output power, power efficiency and load impedance were described in chapter 4.

7.1.1 Circuit design

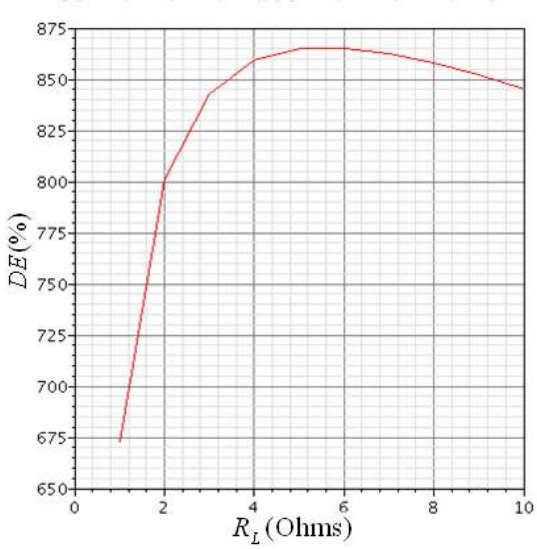
The role of the driver is to increase the slope gain of the amplifier and also reduce the short-circuit power loss, through reduction of the transition time between the on-off switching states. The capacitors C_1 and C_2 are off chip, and the impedance Z_L will be realized with the load tuner. The biasing of the power stage will be adjusted by the output dc voltage of the first one, which will depend on the voltage V_{GG}. The biasing should keep the output of both stages at the quiescent voltage of $V_{DD}/2$. If the exact value is important, then a feedback mechanism should be devised to compensate for deviations of the output bias from $V_{DD}/2$.

The most important issue is to get the required output power with the highest possible power efficiency. The ratio between the PMOS and NMOS transistors is very important for symmetric switching.

Fig. 7-2-a shows the schematic diagram of the designed circuit in Cadence™. Fig. 7- 2-b shows that, as expected, the load impedances for maximum efficiency and maximum power don't



(a)



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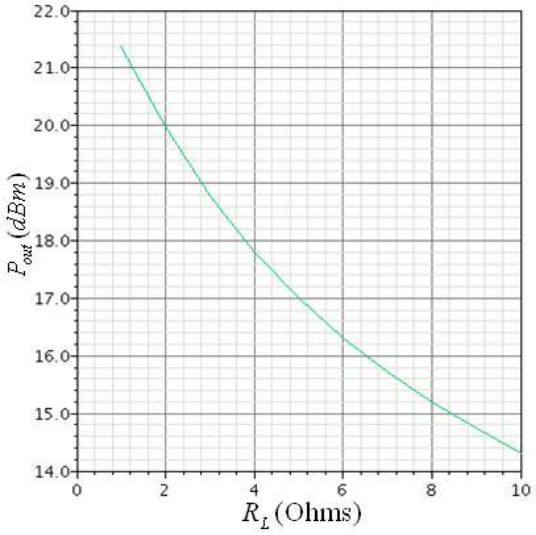


(c)

Fig. 7-2: (a): The schematic diagram of the VMCD in Cadence; (b): drain efficiency times ten versus the output resistance; (c): output power versus load resistance, for CW input at 200 MHz

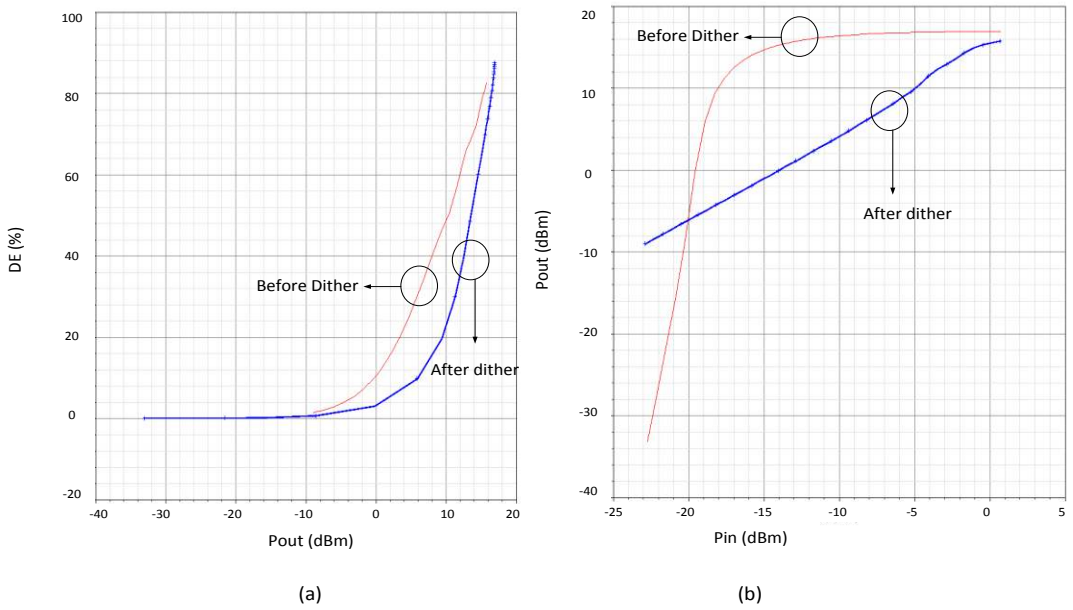


Fig. 7-3: (a): Drain Efficiency of the CMCD, before and after dithering, with a 1 volt sinusoidal dither, applied directly to the gate, and input power swept and (b) AM/AM characteristics, before and after dithering from -40 dBm to -3 dBm. This figure shows that the efficiency drops by maximally 44 %, while the linearity improves, as expected, after HFD.

coincide. The schematic level simulation shows that for optimum efficiency, the load resistance should be tuned at 5 ohm, delivering 17 dBm output power to the load. For the higher order harmonics the load impedance should be infinity.

The dithering results and its effect on the AM/AM and drain efficiency versus output power are illustrated in Fig. 7- 3 a,b.

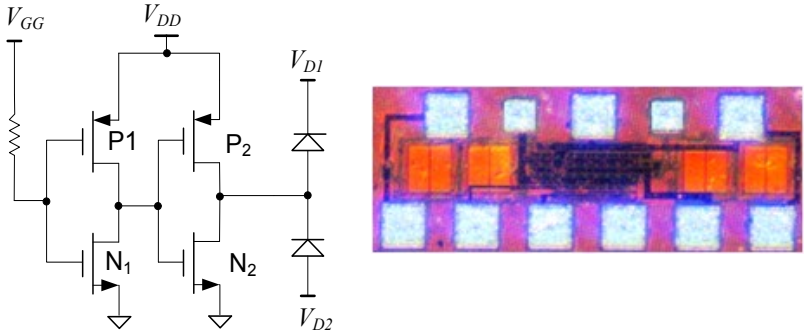


Fig. 7-4: The schematic level and chip photograph of the realized VMCD

According to Fig. 7- 3, the dithering level of 1volt (available dither power of 10 dBm) is enough to extend the linear dynamic range of the VMCD, up to output powers of 15 dBm. Meanwhile, the drain efficiency drops by 44 percent (from 76 percent before dithering, to 32 percent after dithering, because of the previously mentioned capacitive power loss.

7.1.2 Measurement and validation

The CMOS voltage mode class-D amplifier was realized for verification purposes, in 65nm technology. The schematic diagram is shown in Fig. 7-4-a and the IC photograph is shown in 7-5-b. The final stage consists of 10, 20 NMOS-PMOS pairs respectively, providing 20 dBm peak output power to the optimum load at 1 GHz. Each transistor has 6x32um gate width.

A load pull setup (see Fig. 7-5) was utilized to find the optimum load impedance for maximum power/efficiency. Three different measurements were performed on the circuit. First of all, the frequency variations of ACPR versus the dithering frequency; then, after fixing the dither frequency, output signal power Pout vs. Pin; and finally the drain efficiency for two cases of CW signal and low frequency dithered signal.

All of the measurements are presented in Fig. 7-6 (a-c) together with the calculation/simulation results. Fig. 7-6-a shows the linearized AM to AM transfer function, before and after dithering, It is seen that the compression for undithered CDA already has started below -20dBm input power. Fig. 7-6-b illustrates the measured drain efficiency, which shows 7 percent decline in its peak value, compared to CW mode; the degradation of the efficiency compared to the measurement results is due to the contact resistance of the probes. Even a contact resistance in the order of 5 ohm can reduce the efficiency by more than 50 percent. Fig. 7-6-c shows the ACPR versus output power back-off (OPBO). The metrics show that the high frequency dithered PA meets the 3G spectral mask to 1 dB back-off from the output peak power (≈19dBm at optimum load achieved from load-pull measurement).

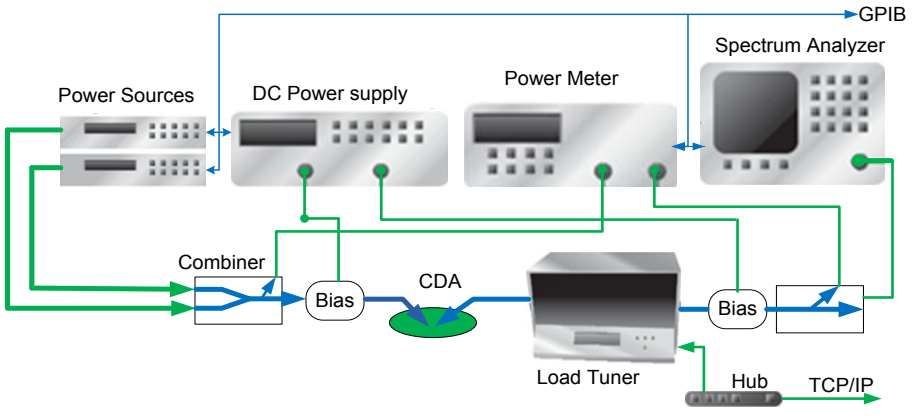
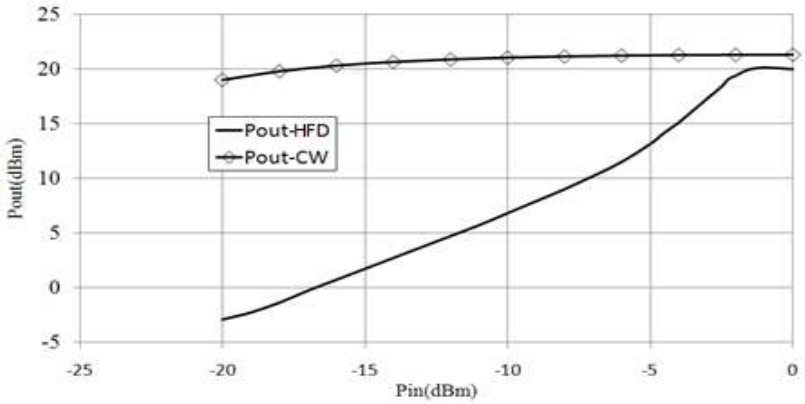
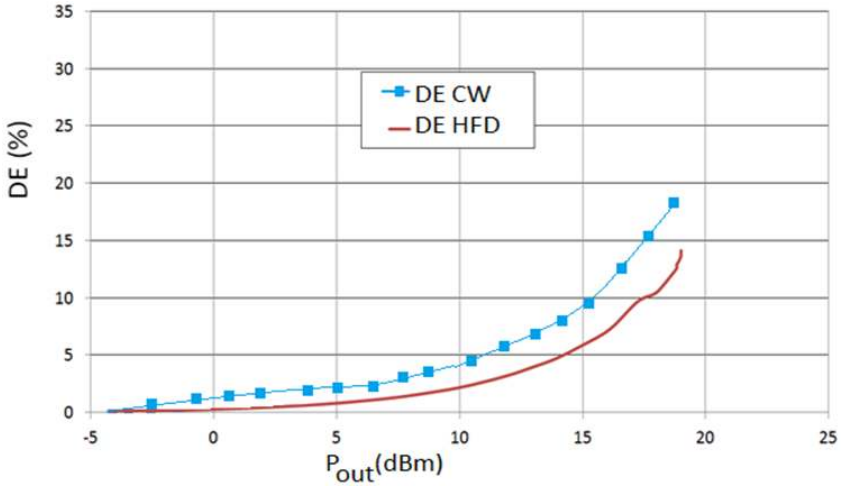


Fig. 7-5: The load-pull setup



(a)



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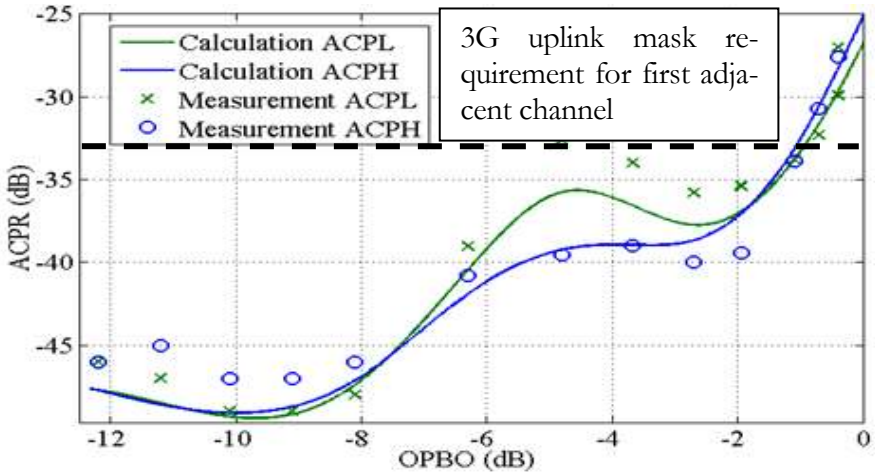


(c)

Fig. 7-6 (a): Measurement results for AM-AM curve before and after dithering; (b): drain efficiency before and after HFD, versus the output CW power; (c): ACPR versus the output power back-off

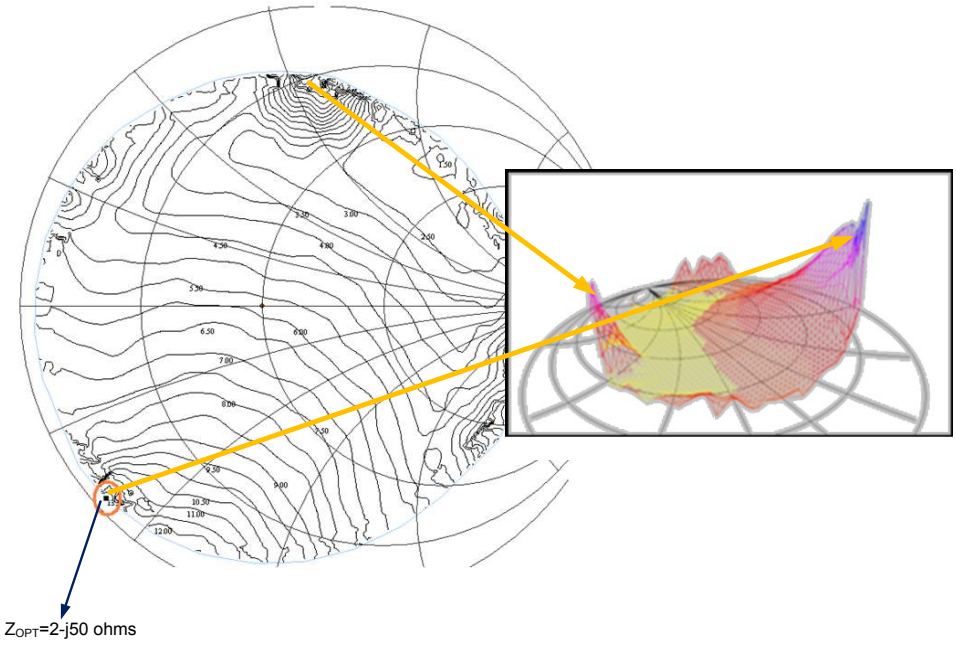


Fig.7-7: The LP constant power counters and optimum impedance (circle), along with the 3D power surface on smith chart.

A load pull setup was arranged and applied to the designed PA. The required load pull was a multi harmonic load pull, providing arbitrary tuning capability, simultaneously in three frequencies. The setup is depicted in Fig. 7-5 and the results are illustrated in Fig. 7-7. So a matching network should transfer the 50 ohm standard termination to the Z_{opt} determined in Fig. 7-7, in the final design.

Figs. 7-8-(a, b, c) illustrate the variations in ACPR for higher and lower adjacent channels, along with the linear norm. The agreement between the measurement, calculation and simulation validates the analysis approach presented in previous sections. It is observed that for dithering frequency bigger than 2GHz, there are less fluctuations in the ACPR level, while those fluctuations increase for lower frequencies. A special set of points, marked by points P_1 and P_2 in Figs. 7-8(a, b, c) show the trend of variations for to close frequency points. P_1 and P_2 correspond to 1.25 and 1.3 GHz, and show a huge difference (at the order of 30 dB) in ACPR level, while the former has a slightly better power efficiency. It should be noted that P_1 is superior to P_2 in terms of efficiency and linearity, and therefore the dithering frequency should be tuned for P_1.

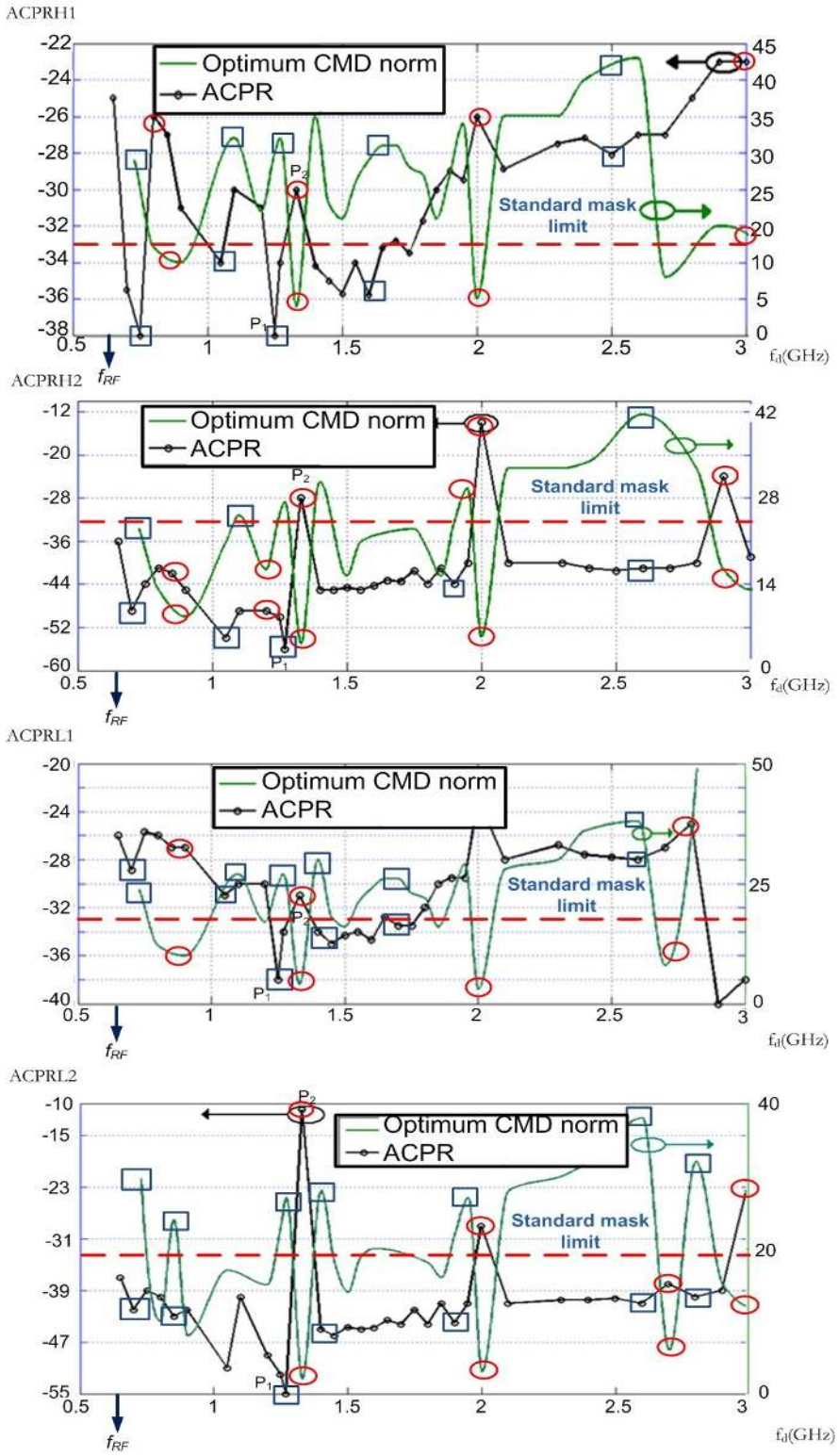


Fig.7-8: ACPR (dB) for adjacent and alternate higher and lower channels of 670 MHz WCDMA, and the optimum CMD norm, versus the switching frequency (in GHz).; the circles are the minima of the norm and squares are the **optimum** norm maxima (low spurious); the trend is that more fluctuations are seen at lower frequencies, for example points P_1 and P_2 according to 1.25 and 1.3 GHz have extremely different spurious performance (P_1 complies to the mask requirement or dashed line and P_2 doesn't), while P_1 has superior efficiency performance because of less reactive power loss.

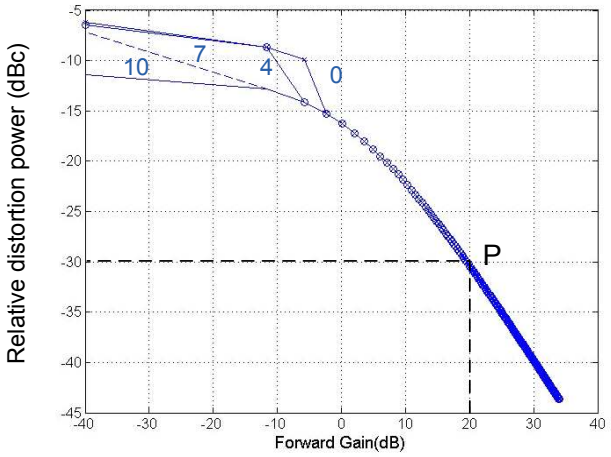


Fig. (7-9) Total distortion power versus forward loop Gain for input CW power levels from 0dBm to 10dBm; the point P was chosen for the total forward gain, at the signal frequency, as the total uncorrelated power is 30 dB below the carrier power.

7.2 Self-oscillating class-D

A self-oscillating class-D amplifier uses a high frequency limit cycle as the dither signal. Moreover, utilization of negative feedback enhances the linearity. This structure is sometimes called asynchronous sigma delta, due to resemblance to a sigma delta modulator and the absence of an external clock signal. The complete analysis of a single SOPA (ASDM) loop was presented in chapter 5, and it was mentioned that the main difference between the SOPA and an ordinary (forced) dithering is the independence of the dithering level on the signal amplitude. The term "order" of the loop, usually refers to the order of the forward filter.

In order to validate that theory, a zero order self-oscillating loop, with a second order RC filter in the feedback is implemented in 65nm CMOS technology. The important loop parameters are the phase shift of the CDA and the feedback filter. Assuming a 180 degree phase shift for the input subtraction, the following equation has to be satisfied in the intended limit cycle frequency of 1GHz (see Fig. 7-11-a):

$$angle\big(H_2(j\omega_{LC})\big) + angle\big(G_v(j\omega_{LC})\big) \cong -2 * tan^{-1}(RC\omega_{LC}) + angle\big(G_v(j\omega_{LC})\big) = 180^0$$

in which G_v is the complex two tone voltage gain of the CDA, at the limit cycle frequency, obtained from simulation or measurement.

7.2.1 Topology design

There are two major requirements related to the design of the system gain budget. First is enough limit cycle frequency loop gain to satisfy the Barkhausen criterion at the desired limit cycle frequency and do not meet the round trip phase of zero at any other frequency. The second condition deals with the required *loop gain for the RF frequency*. The total uncorrelated output in-band distortion power of order '*n*' at the output of a limit cycle loop is expressed based on equation (5-24-a) in equation (7-1):

$$Y_{u,n}(\omega) = c_n.\sigma_{in}^{2n}\left|\frac{(G_S G_F H_1(j\omega))^n}{(1+G_S G_F H_1(j\omega)H_2(j\omega)N_r(A,\sigma_r))^n(1+G_S G_F H_1(j\omega)H_2(j\omega)N_r(A,\sigma_r))}\right|^2 \qquad (7\text{-}1)$$

in which the second term in denominator shows the feedback effect on uncorrelated part, and the rest is input variance to the power of '*n*' times the corresponding autocorrelation coefficient.

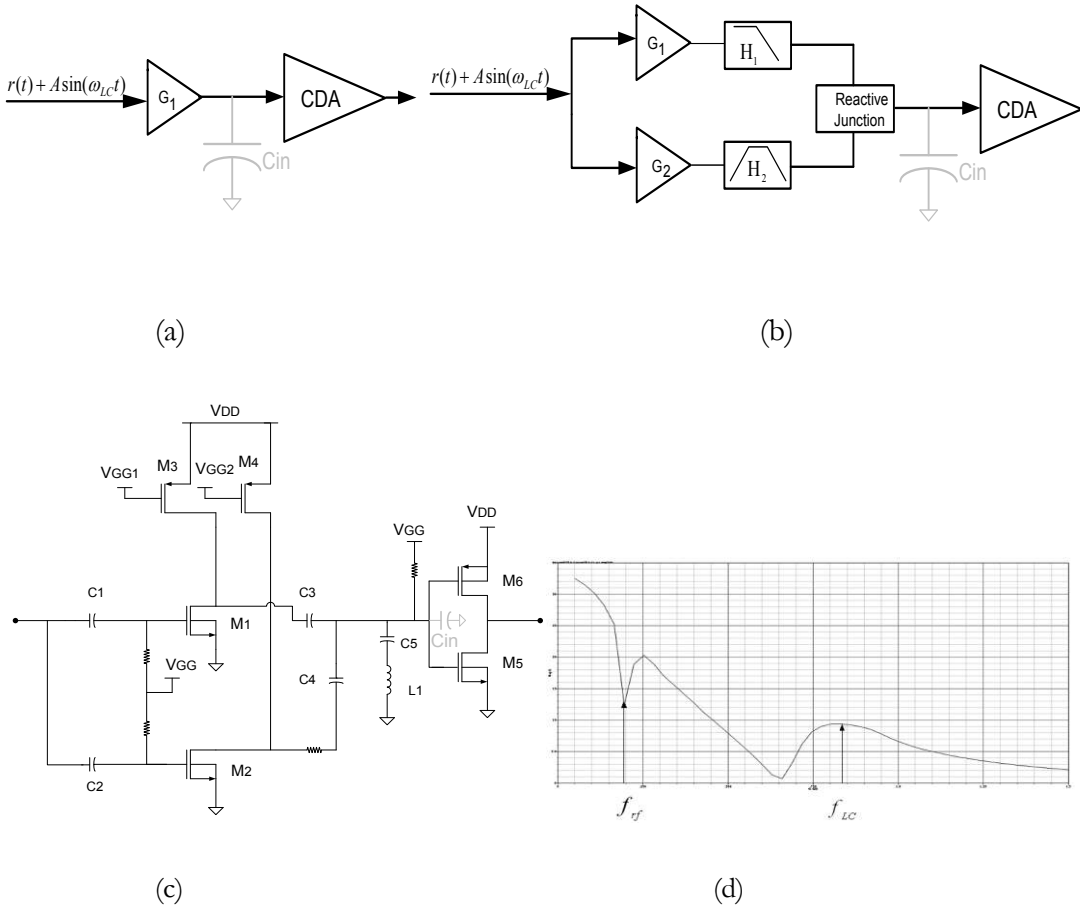
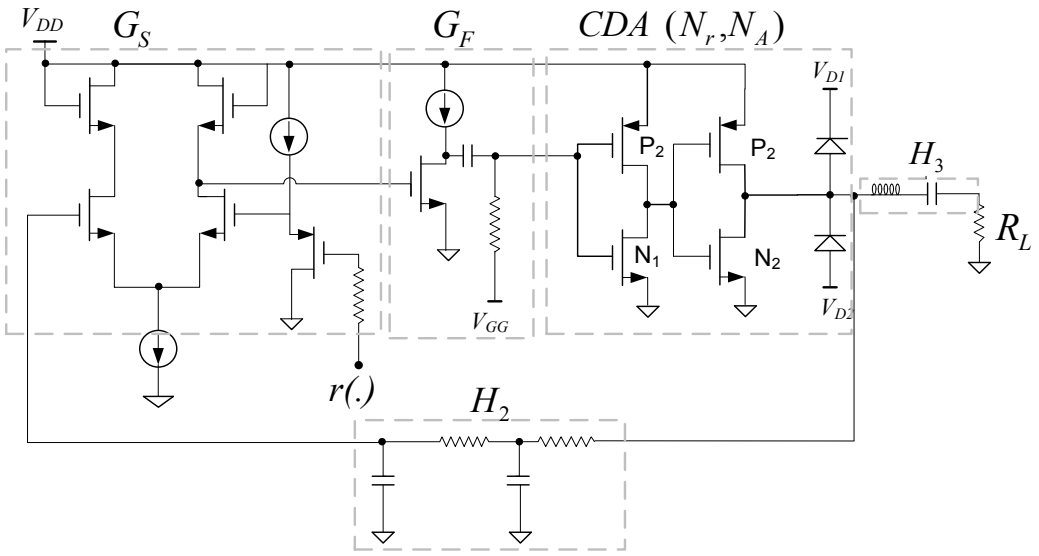
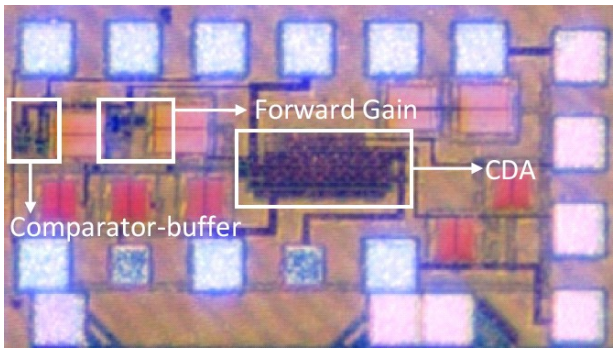


Fig. (7-10): (a): Single amplifier driving the CDA in the forward path; (b) active duplexer, for independent forward limit cycle and RF gain adjustments; (c): a possible circuit realization of (b), where V_{GG1},V_{GG2} are controlling voltages for limit cycle and RF signal gains, as they control the currents of M_1 and M_2; (d): frequency response of the driver of (b), as circuit (c) implemented in CMOS.

where N_r is the switched mode amplifier random input describing function, σ_r and σ_{in} are loop and amplifier input rms values, and c_n is the n'th order distortion coefficient. Equation (7-1) is valid for higher order distortions by changing the input, numerator and denominator exponents according to the distortion order. Fig. (7-9) shows the sharp decrease in the distortion value versus the forward gain for gain values above 0 dB (or 1). According to Fig. 7-9, the point P is a good candidate for a linear design, as the total uncorrelated output distortion is -30 dBc, and the requirement for an uplink 3G signal is -33 dBc for the first adjacent channel ACPR, and 17 percent for EVM [85].



(a)



(b)

Fig. 7-11: (a) Schematic diagram and (b): photograph of the implemented SOPA loop with 65nm TSMC CMOS technology

The major burden to achieve the high enough loop gain is the high input capacitance of the CDA. In case of high limit cycle frequencies, we can use multiple driver stages to reduce the effective input capacitance. Another approach is inductive peaking, i.e. an inductor that resonates with the input capacitance, at the intended frequency.

Fig. 7-10-a shows the ordinary forward topology, with a single gain block for all of the signal components. In this method, the forward gain for RF and limit cycle frequency will depend on each other, and it is impossible to adjust them independently. The third approach, which suits to high frequency limit cycle amplifiers, is shown in Fig. 7-10-b, which allows for separate adjustment of RF and limit cycle gains. It is composed of an active duplexer exciting a VMCD.

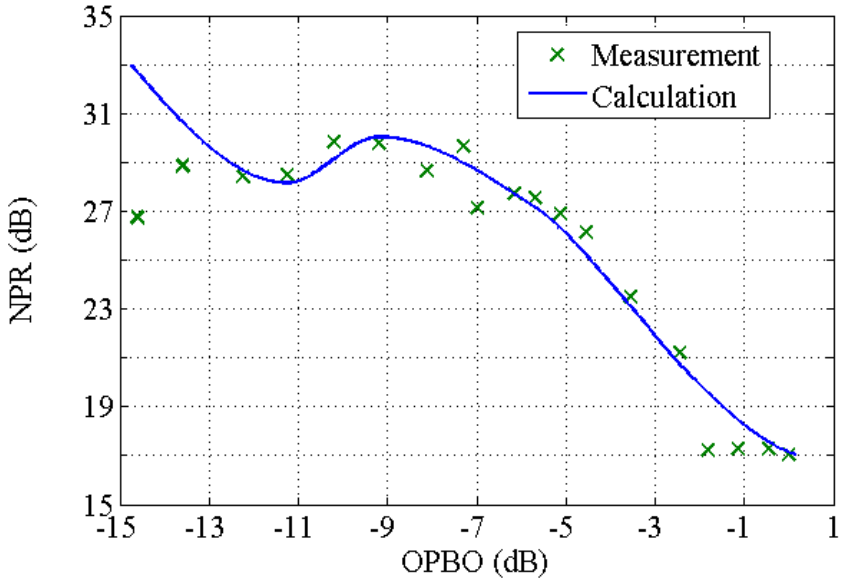
Figure (7-10-c) is a possible circuit realization of the duplexer. It uses a series LC resonator as the band stop filter. Above the resonance frequency, the input inductance cancels out the input gate capacitance at the limit cycle oscillation frequency. Therefore the series resonance frequency is adjusted between RF and limit cycle frequencies. C_3, L_1 and C_{in} act as a parallel LC resonator. Below the resonance frequency, the capacitor C_5 will act in parallel with C_{in} as a low pass filter in combination with active gain of M_2 which is in turn adjusted with current source M_4. Figure (7-10-d) shows the duplexer frequency response. M_1 and M_2 act as G_1 and G_2 gain stages. The gain is determined by the current adjusted by current sources M_3 and M_4. Fig. 7-10-d illustrates the frequency response for a sample active duplexer of Fig. 7-10-c.

The single forward gain topology opts for low frequencies, while the active duplexer topology provides the possibility of two independent forward gain adjustments, without affecting each other. Thus it opts for higher frequency SOPAs.

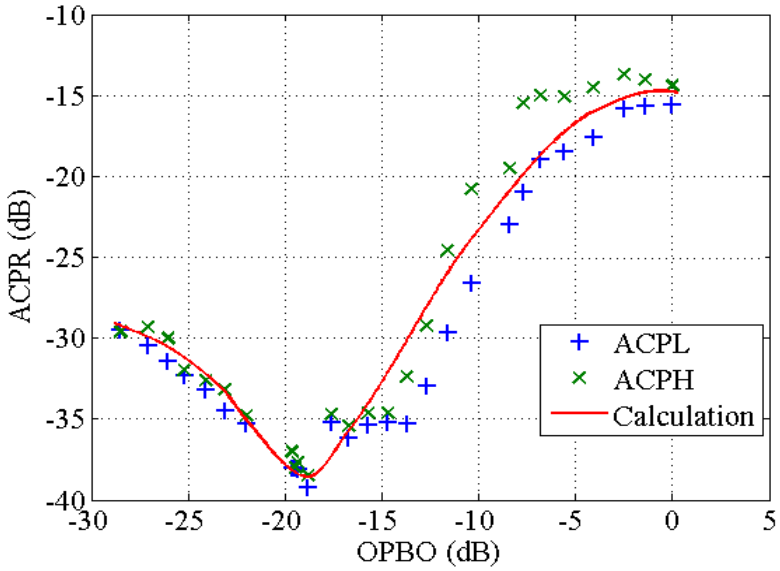
7.2.2 Circuit design

The single gain topology of 7-10-a is selected to design a SOPA. The SOPA loop is intended to oscillate at the limit cycle frequency of 1GHz and the input signal frequency to be centered at 200MHz. The schematic diagram of the circuit is sketched in Fig. 7-11-a. The CDA circuit consists of complementary PMOS and NMOS switches, including 20 PMOS and 10 NMOS transistors for the last stage (P_2, N_2) and 2 and 4 transistors for the driver stage (P_1, N_1) respectively. Every transistor of it has 32 gate fingers, each having 6um width. The driver is needed to increase the gain of the CDA and lower the input capacitance of the amplifier. Each transistor has 32x6um gate width. The output is fed back to the subtraction through a two stage RC filter, with the insertion loss and phase shift adjusted such as to provide the necessary gain and phase for oscillation, at the frequency of 1GHz. The loop input r (Fig. 7-11-a) goes to a PMOS source follower biased with a current source to maintain the required dc voltage at the input gate node of the subtraction. The output dc voltage coming from the feedback path is the same as the bias voltage needed for the gate node of the subtraction differential pair.

Fig. 7-11-b shows the photograph taken from the die. The dimensions are 720um×260um, including the bond-pads. The main blocks are shown with a frame. The filter capacitors are MIM types in parallel with diodes to prevent the antenna effect. The output LC reconstruction filter is realized with an external multi-harmonic load-pull system, to provide optimum termination for the best efficiency (i.e. high impedance at the switching frequency and its harmonics and Z_{opt} at the desired frequency [34].



(a)



(b)

Fig. 7-12(a): NPR vs. output power back-off; (b): 20 MHz offset upper and lower channel ACPRs versus output power back-off

TABLE 7-I

The extracted model parameters for driver and power stages

	$c_{in}(fF)$	$c_f(fF)$	$c_{out}(fF)$	$R_{out}(\Omega)$	a	b
Driver	1840	2380	2050	1.6	-0.43	6.5
PA	5048	5880	4200	0.5	-0.4959	11.3

7.2.3 Measurement and validation

The parameters of the power amplifier model are extracted based on the method presented in section E, through nonlinear optimization of the voltage gain error function. The model parameters and the results are given in TABLE 7-I.

The extracted model parameters will be used in the nonlinear analysis approach to find the nonlinear loop metrics, like transfer function and ACPR and compare them to the measured quantities, on the realized system.

The measurement setup is the same as the one depicted in Fig. 7-5, but with only one signal generator at the input of the loop as the DUT. The iMPT tuner should be terminated at the optimum impedance at the fundamental and open circuit termination at the limit cycle frequency and its harmonics.

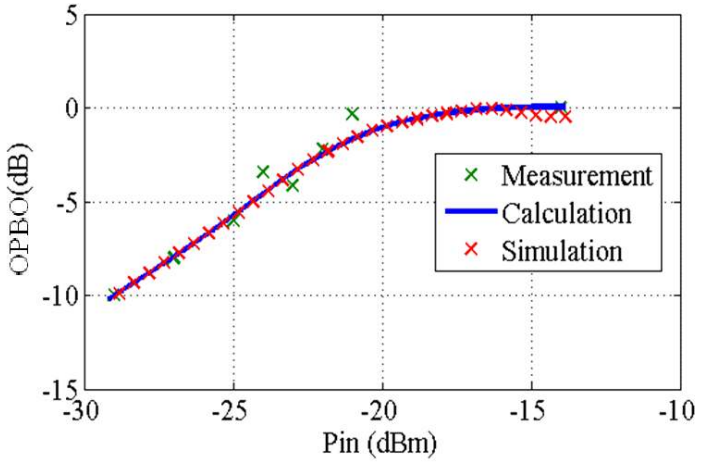
All of the measurements are illustrated in the Fig. 7-12 and Fig. 7-13 versus the calculation/simulation results. Fig. 7-12-(a,b) illustrate the variations in NPR and ACPR for higher and lower adjacent channels, along with the linear norm (minus sign in NPR is omitted for simplicity). Fig. 7-13-a shows the linearized AM to AM transfer function.

Fig. 7-12-b shows the calculated and measured ACPR results, which validates the proposed linearity analysis approach. The metrics show that the low frequency dithered PA meets the 3G spectral mask to 1 dB back off from the output peak power (≈19dBm at optimum load achieved from load-pull measurements.)A load pull setup was arranged and applied to the designed PA. The required load pull was a multi harmonic load pull, providing arbitrary tuning capability, simultaneously in three arbitrary frequencies. The load pull system used was the iMPT-704 of Focus™ Corporation [34], providing the optimum terminations for the limit cycle signal, desired signal and its third harmonic. The impedances are $2 - j50$ for the main signal and high impedance for limit cycle and it's third frequency. The reason for the high negative reactive part is the probe reactance. The load pull was tuned to the desired frequency, limit cycle frequency and its third harmonic. Optimum termination is achieved through peak power search in the whole smith chart region.

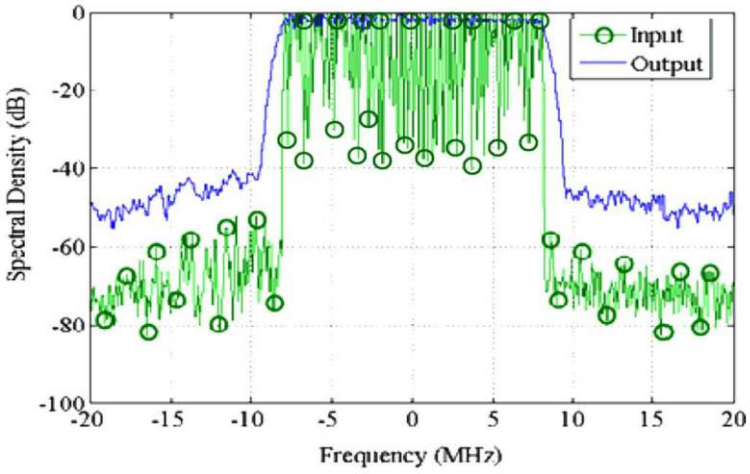
Although normally the second harmonic is not negligible (due to mismatch between PMOS and NMOS transistors), its value drops effectively with increasing impedance seen at the third harmonic of the switching frequency.

The maximum CW output power achieved from the structure is 20dBm along with peak drain efficiency of 65 percent of the CDA, for the maximum input power of -5dBm. The AM/AM characteristic is compared with linear simulation in Fig.7-13-a. Fig.7-13-b shows the input and output normalized spectra; the input signal has -65dB inherent ACPR.

The vector signal generator E8267D was used to generate the OFDM multi-sine and WCDMA signals. A 52 tone multisine with random phases is synthesized to mimic the 802.11g signal, and the power was swept the maximum level of -12dBm. The synthesized sig-



(a)



(b)

Fig. 7-13(a): Output power back-off versus P_{in} , measurement, calculation and Cadence simulation; (b): measured and normalized input and output Spectra of 1 channel 802.11 g for P_{in}=*-10dBm*

nal has a Peak to average ratio of 7.5 dB and notch bandwidth for NPR calculation was selected to be 1MHz. The NPR and ACPR is also calculated and plotted versus output power back-off (OPBO) in Fig. 7-12a.

The WCDMA signal with 64DPCH was taken from the signal source and the ACPR was measured with the spectrum analyzer, and constellation EVM was measured with 89600S vector signal analyzer. The maximum average power for a non-constant envelope in general, depends on its crest factor, and the maximum allowed input power, in view of device breakdown.

7.2.4 Generic design procedure

Again it is helpful to collect all the design aspects of a generic dithered system in one Figure. This is done in Fig. 7-14. The design flow starts with the circuit design of the Class-D amplifier based on the intended topology or technology, as discussed in chapter 4. Then, we set a level for the dither signal in a frequency much higher than that of the input signal frequency, based on sweeping its level and observing the required linearity metrics. The next step is frequency tuning for the dither. This step can be done by either measuring the dithered CDA by sweeping the frequency, or through linear programming optimization techniques introduced in chapter 6. As stated previously, it is always preferred to choose the least possible dithering frequency, for better efficiency or less reactive power loss. If the required metrics values are good enough, the open loop linearity satisfies the requirements. Otherwise, a feedback loop is

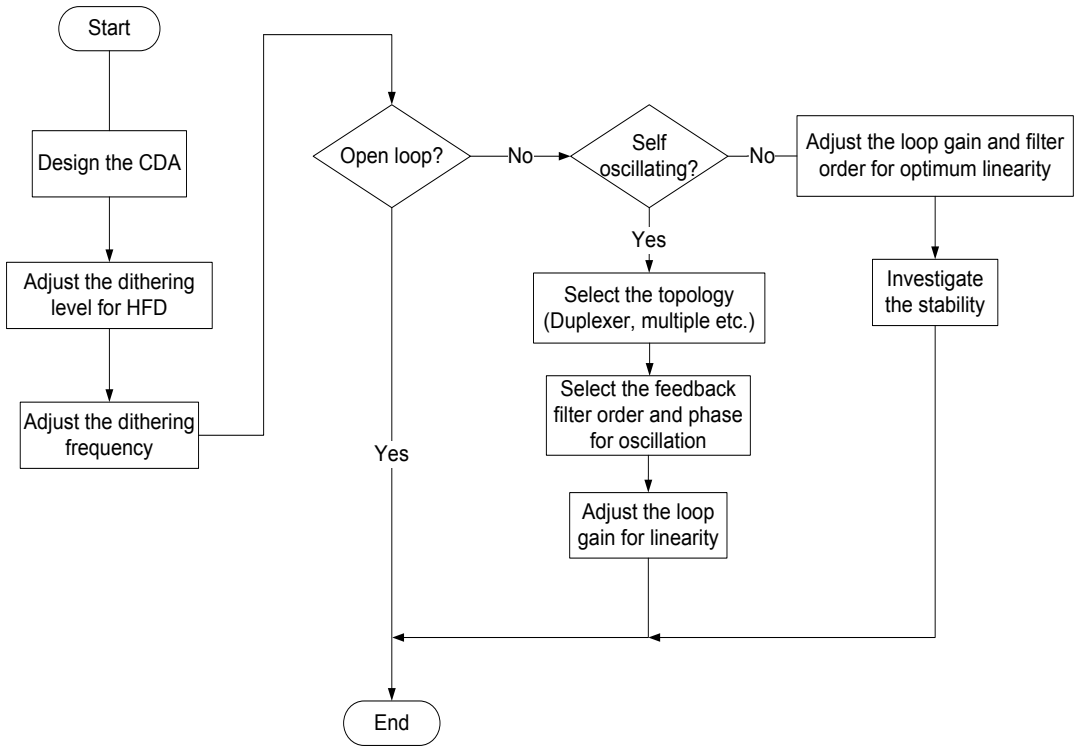


Fig. 7-14: The flowchart of the design procedure of a general dithered CDA system.

needed for linearity enhancement.

The architecture for the feedback can vary, but it is either autonomous (self-oscillating) or externally dithered. The only advantage of the former architecture is that it does not require an additional power source or signal generator as dithering, but the main drawback is that the dither level depends on the input signal level, which in turn will deteriorate the linearity. Therefore it is sometimes possible to achieve the same linearity, without the negative feedback loop, considering the gain requirements, i.e. the gain drop is still acceptable for excess dither level. The biggest disadvantages of the SOPA are the system complexity, especially for very high limit cycle frequencies, and the inability to fine-tune the oscillation frequency, in a normal loop, like the one realized in this chapter.

In case of targeting the autonomous system, like the one discussed in subsection 7.2, the Barkhausen criteria for a stable oscillation should be obeyed. The nonlinear phase shift of the CDA is very important in this type of architecture, especially for high frequency limit cycles. Moreover, the self-oscillating architecture is only applicable to HFD: in SOPA, the self oscillation frequency will quench, after excitation of the loop with a frequency higher than the designed limit cycle [92].

In case of targeting the ordinary negative feedback, the loop order and forward gain are the only important loop parameters, provided that there is no unintended limit cycle oscillation or chaotic behavior. Therefore, a band-pass filter in the feedback and a proper forward gain in the forward path should guarantee the intended linearity performance.

7.3 Conclusion

The HFD technique was applied to two sample test circuits and the linearity and efficiency results were measured. The test circuits where a VMCD and a SOPA, embedding the designed VMCD, oscillating at limit cycle frequency of 1GHz. A load pull was set up to find the optimum impedance for power and efficiency. The issues regarding the difference between the schematic level efficiency and the measured efficiency were discussed.

The linearity results show that the device shows a good linearity performance, with reduced drain efficiency compared to CW mode. It was observed that the drain efficiency drops by 7 percent after HFD, while it becomes linear and the spectral density of the WCDMA signal at the output of the amplifier complies to the standard mask for uplink (-33 dBc for first adjacent channel). The achieved linearity results validate the calculation results. The same linearity level could be achieved with open loop HFD, with less design complexity. This is due to the fact that the oscillation frequency of the SOPA cannot normally be tuned and the stability of the oscillation is easily influenced by the high frequency input signal excitation. The biggest disadvantages of the SOPA are the system complexity, especially for very high limit cycle frequencies, and the inability to fine-tune the oscillation frequency, in a normal loop, like the one realized in this chapter. Therefore HFD, realized in the form of open loop or closed loop none self-oscillating, can have even better linearity performance, with much easier design flow. The closed loop architecture can have the forward path topologies discussed in subsection 7.2.1,

i.e. active duplexer with independent gain adjustment for dither and signal, or a single gain block. The former is better for very high frequency HFD designs, while the latter works fine with lower switching frequencies.

Finally a generic design procedure for design and realization of a dithered class-D was proposed and summarized, which is applicable to any topology and architecture, including the self oscillating and externally dithered closed and open loop systems.

Chapter 8

Low frequency dithering

The open loop and closed loop class-D amplifiers both opt for low frequency dithering for linearization, due to their high slope gain. They may opt for drain efficiency improvement, depending on their process technology, or intrinsic capacitance value.

In order to verify the theoretical findings for linearity and efficiency behavior, two cases are realized and investigated thoroughly: an open loop voltage mode and an open loop current mode Class-D amplifier, while the former is dithered as a single ended amplifier and the latter one is dithered in common mode.

The VMCD amplifier used in this chapter is the same one that was designed in chapter 7. Besides a 2-Watt level CMCD was designed in PCB form, with LDMOS technology. The active differential pair acts as a differential switch, steering the current between two transistors. The circuit design process will be discussed in detail, in three steps. It will be shown that the drain efficiency will be improved by as much as 20 percent after dithering, for VMCD, and 4 percent after dithering for CMCD, while both comply with the spectral mask requirements defined for an uplink 3G signal [85].

All of the important linearity and efficiency metrics are measured, and compared with theoretical predictions, which again validates the analysis approach. The linearity shows the expected improvement, while the drain efficiency improved depending on topology.

8.1 Open loop VMCD

The open loop VMCD is exactly the same circuit as used in chapter 7 and in SOPA design. The load pull results are the same, and the linearity and efficiency were measured, after optimization of the dither frequency. The tuning results are also compared to those achieved with optimization, as discussed in chapter 6.

Fig. 8-1 shows a VMCD schematic, with LFD applied. The goal is to amplify a signal with a carrier frequency of 1GHz, with a class-D PWM amplifier dithered at the optimum dithering frequency f_d, below 1GHz.

The driver stage P_1, N_1 excites the power stage P_2, N_2, which delivers the required power to the load impedance Z_L. The relationships between the output power, power efficiency and load impedance were described in chapter 4 and 7.

The role of the driver is to increase the slope gain of the amplifier and also reduce the short-circuit power loss, through reduction of the transition time between the on-off switching states. The capacitors C_1 and C_2 are off chip, and the impedance Z_L is realized with the load tuner at the carrier frequency of 1GHz and optimum (open circuit) termination at dithering frequency and its harmonics. The biasing of the power stage will be adjusted by the output dc voltage of the first one, which will depend on the voltage VGG. The exact biasing should keep the output of both stages at the quiescent voltage of $V_{DD}/2$.

The load pull simulations and measurements both provide the same optimum fundamental output impedance for maximum efficiency, as the HFD case, discussed in chapter 7.

The most important issue is to get the required output power with the highest possible power efficiency. The ratio between the PMOS and NMOS transistors is very important for symmetric switching.

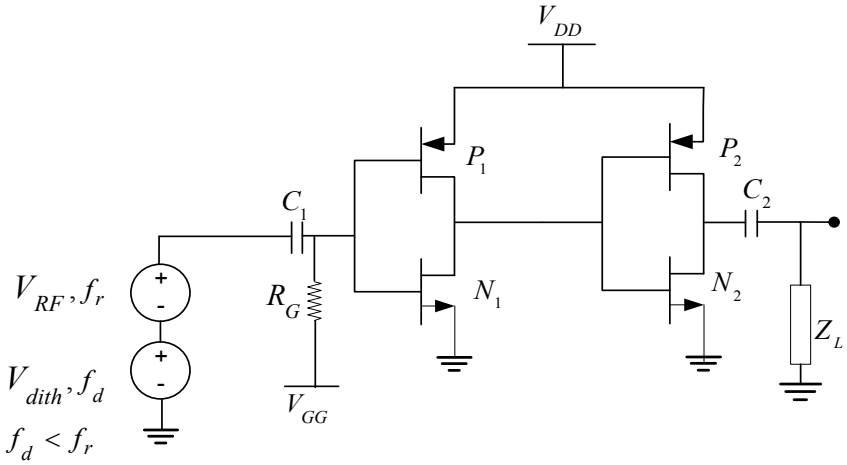
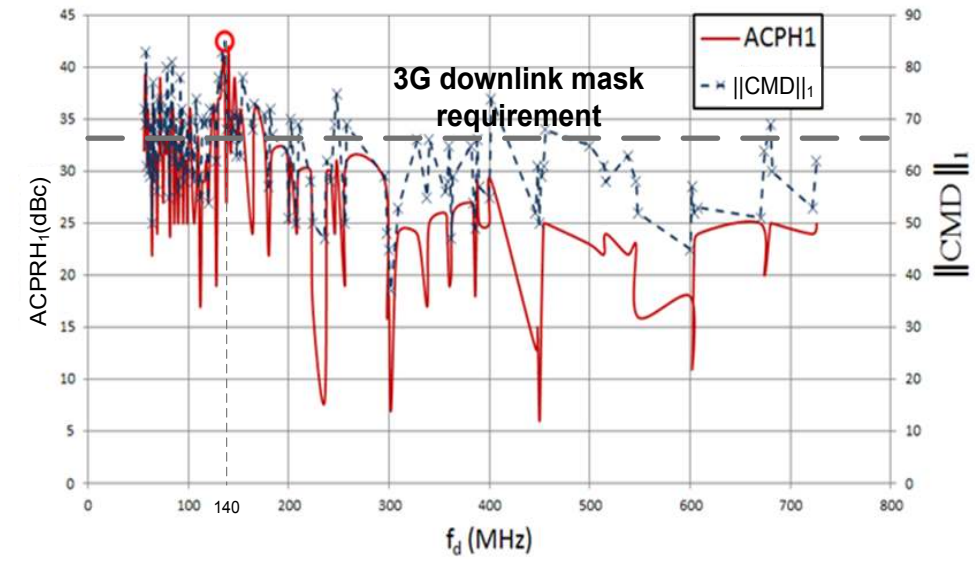


Fig. 8-1: Schematic diagram of VMCD, dithered with f_d



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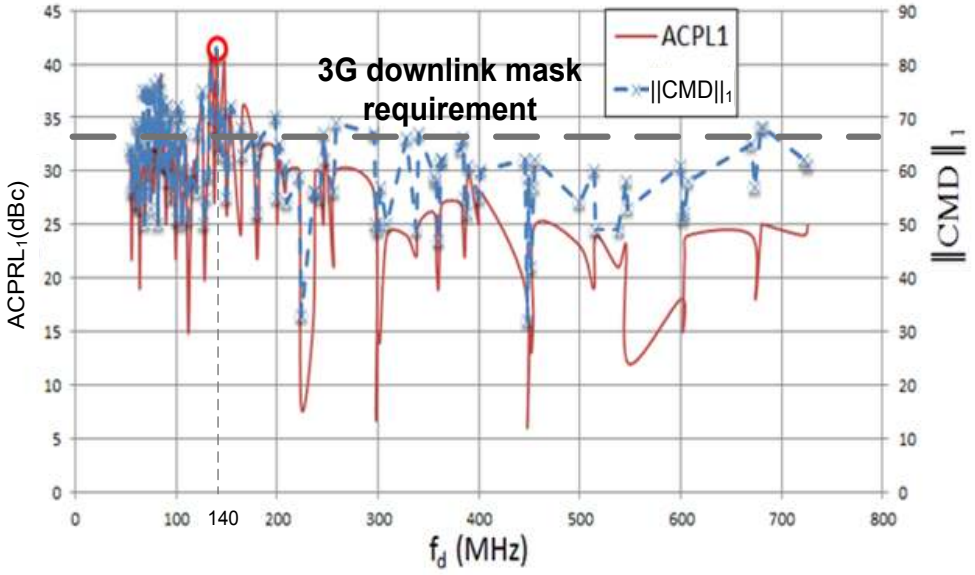


(b)

Fig. 8-2 (a): The adjacent higher and (b): The adjacent lower frequency channel power ratios versus the dithering frequency, for a 3G input signal taken from a signal generator. The solid lines are the measured values, and the dashed line with marker is the results of calculation. The two values have the same trend of variation versus the dithering frequency. The optimum frequency is the one with maximum ACPL1 and ACPU1 values, which is projected at 140 MHz on the f_d axis. There are other neighboring points which do not outperform the linearity compared to it, at are not equally good for higher and lower adjacent channels, for the 3G downlink requirements.

In the next subsection, the dithering frequency is swept and the best frequency, for the best

LFD spurious performance, is measured and compared to the best frequencies achieved through calculations. Afterwards the dither frequency is fixed and the AM/AM, linearity and efficiency results for CW and WCDMA signals are measured, under optimum load termination, achieved with the same iMPT tuner.

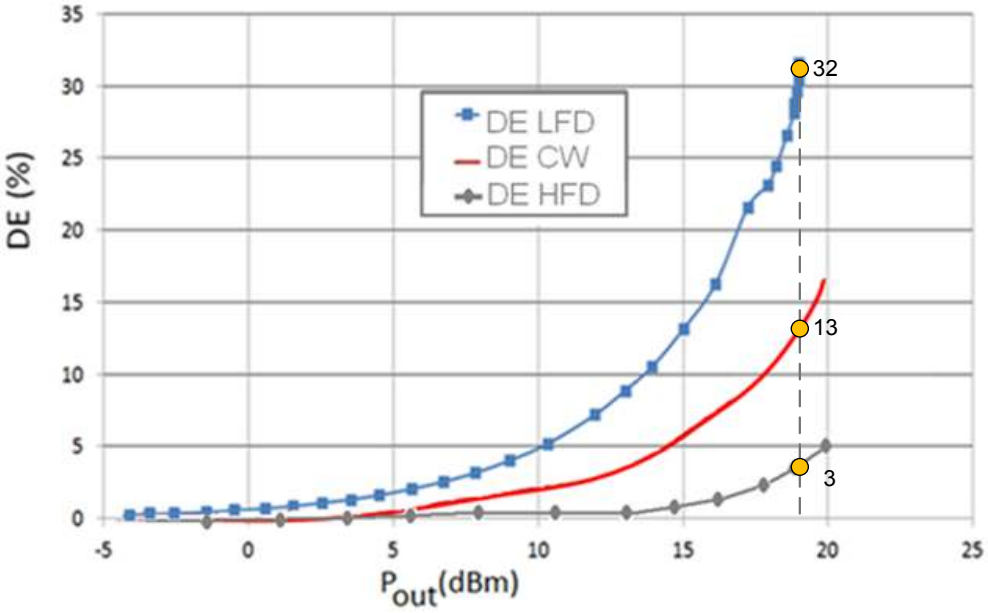
8.1.1 Fine tuning of the dithering frequency

A QPSK modulated signal with PAR of 7.5 dB, and the same bandwidth as a 3G standard carrier was taken from the signal generator. The channel bandwidth is 3.84 MHz and the ACPL1 and ACPH1 denote the ACPR results for first adjacent lower and upper channels. The ACPR is measured versus the dithering frequency for a signal carrier frequency fixed at 1GHz. Fig. 8-2(a,b) illustrate the variations in ACPR for higher and lower adjacent channels, along with the first order linear cross modulation norm of equation 6-6 (minus sign in ACPR is omitted for simplicity). There is a global optimum for the ACPR level, which coincides with the norm value of 82 and 84 in higher and lower adjacent channel power ratios, and corresponds to the dithering frequency of 140 MHz .

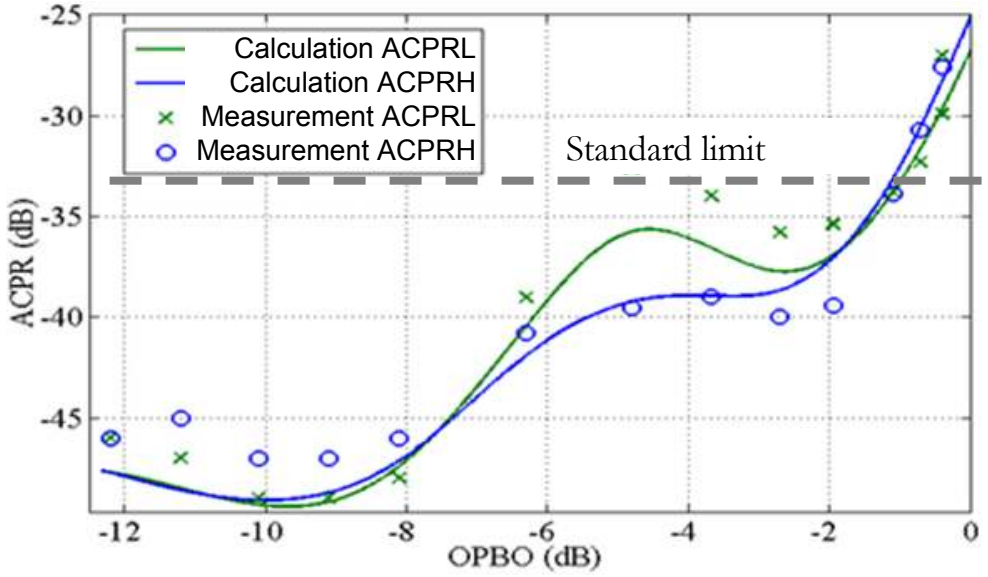
8.1.2 Measurement and validation

The agreement between the measurement, calculation and simulation validates the analysis approach presented in previous sections. The metrics show that the low frequency dithered PA meets the 3G uplink spectral mask to 1 dB back off from the output peak power (≈19dBm) at optimum load achieved from load-pull measurements. As we have observed, the linearity achieved with the HFD and LFD methods are the same but the efficiency is much better for LFD.

Finally Fig. 8-3-a illustrates the measured drain efficiency, which shows up to 20 percent improvement in its peak value, compared to CW mode, and 29 percent maximum improvement compared to HFD mode. Fig. 8-3-b shows the calculated and measured ACPR results, which validates the proposed linearity analysis approach. It should be noted that the ACPRs are exactly the same as those measured in HFD case, and the calculation results are again the same.



(a)



(b)

Fig 8-3: (a): Drain efficiency (DE) comparison for CW operation and LFD operation, measured for CW and LFD, versus the output power; (b): ACPRL and ACPRH versus output power back-off, calculation and measurement.

8.2 Open loop CMCD

The details of the circuit design for current mode class-D as a hard saturative nonlinearity, due to steering current between the two parallel paths along the balanced load, was discussed thoroughly in chapter 4. Common mode dithering can also be applied easily to this topology, due to its symmetry, as discussed in 4.1.5. At the output of this symmetric system only the dithering related spurious components around the odd harmonics of dithering and even harmonics of the input signal appear. All the other spurious will be in phase or common mode, and this makes the design of the output filter easier, and the overall performance much more linear.

Watt level power amplifiers like for base station or watt level handset applications normally cannot be directly implemented totally on a single IC, for size, parasitics and thermal management issues. An alternative for that is to use off chip discrete components with good enough quality factors and high current/voltage handling capability.

The process technology of the active part, used as a differential pair of the CMCD in this section is LDMOS, provided by NXP. It has higher capacitive loss compared to other technologies, which will work better for LFD. There are three many reasons to use this technology for CMCD:

1. High breakdown voltage (around 63 volt)
2. High gain
3. Ruggedness

These issues are all very important parameters in dithering techniques, and the effect of inductive loss reduction is more showing up, when the process has higher intrinsic capacitor. The selected LDMOS technology has a gate length of 750nm, and one gate finger. It will be wire bonded with 25 um diameter gold wires to the ENIG[1] coated (which has a gold coating of 0.6mm on top of FR4), to make the manual connection of the wire-bond possible. The design process includes schematic design, component selection for SMD[2] parts, full wave layout simulation and optimization with a commercial package like Momentum™ and testing after realization.

8.2.1 Circuit design

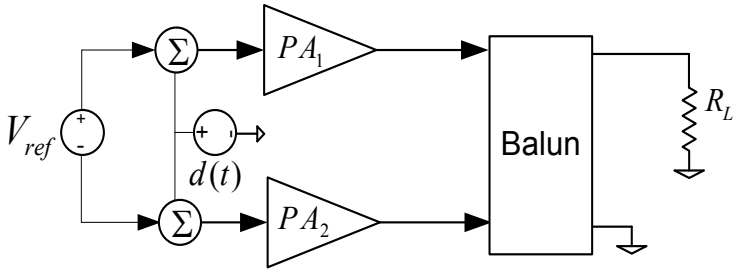
In the design phase three phases can be distinguished:

1. Discrete design with nonlinear device models.
2. Replacement of the real discrete components (with parasitics, quality factors, s-parameters file etc.) in simulations, and layout with full wave simulations.
3. Verification and optimization of the PCB layout (optional).

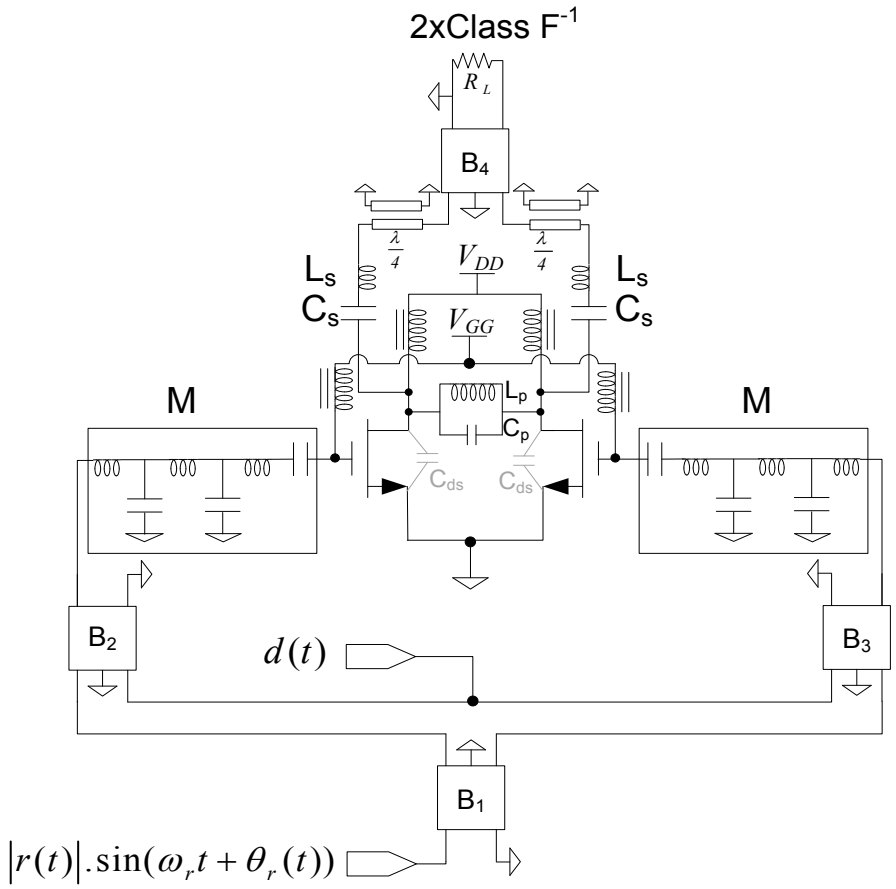
[1] Electro-less nickel induced gold coating

[2] Surface mount device

The optimum dithering frequency should be found for minimum spurious level. The system should be simulated with real SMD components and their quality factors; then the effect of the



(a)



(b)

Fig. 8-4 (a): Block diagram of the common mode dithering method; (b): schematic diagram of the CMCD with LDMOS (B_1 to B_4 are 0,180° baluns)

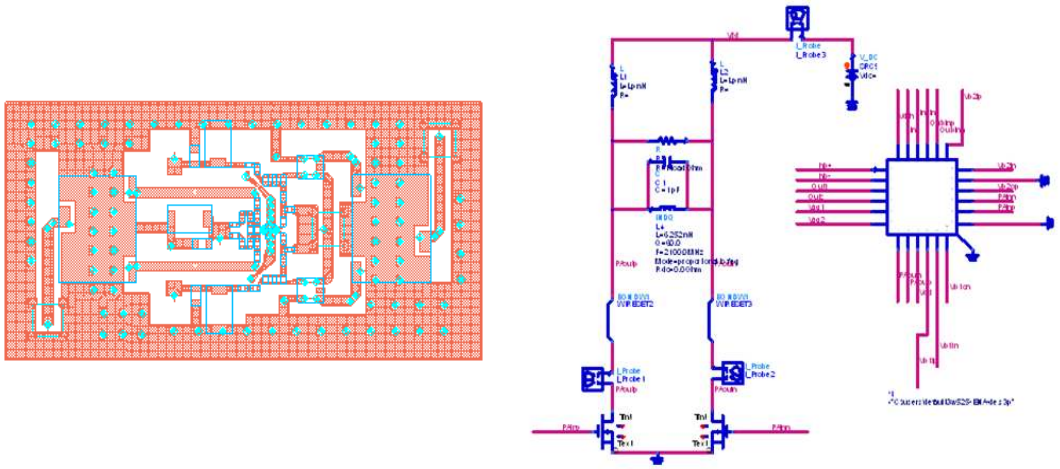
layout in the linear part of the system embedded the stability and linearity- efficiency of the amplifier and re-examined.

Discrete components design

The architecture and circuit level topology are illustrated in Fig. 8-3-a,b. Each PA in Fig. 8-4-a is replaced by a class F^{-1} in Fig. 8-4-b. Matching networks (blocks named as M in Fig. 8-3-b) at the input provide a unit voltage transfer function from the input to the gate input node. The output parallel tank L_p, C_p resonates with the intrinsic device capacitors C_{ds} and wire bond inductors. A Harmonic Balance is done to find the optimum load impedance for optimum power and efficiency.

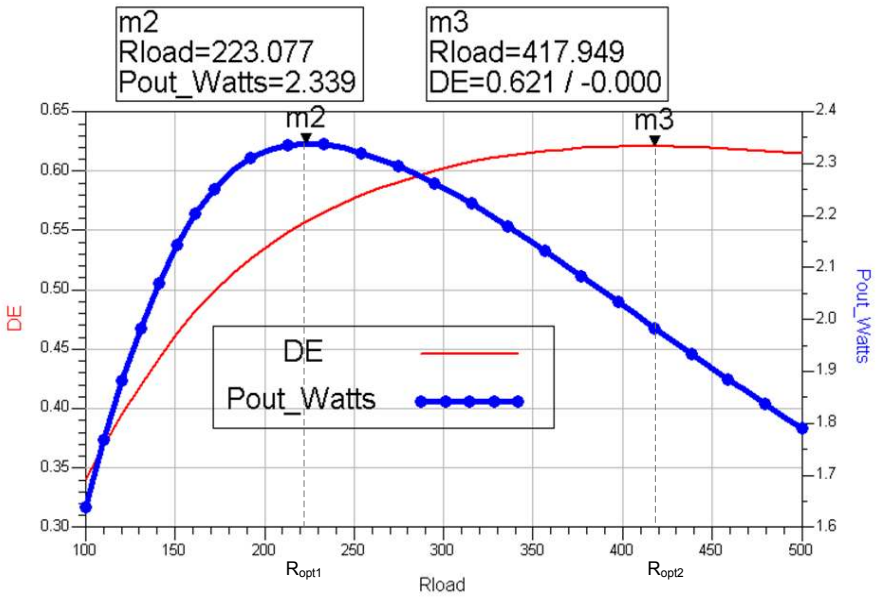
The balun B_4 used to split the message signal and combine the output differential powers at the output is a high power balun, (Anaren balun 3W525). The impedance data was embedded into the schematic design for simulation purposes. The same was done for the dithering baluns. The dithering baluns should have enough bandwidth to allow the low frequency dithering to pass through, with the least possible insertion loss. The selected balun for this purpose is ETC-1-1-13 of *MA/COM*, which is a transmission line transformer, with a bandwidth from 4.5 - 3000 MHz.

The series resonator Ls-Cs, is used to provide high impedance at all frequencies except for the frequency of operation (which is 2.014 GHz). This is due to the fact that the input impedance of the output power combining balun B4 is from 1.8 GHz to 2.5 GHz, which will deviate from the optimum termination for normal CW operation of a current mode class-D amplifier.



(a) (b)

Fig. 8-5: (a) The layout meshed in momentum for full-wave simulation; (b) circuit schematic in ADS™ for HB simulation. The whole layout is modeled in a 24 port data file achieved from Momentum.



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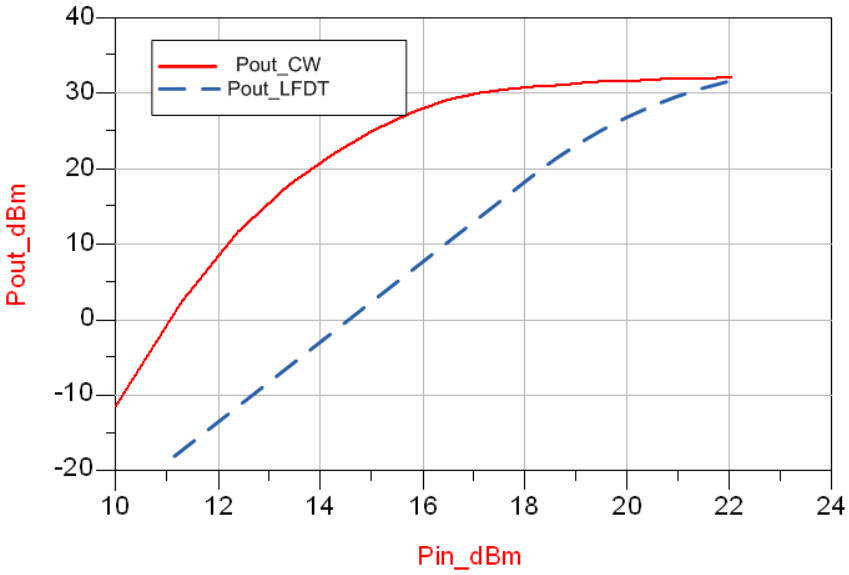


(b)

Fig. 8-6: (a) Load pull simulation for real part of the load impedance, after neutralization of the C_{ds} with tank inductance, to find the optimum load resistances for maximum power and drain efficiency, (b): AM-AM characteristics of the designed CMCD before and after low frequency dithering, The available dither power is 13 dBm, and the frequency is 520 MHz.

PCB layout simulation and overall performance

Microstrip quarter-wave impedances were designed for a 35 mils thickness FR4 PCB material, to convert the input impedance of the B_4 to the optimum load impedance of the CMCD, for optimum efficiency performance, which are 29 ohms and 416 ohms respectively.

Fig. 8-5-a illustrates the layout picture in momentum and the schematic level, including the layout effect and Fig. 8-6-a,b illustrates the load pull simulation results, and the linearization effect under optimum termination before and after dithering, versus input power, for a dithering frequency selected to be 520 MHz. This frequency will be later on validated as the optimum frequency form minimum spurious performance of the downlink 3G signal.

8.2.2 Fine tuning

The dithering was taken from an external power source and applied to the dither port, and the ACPR results for the first adjacent channel were measured against frequency as depicted in Fig. 8-7. The message signal is a QPSK modulated signal with a PAR of 7.5 dB, taken from another signal generator. The achieved ACPR level is compliant to the spectral mask requirements of 3G [85].

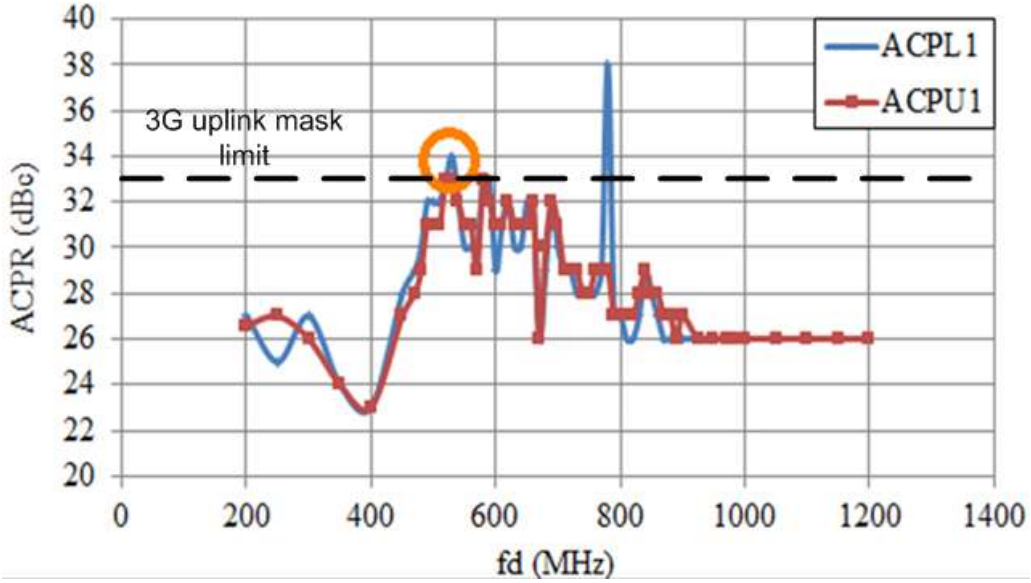


Fig. 8-7: The Adjacent higher and lower 3G channel power ratios versus the dithering frequency. The encircled point is the only point across the frequency grid that ACPU1 and ACPL1 values are maximized and comply to the 3G uplink mask requirement, simultaneously.

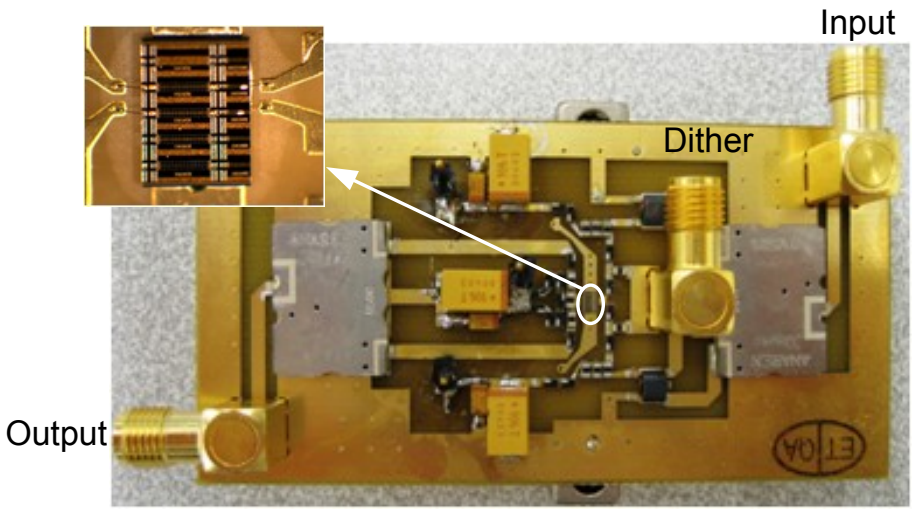


Fig. 8-8: Photograph of the implemented PCB, along with utilized LDMOS die

8.2.3 Measurement and verification

Fig. 8-8 shows the photograph of the PCB, with all the components, along with the magnified LDMOS wire bonded transistors.

Fig. 8-9 shows the LFD linearization effect, after measurement on the realized PCB, for dithering level of 24 dBm, and AM-AM characteristics before and after the dithering. No load-

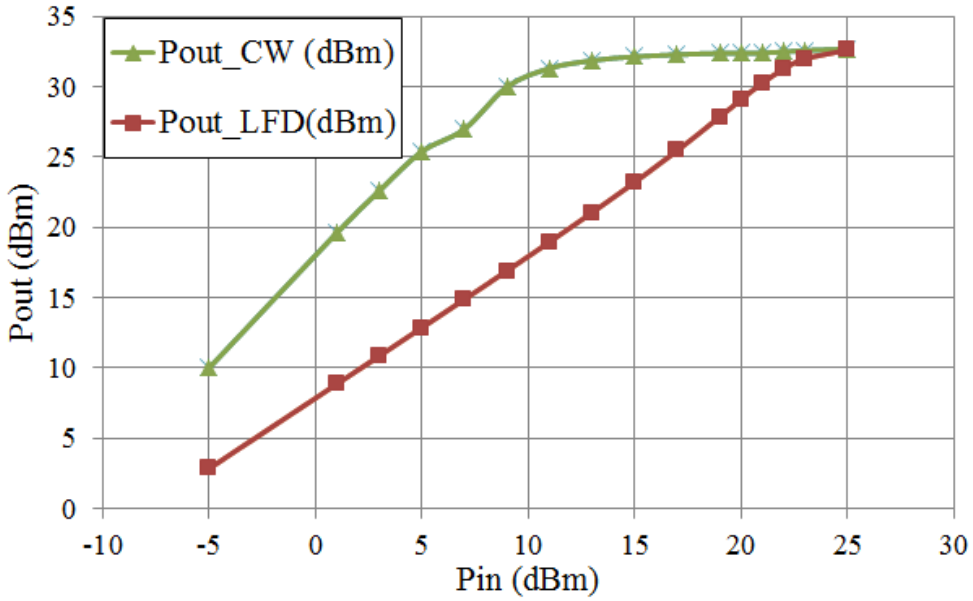
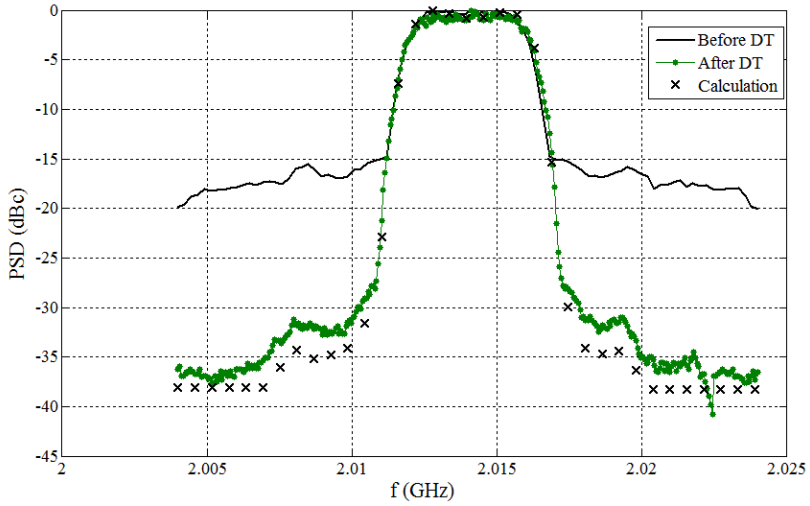
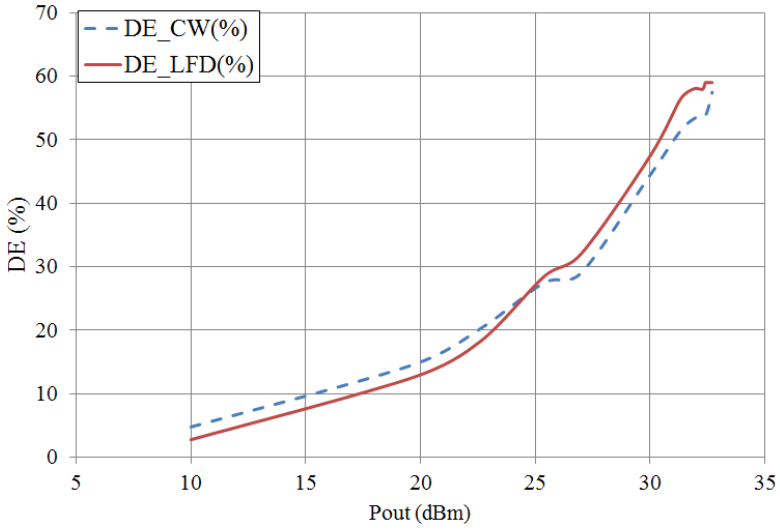


Fig. 8-9: Measured AM/AM characteristic of the designed CMCD and linearization effect of the original hard nonlinearity

pull measurement setup is needed, and the values measured are in agreement with the simulations. The output spectral density and drain efficiency for a downlink 3G signal as the message signal, are plotted in 8-10-a,b respectively, which clearly show the linearization process and the efficiency enhancement versus the output power. The maximum CW efficiency enhancement was 4 percent.



(a)



(b)

Fig. 8-10: (a) Normalized output Spectral density before and after dithering, at 520 MHz, for average output power of 23 dBm, besides the normalized spectrum calculation, the WCDMA downlink signal has a PAR , of 7.5 dB (b): Drain Efficiency versus output power, the LFD efficiency is higher for output powers more than 25 dBm, by maximum of 4 percent.

The CMCD is capable of delivering a CW output power of 32.8 dBm, to a single 50 ohms load, with drain efficiency of 58 percent after dithering. The average drain efficiency for WCDMA is 39 percent, for the average power of 23.5 dBm.

8.3 Generic design procedure

It is helpful to collect all design aspects of a generic dithered system in one Figure, as illustrated in Fig. 8-11. The design flow starts with the circuit design of the Class-D amplifier based on the intended topology or technology, as discussed before in chapter 4. Then, a level is set for the dither signal, based on sweeping its level and observing the required linearity metrics. The simulations should not necessarily be done for high frequency, in any two-tone non-commensurable input frequencies are enough, to optimize the linearity (defined by saturation point), because the spurious is not of importance for non-commensurable CW inputs.

The next step is to optimize the fundamental dithering frequency, which can be done by either measuring the dithered CDA by sweeping the frequency, or through linear programming optimization techniques introduced in chapter 6. As stated previously, it is always preferred to choose the least possible dithering frequency, for better efficiency or less reactive power loss. The difference between LFD tuning and HFD tuning is that there usually is a distinguished global maximum for linearity in LFD case. When the dither frequency is very small, the dithering is not satisfactory, and it limits the spurious free bandwidth, while for dithering frequencies close to the carrier frequency, the linearity is again very poor. Intuitively it is felt that in some point in between, which gives satisfactory spur level at the output. The trend is observed in

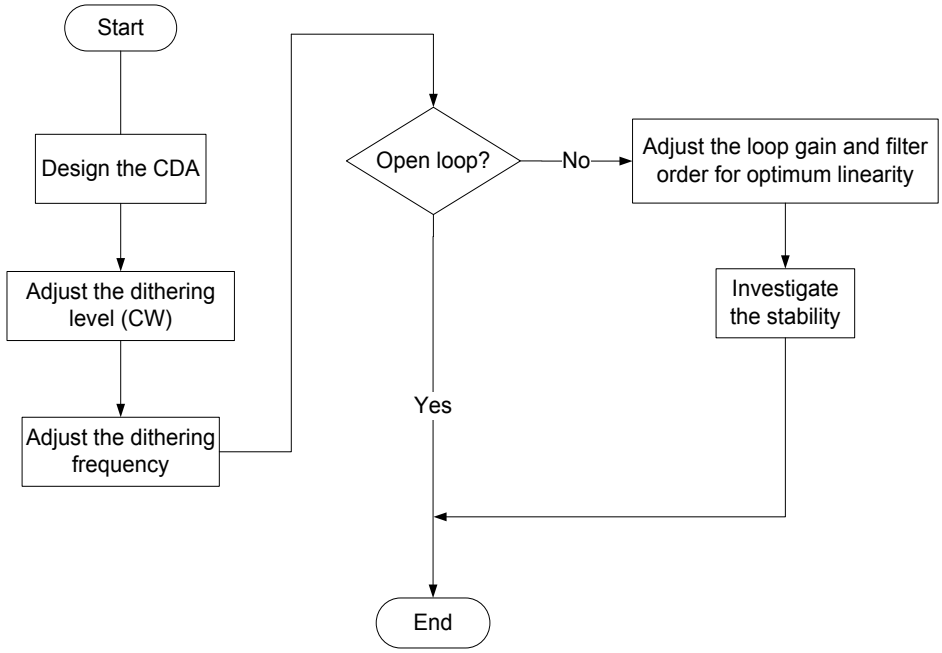


Fig. 8-11: The flowchart of the design procedure of a general dithered CDA system.

figures. 8-2 and 8-7, in which the points 140 MHz and 520 MHz were chosen as optimum points for ACPR. If the required metrics values are good enough, then the open loop linearity satisfies the requirements. Otherwise, a feedback loop is needed for linearity enhancement.

The architecture for the feedback can be a direct RF feedback or a Cartesian one, after down-conversion of the output signal to its in-phase and quadrature components.. The only advantage of architecture is that it does not require an additional power source or signal generator for the dithering, but its main drawback is that the dither level depends on the input signal level, which in turn will deteriorate the linearity. Therefore it is sometimes possible to achieve the same linearity, without the negative feedback loop, based on the gain requirement on the final amplifier.

In case of negative feedback, the loop order and forward gain are the only important loop parameters, provided that there is no unintended limit cycle oscillation or chaotic behavior. Therefore, a band-pass filter in the feedback and a proper forward gain in the forward path guarantee the intended linearity performance.

8.3.1 Conclusion

Two case studies related to verification of low frequency dithering were discussed, i.e. single ended voltage mode class-D PA which was designed and explained in chapter 7 and current mode class-D PA, designed and realized with 750um LDMOS process technology, as a 2 watt switched mode amplifier, on a PCB.

The fine tuning measurements and calculations were done for VMCD and CMCD circuits. For the latter circuit, a common mode dithering, as introduced in chapter 4, was applied, and it was observed that the system output, shows less sensitivity to the dithering frequency, due to common mode spurious component rejection, while a global optimum frequency for 3G signal was observed at 520 MHz.

The anticipated linearity and efficiency results were validated through measurements on a realized voltage mode class-D amplifier and a common mode dithered current mode LDMOS class-D amplifier, tuned at 1GHz and 2.014 GHz respectively. The measurement results agree with the theoretical linearity results, while giving up to 30 percent increase in measured drain efficiency for a realized 65 nm CMOS VMCD, and 4 percent improvement for a LDMOS CMCD, with good linearity in both cases. Using a closed loop architecture can enhance the linearity even more, for multicarrier applications. The realized system with this technique is a standalone linear and efficient power amplifier, without any additional signal processing.

The results confirm that LFD technique has the same linearity results as HFD, but the impact of reactive loss is reduced and drain efficiency is improved.

Chapter 9

Novel interpretations of dithering

The preceding chapters were devoted to analysis and simulation of the dithering process, its linearization effect, and formulation of the in and out of band nonlinearities. According to the theoretical findings, dithering can linearize the system, and it may also enhance the system efficiency in LFD case.

However, the analog applications of the dithering are not limited to what has been discussed so far. Moreover the averaging technique, which was used in derivation of equivalent nonlinearity, may be used, with some modification, to address the describing function calculation of frequency translating nonlinearities. The difference is that the averaging is done in different periods for the inputs and output(s) of the system, and therefore a different technique needs to be used.

New applications are investigated for three examples: dynamic load modulation (DLM), in combination with HFD, RF-ADC with LFD and area modulation power combining with LFD. Afterwards, the extended averaging techniques, known in the literature as multi-frequency averaging, is applied to a Gilbert cell mixer analysis problem, and conversion gain is achieved for a specific case of long channel device, as a closed form equation, which is confirmed with foundry model simulations. The achieved equation is insightful regarding the effect of the device parameters on the conversion gain.

9.1 Dynamic load modulation and dithering

Occasionally, load modulation has been used for amplitude modulation of a varying envelope signal on constant envelope phase signal [107]. Envelope elimination and restoration is a viable approach to transmit the information of any modulation type. Fig. 9-1-a is the overview to this approach, which is called dynamic load modulation (DLM), in which the amplitude variation of the original signal are modulation into the output constant envelope, through load modulation with a voltage controlled impedance tuner.

The problem concerning this EER approach is that the output envelope is not a linear function of the load impedance, or the control voltage of the tuner. Assuming that the output impedance of the amplifier can be shown as Z_{out}, and the Thevenin equivalent output voltage as V_{out}, the effective load voltage would be:

$$V_L = V_{out}.\left(\frac{Z_L}{Z_{out}+Z_L}\right) \tag{9-1}$$

Which is a saturation function versus Z_L and the saturation threshold depends on Z_{out}. Therefore the linearization will depend on the amplifier type and the envelope amplifier needs calibration.

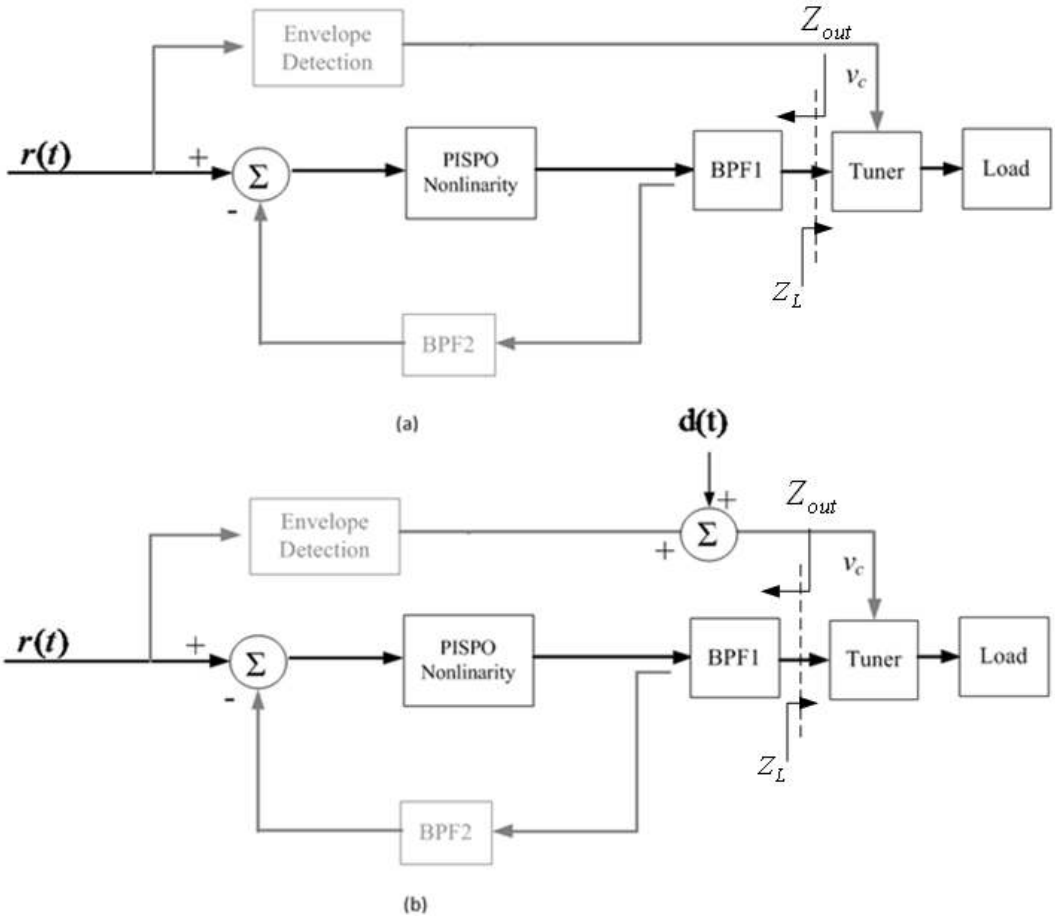
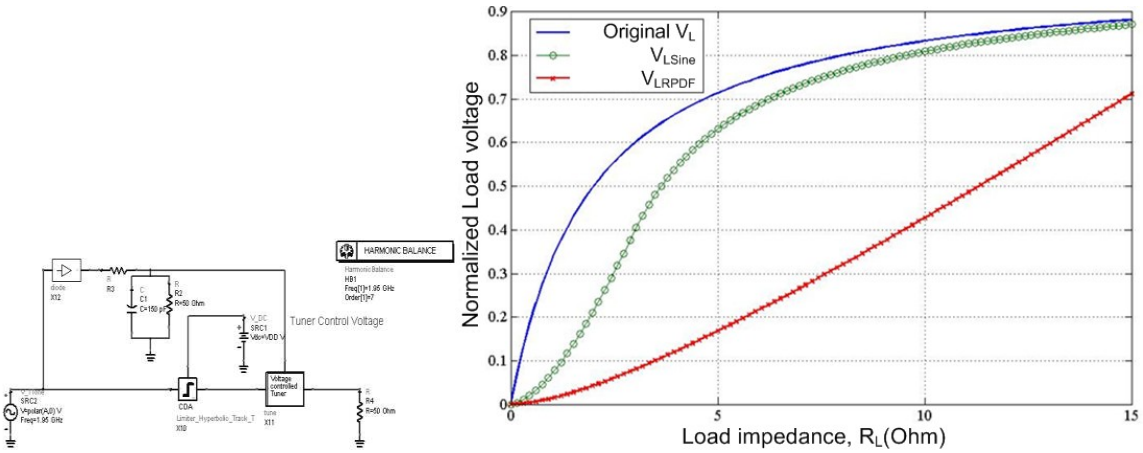


Fig. 9-1(a) Overview to the linearization using envelope; (b): HFD to linearize the EER in (a)



(a) (b)

Fig. 9-2: (a): The schematic diagram of the simulated circuit in ADS environment for DLM; (b): the original voltage transfer function, the HFD with sinusoid and uniformly dithered TF

HFD can be applied here, as illustrated in Fig. 9-1-b. Assuming that the v_c is the control voltage of the tuner, and it can linearly control the load impedance; the new load impedance would be a softer function of the dithered control voltage. The tuner topology may be a varactor tuned LC, with v_c controlling the varactor bias or the load may be adjusted by changing the characteristic impedance of a transmission line, by switching different number of quarter wave transmission lines in the tuner. After dithering and calculation of the equivalent nonlinearity, based on the convolution method explained in chapter 2, the following equations are achieved:

$$V_{L,Sine} = \frac{1}{4}\left(3 - \frac{4R_{out}\sqrt{\frac{(R_L+R_{out})^2}{Rout(2R_L+R_{out})}}}{R_L+R_{out}}\right) + \frac{\sqrt{R_{out}}\left(tan^{-1}\left(\sqrt{\frac{R_{out}}{2R_L+R_{out}}}\right)+tan^{-1}\left(\frac{R_L}{\sqrt{R_{out}(2R_L+R_{out})}}\right)\right)}{\pi\sqrt{2R_L+R_{out}}} \quad (9\text{-}2\text{-a})$$

$$V_{L,RPDF} = \frac{-R_{out}\,ln(R_L+R_{out})+R_L+R_{out}\,ln(R_{out})}{2R_L} \quad (9\text{-}2\text{-b})$$

where $RPDF$ subscript denotes rectangular (uniform) PDF and $Sine$ subscript denotes the sinusoidal dithered load, or control voltage signal. In the former case the control voltage is a high frequency saw-tooth while in the latter it is a sinusoidal. Fig. 9-2-a is the is the schematic diagram of the implemented system in ADS environment for simulation, and Fig. 9-2-b illustrates the original and dithered voltage transfer function, with uniform and sinusoidal HFD. As predicted, in both cases the characteristic is linearized, compared to the original characteristic, which makes the system more linear.

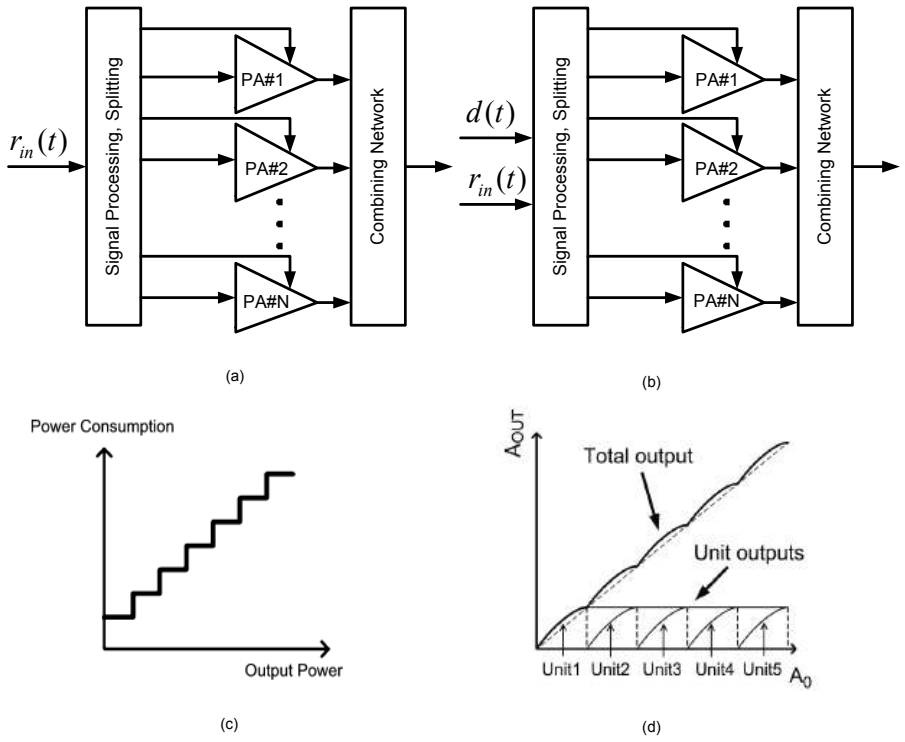


Fig. 9-3: Power Combining, with enhance back-off efficiency a: with envelope and/or input control, b: combined with dithering, c: Power consumption versus output power, d: Output power versus individual unit power [104].

9.2 Area modulation

The long term goal for wireless transceivers is to merge as many components as possible, if not all, to a single die in an inexpensive technology. Therefore, there is a growing interest in utilizing CMOS technologies for RF PAs.

Although several advances have been made recently to enable full integration of PAs in CMOS, it is still among the most difficult challenges for achieving a truly single-chip radio system in CMOS. This is exacerbated by supply voltage reduction due to CMOS technology scaling and on-chip passive losses due to the conductance of the substrate used in deep-submicron CMOS processes.

Conventional PA designs give maximum power efficiency only at peak power level. As the output power is backed off from that point, the efficiency drops rapidly. However, power back-off is inevitable in today's wireless communication systems. First, the need to conserve battery power and to mitigate interference to other users necessitates the transmission of power levels well below the peak output power. Transmitters only use peak output power when

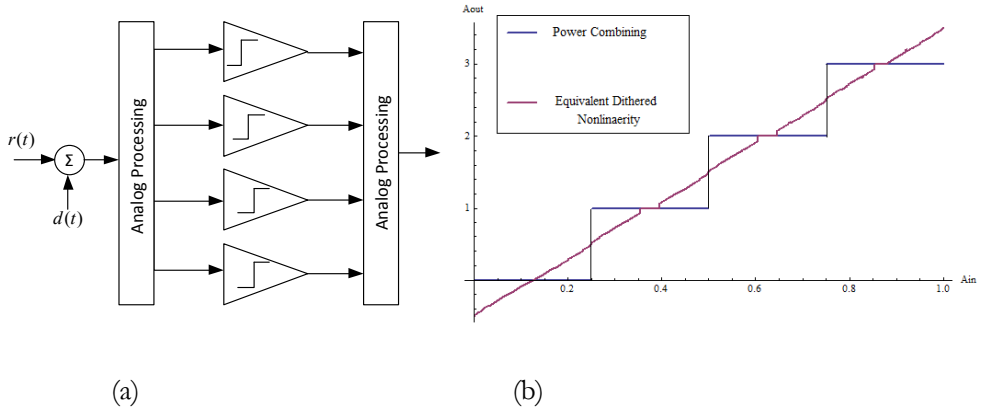


Fig. 9-4: a: Four step quantizer class-D array, area modulated by input level, b: Original staircase transfer function and equivalent dithered nonlinearity

absolutely necessary. In many situations, PAs are operating at 10–20 dB back-off from peak power. Second, the requirement for both high data rate and efficient utilization of the increasingly crowded spectrum necessitates the use of both amplitude and phase modulation, which lead to higher crest factor of the modulated signal.

A new feature that can be utilized to improve the power efficiency at power back-off is a power combining in a manner to force each amplifier work at its peak output power. When all of the amplifiers work at saturation, at each output power, a certain number of the amplifiers are in the system. The signal processing in order to turn on different number of amplifiers at different output powers can be done in different ways. Two of them are:

1. Turning PAs on through connection of the supply voltage/current, based on input signal level.
2. Turning the PAs on based on the value of the input, which is feasible through:
    a. Sensing the input level and connecting the required number of the inputs to the amplifiers [33], [105], [106].
    b. Analog processing of the inputs, to make the connections autonomous.

In all of these methods, the building blocks can be either switched mode or linear power amplifiers like class A or AB. Figs. 9-3-a,b are the block diagram of the described power combining before and after dithering. Fig. 9-3-(c,d) show the idea in terms of power consumption of each segment and output power variation versus individual unit contribution. As shown in Fig. 9-3-c, the power consumption is controlled versus the output power and this enhances the efficiency at output power back-off.

If each unit cell of 9-3-a is replaced by a CDA, then the input output transfer function of Fig. 9-3-d would look like a staircase quantizer. In this case the low frequency dithering will be beneficial, in order to enhance both linearity and efficiency. The efficiency would become uniform and may enhance in back-off depending on technology, and the linearity will definitely

improve. The describing function of staircase quantizer is explained and calculated in appendix A.II, and the resulting sinusoidal dithered equivalent nonlinearity versus the original one is plotted in Fig. 9-4-b.

9.3 RF-ADC with dithering

RF analog to digital conversion has been fully investigated in the literature. Placing the required Analog signal conditioning in the digital part has many advantages: more processing power is available, and the receiver chain would be much easier to control.

Low frequency dithering of a band-pass RF signal modulates the input information on the duty cycle and zero crossing frequency of the output pulse train for the narrowband input to the negative feedback loop of the Fig. 9-5-a. Quantization of the time axis is required in order to generate a synchronized bit stream usable by the digital part.

Roza has investigated the combination of ordinary limit cycle loop (HFD) with sampler; issues like quantization noise, over sampling effect and bandwidth are discussed in [10]. For low frequency dithering, a research should be done in order to model the effect of time domain quantization on the SNR of the output signal. That can be the subject of a future research.

The difference between ADC with LFD of Fig.9-5 with ordinary duty cycle is that the sampling frequency can be adjusted to sub-sample the output pulse train of the modulator. The Nyquist bandwidth for a band-pass signal of bandwidth Δf is $2.\Delta f$, and sampling lower than that may cause aliasing. For this ADC configuration, the minimum sampling will depend on the bandwidth of the input signal. A sampling frequency optimization, which is similar to the

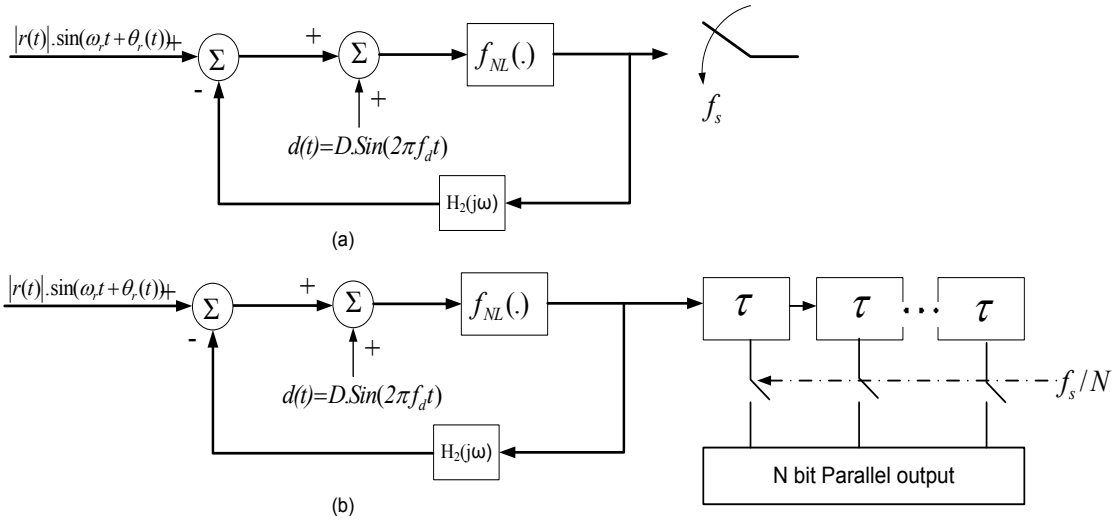


Fig. 9-5: (a): LFD sampler; (b): synchronized parallel sampling with delay line

tuning of chapter 6 can be developed for sub-sampling of LFD, to achieve the best linearity.

For example if the input is a 3G carrier at 1.95 GHz, it can be encoded in a pulse train by LFD frequency of 520 MHz, which will make the average switching frequency for optimum linearity roughly equal to 1.8 GHz. The resulting rectangular pulse then can be sampled with the delay line, at a sub-sampling frequency of 40Msample/sec, for a parallel bit stream of 40 Mbit/sec, as shown in Fig 9-5-b.

9.4 Mixer as dithering

Frequency translating describing function was briefly introduced in chapter 3, for a static single valued nonlinearity, excited by sum of two sinusoids. One major example of the frequency translating blocks is frequency mixer, used in transceiver chains. The local oscillator signal is multiplied by the RF/baseband signal to either up/down convert it to the desired frequency band. In order to preserve the signal information, the multiplication should be linear, i.e. the multiplication should only transfer the carrier frequency while envelope and phase information should be retained

In terms of frequency translated DF, this feature is described by constant frequency translated DF, with in the dynamic amplitude range of the RF/Baseband signal. In this interpretation, the LO resembles the dithering. If the LO is not present, the desired component of the output won't be present and the system is absolutely 'nonlinear', and proportionality is not satisfied. Furthermore if the LO is applied, it changes the system behavior in two different ways: It translates the frequency and keeps the conversion gain independent of the input level, so the resulting output will be linear frequency transformation of the input.

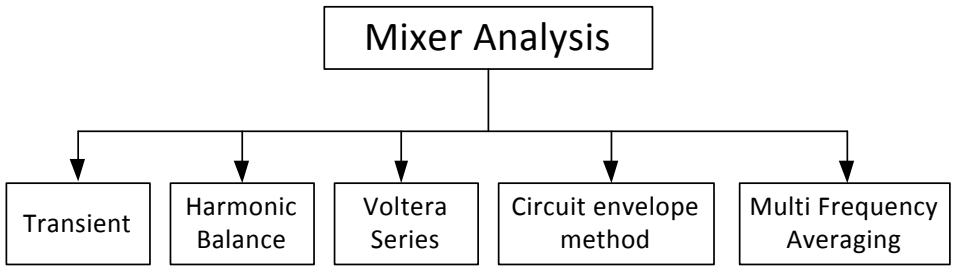
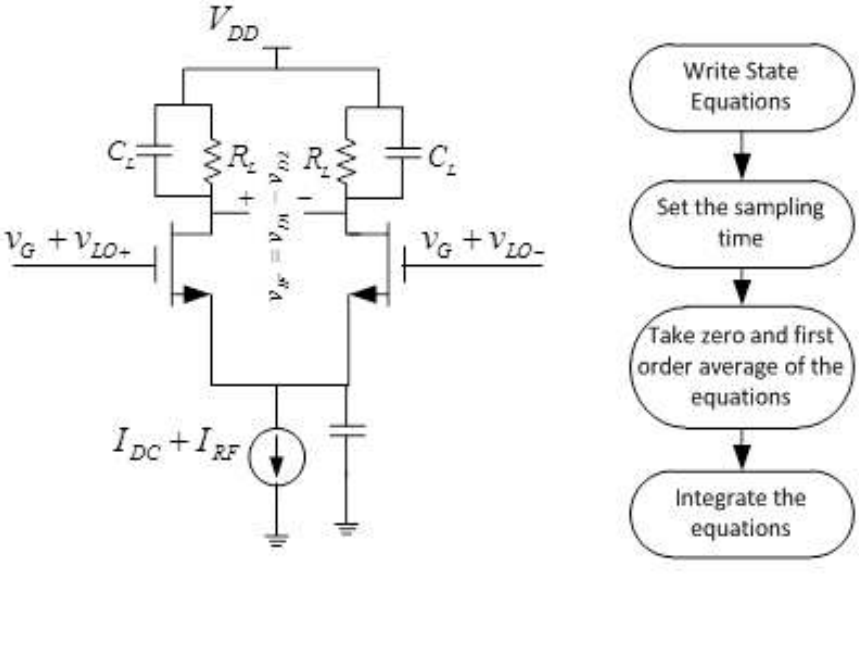


Fig. 9-6: Different methods of mixer analysis



(a) (b)

Fig. 9-7 (a): The single balanced Gilbert cell; (b): multi-frequency averaging technique flowchart

The difficult issue in mixer analysis in order to find the DF is that the input output function is not often describable by an analytic and static equation, and a simple formula cannot be offered in order to describe that. Normally the state variables of the mixer are described through a set of differential equation, which should be solved with a circuit simulator, through Harmonic Balance simulations. Fig.9-6 illustrates various analysis techniques used in the literature for mixer simulations. Harmonic balance analysis of mixer is given in [91] and [90] has used time variable Volterra series for nonlinear analysis.

The key to extract the frequency translated DF is to solve this set of differential equation for each frequency, in a manner similar to multi-carrier circuit envelope method or generalized HB method. This method is also called multi-frequency averaging in [56] and [57], in a totally different context of power electronic circuits. A similar averaging method, inspired by the procedure, presented in [56] and [57] can be applied to mixers. The principal steps are summed up in Fig. 9-7-b, for a typical Gilbert cell mixer of Fig. 9-7-a.

Among different topologies the Gilbert cell mixer is selected for a case study example. The multi frequency averaging technique tries to expand the signal versus its zero and higher order harmonics, which are all time variant. Then a new set of differential equations are derived,

from the original state equations of the nonlinear system. The new set of differential equations is of a much lower sampling rate, and the sample rate is determined by the IF band width. In

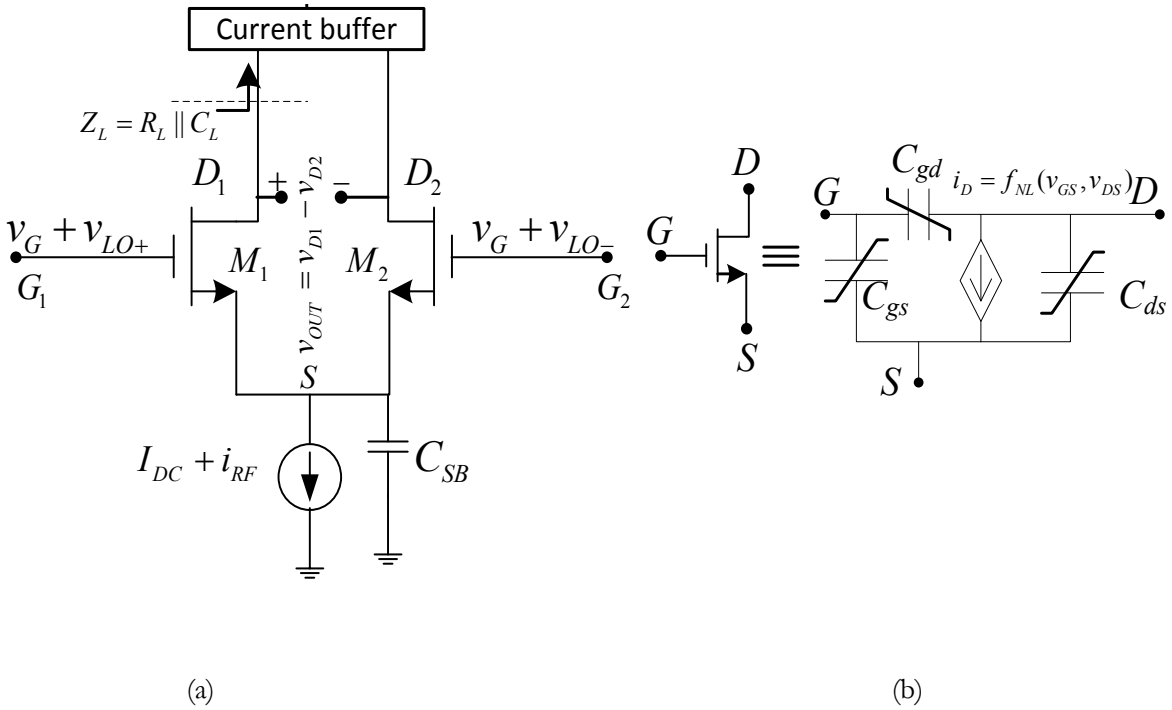
circuit CAD techniques this method resembles multi-carrier envelope but it is not based on harmonic balance solution of the system, and it can be used for random signals.

In order to be more specific about the circuit topology, Fig. 9-8-a shows the schematic diagram of a single balanced mixer and its transistor equivalent circuit. The current buffer at the output of Fig. 9-8- (a) has negligible input impedance compared to the device output impedance and therefore channel modulation will only depend on the RF input voltage. Fig. 9-8-b is the typical FET device model used in the mixer. The voltage controlled current source can be described as a polynomial function of the input voltage, while the parasitic capacitors can sometimes be approximated as linear equivalent capacitances. The MFA steps are followed according to the flowchart, in the following subsections.

Driving state equations

The first step in solution of this circuit with any method is to write the governing KCL equations, or state equations. Assuming that the dc voltage of the drain is the same as V_{DD} and writing KCL at the source terminal of M_1 will result in:

$$I_{DC} + i_{RF} + C_{SB}\frac{d(v_S)}{dt} - f_{NL}(v_{G1} - v_S, v_{DD} - v_S) - f_{NL}(v_{G2} - v_S, v_{DD} - v_S) +$$
$$C_{ds1}.\frac{d(v_S)}{dt} + C_{ds2}.\frac{d(v_S)}{dt} - C_{gs1}.\frac{d(v_{G1} - v_S)}{dt} - C_{gs2}.\frac{d(v_{G2} - v_S)}{dt} = 0 \qquad (9\text{-}3\text{-a})$$



(a) (b)

Fig. 9-8: (a) Current buffered single balanced mixer and (b) the transistor equivalent circuit

$$-C_{ds1}\frac{dv_S}{dt}-C_{gd1}\frac{dv_{G1}}{dt}-i_L+f_{NL}(v_{G1}-v_S,v_{DD}-v_S)=0 \tag{9-3-b}$$

In general, all of the capacitors in the model are nonlinear, which can be modeled as polynomial functions of terminal voltages v_{GS} and v_{DS}. The equation 9-3-(a) describes the operation of the circuit completely with v_S as the state variable. Knowing the v_S enables us to find the output current and voltage, from solution of 9-3-(b) and solving it versus i_L, we can eventually all of the important mixer metrics, like conversion gain, compression point, optimum bias etc. Equation 9-3-a is a first order nonlinear differential equation.

Taking averages

The numerical solution of A.V-1 can be done using a simulator. Another approach is to use the averaged differential state equations. Based on the approach taken in [56], any signal can be expanded as a Fourier series, around an arbitrary sampling frequency ω_s, as follows:

$$x(t)=\langle x(t)\rangle_0+\sum_{k=-\infty,k\neq 0}^{\infty}\langle x(t)\rangle_k\exp(jk\,\omega_s t) \tag{9-4}$$

in which the $\langle x(t)\rangle_0$ and $\langle x(t)\rangle_k$ are the zero order and kth order averages respectively, and are defined as follows:

$$\langle x(t)\rangle_k\triangleq\frac{\omega_s}{2\pi}\int_0^{\frac{2\pi}{\omega_s}}x(t)\exp(-jk\omega_s t)dt \tag{9-5}$$

It should be noted that the zero order average is not the same as the DC component of the signal, and will depend on the sampling frequency ω_s. The averaging is done on orthogonal bases; therefore if we take the averages of the equations 9-3-a, each individual average should be equal to zero. Calling the left side of equation 9-3-a as $'eqn_1'$, the kth order average, for any order of 'k' should be equal to zero, i.e. $\langle eqn_1\rangle_k=0$, for any k. This averaging is the same as writing KCL for each harmonic of ω_s at the output separately.

Assuming that the output signal can be totally described by its first and zero order averages, as follows:

$$v_s=\langle v_s\rangle_0+\langle v_s\rangle_1\exp(j\omega_s t)+\langle v_s\rangle_{-1}\exp(-j\omega_s t) \tag{9-6}$$

and substituting 9-6 in 9-1-a, we obtain two differential equations for zero and first order averages of the output voltage as follows:

$$I_{DC}+C_{SB}\frac{d(\langle v_s\rangle_0)}{dt}-\langle f_{NL}(v_{G1}-v_S,v_{DD}-v_S)\rangle_0-\langle f_{NL}(v_{G2}-v_S,v_{DD}-v_S)\rangle_0+$$
$$C_{ds1}.\frac{d(\langle v_s\rangle_0)}{dt}+C_{ds2}.\frac{d(\langle v_s\rangle_0)}{dt}-C_{gs1}.\frac{d(v_{G1}-\langle v_s\rangle_0)}{dt}-C_{gs2}.\frac{d(v_{G2}-\langle v_s\rangle_0)}{dt}=0 \tag{9-7-a}$$

$$C_{ds1}\frac{d(< v_{D1} >_1 - < v_S >_1)}{dt} + C_{gd1}\frac{d(< v_{D1} >_1 - < v_{G1} >_1)}{dt} + \frac{< v_{D1} >_1}{R_L} + C_L\frac{d(< v_{D1} >_1)}{dt} + < f_{NL}(v_{G1} - v_S, v_{D1} - v_S) >_1 = 0 \quad (9\text{-}7\text{-b})$$

which is a new set of differential equations versus zero and first order averages of the state variable v_s. Equations 9-7-(a, b) are the KCL equation for DC and fundamental harmonics around ω_s.

Solution of the differential equations

A two dimensional polynomial ($i_D = f_{NL}(v_{GS}, v_{DS})$) fitted to the DC I-V characteristic of the transistor, can be used to characterize the f_{NL} function as follows:

$$i_D = \sum_{l=0}^{L}\sum_{m=0}^{M} p_{lm} v_{GS}^{l}\, v_{DS}^{m} \quad (9\text{-}8)$$

when the i_D is a function of v_{DS}, a closed form solution is not feasible, and equation 9-3-a (or equivalently 9-7-(a,b)) can be solved numerically. . The analysis results for a sample single balanced Gilbert cell multiplier for 60 GHz, under simplifying assumptions of negligible channel length modulation, which makes the equation 9-8 independent of the drain-source voltage, and assumption of linear intrinsic capacitors, is given in appendix A.V.

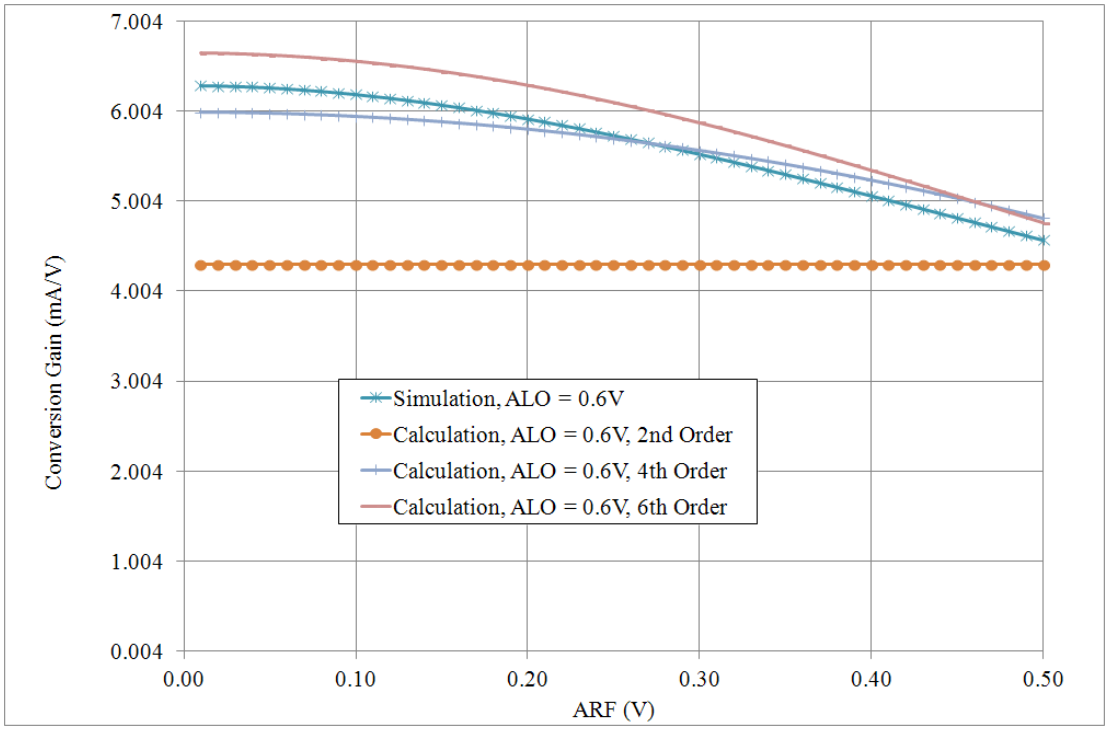


Fig. 9-9: Calculation and simulation of a single balanced mixer with long channel, and linear parasitic approximation

The method is *the same* as *multi-carrier envelope*, when solved numerically and has less no significant contribution, given the fact that the existing state of the art techniques are able to solve any topology with any degree of complexity.

The achieved current gain is plotted in Fig. 9-9, versus the RF amplitude, for a designed mixer in 60GHz, based on the closed form relationship given in appendix A.V. The gain results are plotted for different v_{GS} polynomial order, and it is seen that the compression is more accurate for higher orders. The simulation results are for 240 nm TSMC CMOS technology.

9.5 Conclusion

In this chapter, three new applications of the dithering phenomena, which were dynamic load modulation, RF-ADC, and area modulation power combining-linearization, were presented. For mixer analysis, multi-frequency averaging was introduced as an efficient and insightful technique, which was based on the solution of the nonlinear state differential equations of the system, with a sampling rate determined by the information bandwidth. In the special case of long channel (older) process technologies, where the output resistance of the device is negligible, the gain of the system can be derived in closed form. The results agree with the simulation with real device models.

Conclusions

In this thesis, it has been proven that the dithering technique can be applied for simultaneous improvement of linearity and efficiency of switched mode power amplifiers. A generic framework, based on averaging techniques has been developed, in order to provide a theoretical background for dithered systems. This framework provides the answers to the questions posed in chapter 1.

The concept of equivalent nonlinearity has been introduced, based on the time-domain averaging and statistical averaging. All important nonlinearity metrics (e.g. ACPR, SNDR etc.) for dithered relay-type nonlinearities were derived in closed form, for generic random input signals. It was shown that a proper performance of the dithered system requires possessing a high enough slope gain. As proper circuit topologies for dithering, VMCD, SOPA and CMCD were singled out, due to their high slope gain and high power efficiency.

The effect of the dithering frequency on the efficiency was studied and two different conditions for both high and low frequency ditherings (HFD and LFD) were identified. The LFD technique was introduced for the first time. Both HFD and LFD linearize the switched mode amplifier. Moreover LFD is superior since it increases the power efficiency of the nonlinear block, due to reduction of the reactive power loss. For both HFD and LFD, the spurious level depends on the frequency of the dither signal; there are optimum frequency allocations for the dither, in which the output spurious level will be minimized; these points can be obtained through a systematic optimization procedure.

For both HFD and LFD, a generic synthesis approach has been developed and utilized to design the dithered systems, based on the input signal type and circuit topology, and required linearity-efficiency compromise.

The validation of the theoretical findings has been approved through realization and measurement of three test circuits, which were CMOS VMCD, SOPA and LDMOS CMCD. It was shown that for a 2 watt LDMOS power amplifier, the maximum drain efficiency was improved by 4 percent and the first adjacent channel ACPR by 25 dB, which satisfies the standard spectral mask requirement for downlink WCDMA, at an average output power of 23.5 dBm.

The achieved knowledge on dithering has further been utilized for other applications. to introduce three new architectures and one new analysis method. Linearity can be enhanced by

combination of dynamic load modulation (DLM) and HFD dithering. An area-modulation power-combining technique was introduced as an array of switched mode PAs; in combination with LFD it enhances the back-off power efficiency and the average power efficiency. A new RF-ADC architecture, in combination with LFD was introduced, which benefits from a lower clock rate compared to conventional sigma delta techniques.

Finally, based on a multi-frequency averaging approach, a closed-form description was achieved for the conversion gain of a single balanced Gilbert cell mixer, and for long-channel technologies the achieved gain formulas were validated through comparison with simulations.

Recommendations

There is plenty of room for future investigation about the following aspects:

- Development of a thermal behavioral model, which will affect the performance of the dithered SMPAs, in long durations of performance and possibly change all of the important metrics. The model can address long term and short term effects, as well as static and dynamic effects.

- Realization of dynamic load modulation in combination with HFD to enhance the linearity, as discussed in chapter 9.

- Realization of the RF ADC, with the proposed dithering method described chapter 9.

- Investigation of combination of dithering with pre-distortion technique, to enhance the linearity and compensate the wide band memory effect for wide-band applications, like multicarrier 3G.

- Realization of RF or Cartesian feedback loop, around the dithering, in order to enhance the linearity, for multi-carrier and ultra linear single carrier applications.

- Investigation of the effect of different terminations on the different frequency components available in the dithered system output terminals, and waveform engineering of the current/voltage wave forms of the active devices, to enhance the power efficiency.

References

[1] T. Piessens and M. S. J. Steyaert, "Behavioral analysis of self-oscillating class-D line drivers," *IEEE Trans. Circuits Syst. I,* Reg. Papers, vol. 52, no. 4, pp. 706–714, Apr. 2005.

[2] S. Ouzounov et al., "Design of high-performance asynchronous sigma delta modulators with a binary quantizer with hysteresis," in Proc. *Custom Integr. Circuit Conf.*, Oct. 2004, pp. 181–184.

[3] F. A. Malekzadeh et al., "A new statistical approach for nonlinear analysis of limit cycle amplifiers," in *Proc. IEEE RadioWireless Symp.*, Jan. 18–22, 2009, pp. 47–50.

[4] A. Gelb and W. E. V. Velde, *Multiple-Input Describing Functions and Nonlinear System Design*. New York: McGraw-Hill.

[5] K. M. Gharaibeh, K. G. Gard, and M. B. Steer, "In-band distortion of multisines," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3227–3236, Aug. 2006.

[6] K. Gard, *Autocorrelation Analysis of Spectral Regrowth Generated by Nonlinear Circuits in Wireless Communication Systems*. San Diego, CA: Univ. California, 2003.

[7] K. A. Remley, "Multisine excitation for ACPR measurements," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 8–13, 2003, vol. 3, pp. 2141–2144.

[8] R. J. Webster, "Formulas which approximate the distribution of a sinusoid plus noise," *IEEE Trans. Inf. Theory*, vol. IT-29, no. 5, pp. 765–767, Dec. 1983.

[9] M. Abramovitch and I. A. Stegun, *Handbook of Mathematical Functions, With Formulas, Graphs and Mathematical Tables*. New York: Dover, 1966.

[10] E. Roza, "Analog-to-digital conversion via duty-cycle modulation," *IEEE Trans. Circuit Syst. II, Analog Digit. Signal Process*, vol. 44, no. 11, pp. 907–914, Nov. 1997.

[11] B. Kelleci et al., "THD + Noise estimation in class-D amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS),* May 27–30, 2007, pp. 465–468.

[12] W. Shu and J. S. Chang, "IMD of closed-loop filterless class-D amplifiers," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 57, no. 2, pp. 518–527, Feb. 2010.

[13] F. A. Malekzadeh et al., "A new behavioral model for nonlinear analysis of class-D amplifiers for PWM applications," in *Eur. Microw. Integr. Circuits Conf. (EuMIC),* Sep. 27–28, 2010, pp. 138–141.

[14] M. Iwamoto et al., "Band-pass delta sigma class S amplifiers," *Electron. Lett.*, vol. 36, no. 12, pp. 1010–1012, Jun. 8, 2000.

[15] A. Roermund et al., "Extended modeling of time domain convertors," in Proc. *Int. Symp. Circuits Syst. (ISCAS),* May 30–Jun. 2, 2010, pp. 1077–1080.

[16] K. G. Gard, H. M. Gutierrez, and M. B. Steer, "Characterization of spectral regrowth in microwave amplifiers based on the nonlinear transformation of a complex Gaussian process," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 7, pp. 1059–1069, Jul. 1999.

[17] J. C. Pedro and N. B. Carvalho, "On the use of multi-tone techniques for assessing RF components' intermodulation distortion," *IEEE Trans. Microw. Theory Tech.*, vol. 47, pp. 2393–2402, Dec. 1999.

[18][18] T. Johnson et al., "CMOS RF class-D power amplifier with bandpass sigma-delta modulation," *Microelectron. J.,* vol. 38, no. 3, pp. 439–446, Mar. 2007.

[19] IEEE Standard for Information Technology—Telecommunications and Information Exchange Between Systems—Local and Metropolitan Area Networks—Specific Requirements Part Ii: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, *IEEE Standard 802.11g.-2003,* Amendment to IEEE Std 802.11, 1999 Ed.

[20] 3 GPP Standard,, TS 25.101 (V5.2.0), 2002, .

[21] K. M. Gharaibeh, K. G. Gard, and M. B. Steer, "Accurate estimation of digital communication system metrics—SNR, EVM and ρ in a nonlinear amplifier environment," in *Proc. ARFTG Microw. Meas. Conf.*, Fall, 2004, pp. 41–44.

[22] N. M. Blachman, "Zero-crossing rate for the sum of two sinusoids or a signal plus noise," *IEEE Trans. Inf. Theory*, vol. IT-21, no. 6, pp. 671–675, Nov. 1975.

[23] Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High-Speed Physical Layer in the 5 GHz Band, *IEEE Standard 802.11a-1999*, 1999.

[24] M. Li et al., "Accurate multisine representation of digital communication signals for characterization of nonlinear circuits," in *Proc. Radio Wirel. Symp.*, Jan. 2006, pp. 527–530.

[25] iMPT-704-TC multi-purpose tuner [Online]. Available: www.focus-microwaves.com/downFile.php?id=277

[26] W. H. Tranter, K. S. Shanmugan, T. S. Rappaport, and K. L. Kosbar, *Principles of Communication Systems Simulation With Wireless Applications*. Upper Saddle River, NJ: Prentice-Hall, 2004.

[27] M. J. Brusco and S. Stahl, *Branch-and-Bound Applications in Combinatorial Data Analysis (Statistics and Computing)*. New York: Springer, 2005.

[28] I. S. Reed, "On a moment theorem for complex Gaussian processes," *IRE Trans. Inf. Theory*, vol. IT-8, no. 3, pp. 194–195, Apr. 1962.

[29] S. Cannizzaro, G. Palumbo, and S. Pennisi, "Effects of nonlinear feedback in the frequency domain," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 53, no. 2, pp. 225–234, Feb. 2006.

[30] S. C. Li, V. C.-C. Lin, K. Nandhasri, and J. Ngarmnil, "New highefficiency 2.5 V/0.45 W RWDM class-D audio amplifier for portable consumer electronics," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 52, no. 9, pp. 1767–1774, Sep. 2005.

[31] G. T. Zhou, H. Qian, L. Ding, and R. Raich, "On the baseband representation of a bandpass nonlinearity," *IEEE Trans. Signal Process.*, vol. 53, no. 8, pp. 2953–2957, Aug. 2005.

[32] S. Benedetto, E. Biglieri, and R. Daffara, "Modeling and performance evaluation of nonlinear satellite links—A volterra series approach," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-15, no. 4, pp. 494–507, Jul. 1979.

[33] Kavousian, A.; Su, D.K.; Hekmat, M.; Shirvani, A.; Wooley, B.A.; , "A Digitally Modulated Polar CMOS Power Amplifier With a 20-MHz Channel Bandwidth," *Solid-State Circuits, IEEE Journal of* , vol.43, no.10, pp.2251-2258, Oct. 2008.

[34] Staszewski, R.B.; Wallberg, J.L.; Rezeq, S.; Chih-Ming Hung; Eliezer, O.E.; Vemulapalli, S.K.; Fernando, C.; Maggio, K.; Staszewski, R.; Barton, N.; Meng-Chang Lee; Cruise, P.; Entezari, M.; Muhammad, K.; Leipold, D.; , "All-digital PLL and transmitter for mobile phones," Solid-State Circuits, IEEE Journal of , vol.40, no.12, pp. 2469- 2482, Dec. 2005

[35] G. Zames et. al. ,"Dither in Nonlinear Systems", *IEEE Transactions on Automatic Control*, VOL. AC-21, NO. 5, OCTOBER 1976.

[36] Frasca, R.; Iannelli, L.; Vasca, F.; , "Dithered Sliding-Mode Control for Switched Systems," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.53, no.9, pp.872-876, Sept. 2006.

[37] S. Mossaheb, "Application of a method of averaging to the study of dither in nonlinear systems," *Int. J. Contr.*, vol. 38, no. 3, pp. 557–576, 1983.

[38] Malekzadeh, F. A.; Mahmoudi, R.; Roermund, A.; , "Statistical Analysis of Self-Oscillating Power Amplifiers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*

[39] Johnson, T.; Stapleton, S. P.; , "RF Class-D Amplification With Bandpass Sigma–Delta Modulator Drive Signals," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.53, no.12, pp.2507-2520, Dec. 2006.

[40] F. H. Raab, "Maximum Efficiency and Output of Class-F Power Amplifiers", *IEEE Tran. on Microwave Theory and Techniques*, Vol. 49, No. 6, June 2001.

[41] Tsai-Pi Hung et. al. , "Design of high-efficiency current-mode class-D amplifiers for wireless handsets," *Microwave Theory and Techniques, IEEE Transactions on* , Vol.53, no.1, pp. 144- 151, Jan. 2005.

[42] Weisstein, Eric W. "Frobenius Equation." From MathWorld [Online]: http://mathworld.wolfram.com/FrobeniusEquation.html.

[43] Simon Cimin Li et al., "New High-Efficiency 2.5 V/0.45 W RWDM Class-DAudio Amplifier for Portable Consumer Electronics New High-Efficiency 2.5 V/0.45 W RWDM Class-DAudio Amplifier for Portable Consumer Electronics", *IEEE Tran. On Circuits and Systems I*, 2005.

[44] S. O. Rice, "Statistical properties of a sine wave plus random noise," *Bell Syst. Tech. J.,* vol. 27, pp. 109-157, eq.(2.8), Jan. 1948.

[45] Johnson, T.; Stapleton, S. P., "RF Class-D Amplification With Bandpass Sigma–Delta Modulator Drive Signals," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.53, no.12, pp.2507-2520, Dec. 2006.

[46]Shaharuddin Salleh, et. al. *Computing for Numerical Methods Using Visual C++,* ISBN:0470127953 9780470127957.

[47] Sarkeshi, M et. al. "Accurate determination of switching loss in class-D power amplifiers with random Gaussian excitation using Rice Formula," *Power Amplifiers for Wireless and Radio Applications (PAWR)*, 2011 IEEE Topical Conference on.

[48] Anthony Lawrence Long, *High Frequency Current Mode Class-D Amplifiers With High Output Power and Efficiency,* M.Sc. Thesis, Department of Electrical and Computer Engineering University of California, Santa Barbara, CA 93106-9560 May 2003.

[49] El-Hamamsy, S.-A.; , "Design of high-efficiency RF Class-D power amplifier," *Power Electronics, IEEE Transactions on* , vol.9, no.3, pp.297-308, May 1994.

[50] Arfaei Malekzadeh, F., Mahmoudi, R. & Roermund, A.H.M. van (2011). Fine Tuning of Switching Frequency for Minimal Distortion High Frequency PWM Systems. *IEEE MTT-S International Microwave Symposium*, 5-10 June 2011, Baltimore, USA.

[51] Tsai-Pi Hung; Metzger, A.G.; Zampardi, P.J.; Iwamoto, M.; Asbeck, P.M.; , "Design of high-efficiency current-mode class-D amplifiers for wireless handsets," *Microwave Theory and Techniques, IEEE Transactions on* , vol.53, no.1, pp. 144- 151, Jan. 2005.

[52] Frebrowski, D.; Boumaiza, S.; , "Inverse class F power amplifier in push-pull configuration," *Signals, Circuits and Systems (SCS), 3rd International Conference on* , vol., no., pp.1-4, 6-8 Nov. 2009.

[53] Qureshi, J.H.; Pelk, M.J.; Marchetti, M.; Neo, W.C.E.; Gajadharsing, J.R.; van der Heijden, M.P.; de Vreede, L.C.N.; , "A 90-W Peak Power GaN Outphasing Amplifier With Optimum Input Signal Conditioning," *Microwave Theory and Techniques, IEEE Transactions on* , vol.57, no.8, pp.1925-1935, Aug. 2009.

[54] F. A. Malekzadeh, Arthur van Roermund, Reza Mahmoudi, "Low Frequency dithering technique for high performance transmitters", *U.S. Patent US 51/575,181*, 8 May 2011.

[55] Jan Verspecht, *Describing Functions Can Better Model Hard Nonlinearities In The Frequency Domain Than The Volterra Theory*, Annex to Doctoral Dissertation - Vrije Universiteit Brussel, November 1995

[56][55] Frans Verbeyst and Marc Vanden Bossche, "The Volterra Input-Output Map of a High Frequency Amplifier as a Practical Alternative to Load-Pull Measurements", *IEEE Transactions on Instrumentation and Measurement*, Vol. 44, No. 3, June 1995.

[57] Vahe A. Caliskan et.al., "Multifrequency Averaging of DC/DC Converters:, *IEEE Transactions on Instrumentation and Measurement*, Vol. 44, No. 3, June 1995.

[58] J. Madhavi, E. Emandi, M. D. Bellar, and M. Ehsani, "Analysis of power electronics converters using the generalized state-space averaging approach," IEEE Trans. Circuits Syst. I, vol. 44, pp. 767–770, Aug. 1997.

[59] J. Webster (ed.), Wiley Encyclopedia of Electrical and Electronics Engineering 1999 John Wiley & Sons, Inc.

[60] D. P. Atherton, Nonlinear Control Engineering, Van Nostrand Reinhold Co., London &
[61]New York; full edition 1975, student edition 1982.

[62] D. P. Atherton, Stability of Nonlinear Systems. Research Studies Press (Wiley), Chichester, 1981.

[63] I. E. Kazakov, "Generalization of the method of statistical linearization to multidimensional systems", *Avtomatika i Telemekhanika*, 26, pp. 1210-1215, 1965.

[64] J. H. Taylor, "An Algorithmic State-Space/Describing Function Technique for Limit Cycle Analysis", IFAC *Symposium on Multivariable Technological Systems*, Fredericton, NB, Canada, July 1977.

[65] D. N. Hannebrink, H. S. Lee, H. Weinstock, and J. K. Hedrick, "Influence of axle load, track gauge, and wheel profile on rail vehicle hunting", *Trans. ASME - J. Eng.* Ind. pp. 186-195, 1977.

[66] Charles A. Desoer, M. Vidyasagar, *Feedback systems: Input-output properties*, Academic Press, 1975 - Technology & Engineering.

[67] Iannelli, L.; Johansson, K.H.; Jonsson, U.T.; Vasca, F.; , "Dither for smoothing relay feedback systems," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , vol.50, no.8, pp. 1025- 1035, Aug. 2003.

[68] A. Gelb R. S. Warren, Direct statistical analysis of nonlinear systems: CADET, AIAA J., 11 (5): 689–694, 1973.

[69] J. L. Doob, *Stochastic Process*. New York: Wiley, 1953.

[70] A. Papoulis, Probability, Random Variables and Stochastic Processes, 3rd. Ed. McGraw-Hill Inc., 1991.

[71] F. Arfaei Malekzadeh et.al., "Low frequency dithering technique for highly efficient and linear transmitters", submitted to *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*.

[72] Sarkeshi, M., et.al. "Efficiency Analysis of a Limit-Cycle Class-D Amplifier with a Random Gaussian Excitation", *IMS 2009*.

[73] Arfaei Malekzadeh, F., et.al. "A new behavioral model for nonlinear analysis of class-D amplifiers for PWM Applications" *Proceeding of EuMW2010, 26 September - 1 October 2010, Paris, France.*

[74] Arfaei Malekzadeh, F., Mahmoudi, R. & Roermund, A.H.M. van (2009) "A new approach for nonlinear metric estimation of limit cycle amplifiers" *Proceeding of EuMW 2009, European Microwave Week*, 28 September-2 October 2009, Rome, Italy. (pp. 1-4).

[75] Matthew Herman, Benjamin Miller, Joel Goodman, "Efficient Multidimensional Polynomial Filtering for Nonlinear Digital Predistortion", *HPEC Workshop 2008*, 23 September 2008.

[76] Bolstad, A.; Miller, B.A.; Goodman, J.; Vian, J.; Kalyanam, J.; , "Identification and compensation of Wiener-Hammerstein systems with feedback," *Acoustics, Speech and Signal Processing (ICASSP), 2011 IEEE International Conference on* , vol., no., pp.4056-4059, 22-27 May 2011.

[77] Mkadem, F.; Boumaiza, S.; , "Extended Hammerstein Behavioral Model Using Artificial Neural Networks," *Microwave Theory and Techniques, IEEE Transactions on* , vol.57, no.4, pp.745-751, April 2009.

[78] By Frederick H. Raab et. al., "RF and Microwave Power Amplifier and Transmitter Technologies", *High Frequency Electronics*, 2003.

[79] Pintelon, R.; Vandersteen, G.; Schoukens, J.; Rolain, Y.; , "Fast FRF measurement of multivariable systems using periodic excitations," *Instrumentation and Measurement Technology Conference (I2MTC), 2011 IEEE* , vol., no., pp.1-6, 10-12 May 2011.

[80] T. Piessens, M. Steyaert, "Oscillator Pulling and Synchronization Issues in Self-Oscillating Class-D Power Amplifiers", *Proceedings of the 29th European Solid State Circuits Conference*, Sept. 2003.

[81] F. H. Raab, "Radio frequency pulse-width modulation," *IEEE Trans. Commun.*, vol. COMM-21, no. 8, pp. 958–966, Aug. 1973.

[82] Kobayashi, H.; Hinrichs, J.M.; and Asbeck, P.M. "Current-Mode Class-D Power Amplifiers for High-efficiency RF Applications", *IEEE Trans. Microwave theory and Techniques*, vol. 49, NO.12, pp. 2480-2485, December 2001.

[83] Chowdhury, D.; Thyagarajan, S.V.; Lu Ye; Alon, E.; Niknejad, A.M.; , "A fully-integrated efficient CMOS inverse Class-D power amplifier for digital polar transmitters," *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011 IEEE , vol., no., pp.1-4, 5-7 June 2011.

[84] Yu-hua Cheng et.al., "Third harmonic distortion calculation of a self-oscillating power amplifier", *Journal of Zhejiang University*, 2011.

[85] Odavic, M.; Sumner, M.; Zanchetta, P.; Clare, J.C.; , "A Theoretical Analysis of the Harmonic Content of PWM Waveforms for Multiple-Frequency Modulators," *Power Electronics, IEEE Transactions on* , vol.25, no.1, pp.131-141, Jan. 2010

[86] Roza, E.; , "Analog-to-digital conversion via duty-cycle modulation," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on ,* vol.44, no.11, pp.907-914, Nov 1997.

[87] TS 25.101 (V5.2.0), 3GPP Standard, 2002.

[88] Gharaibeh, K.M.; Gard, K.G.; Steer, M.B.; , "In-band distortion of multisines," *Microwave Theory and Techniques, IEEE Transactions on* , vol.54, no.8, pp.3227-3236, Aug. 2006.

[89] Palumbo, G.; Pennisi, S.; , "High-frequency harmonic distortion in feedback amplifiers: analysis and applications," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on* , vol.50, no.3, pp. 328- 340, Mar 2003.

[90] Mathews, V.J.; , "Adaptive Volterra filters using orthogonal structures," *Signal Processing Letters, IEEE* , vol.3, no.12, pp.307-309, Dec 1996.

[91] Maas, S.A.; , "Volterra analysis of spectral regrowth," *Microwave and Guided Wave Letters, IEEE* , vol.7, no.7, pp.192-193, Jul 1997

[92] Wei Cheng, Anne-Johan Annema, Jeroen A. Croon, Bram Nauta: Noise and Nonlinearity Modeling of Active Mixers for Fast and Accurate Estimation. *IEEE Trans. on Circuits and Systems* 58-I(2): 276-289 (2011)

[93] Terrovitis, M.T.; Meyer, R.G.; , "Intermodulation distortion in current-commutating CMOS mixers," *Solid-State Circuits, IEEE Journal of* , vol.35, no.10, pp.1461-1473, Oct 2000.

[94] G. Zames et.al.," Structural Stabilization and Quenching by Dither in Nonlinear Systems", *IEEE Transactions on Automatic Control,* Vol. AC-22, No. 3, June 1977.

[95] J.J. Bussgang,"Cross-correlation function of amplitude-distorted Gaussian signals", *Res. Lab. Elec., Mas. Inst. Technol., Cambridge MA*, Tech. Rep. 216, March 1952.

[96] Lopez, J.; Yan Li; Popp, J.D.; Lie, D.Y.C.; Chia-Chang Chuang; Chen, K.; Wu, S.; Tzu-Yin Yang; Gin-Kou Ma; , "Design of Highly Efficient Wideband RF Polar Transmitters Using the Envelope-Tracking Technique," *Solid-State Circuits, IEEE Journal of* , vol.44, no.9, pp.2276-2294, Sept. 2009.

[97] Perreault, D.J.; , "A New Power Combining and Outphasing Modulation System for High-Efficiency Power Amplification," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.58, no.8, pp.1713-1726, Aug. 2011

[98] William C. Farmer (1945). Ordnance Field Guide: Restricted. Military service publishing company.

[99] Granino Arthur Korn and Theresa M. Korn (1952). Electronic Analog Computers: (d-c Analog Computers). McGraw-Hill.

[100] Lawrence G. Roberts, *Picture Coding Using Pseudo-Random Noise*, MIT, S.M. thesis, 1961 online: http://www.packet.cc/files/pic-code-noise.html

[101] Schuchman "Dither Signal and Their Effect on Quantization Noise", *IEEE Trans. Communications* 12(4): 162-165. doi:10.1109/TCOM.1964.1088973.

[102] Wagdy, M.F. , "Effect of additive dither on the resolution of ADC's with single-bit or multibit errors," *Instrumentation and Measurement, IEEE Transactions on* , vol.45, no.2, pp.610-615, Apr 1996.

[103] Wagdy, M.F.; Goff, M.; , "Linearizing average transfer characteristics of ideal ADC's via analog and digital dither," *Instrumentation and Measurement, IEEE Transactions on* , vol.43, no.2, pp.146-150, Apr 1994.

[104]Stephen A. Maas, "*Nonlinear Microwave and RF Circuits*", Second Edition, ISBN 978-1-58053-611-0, Copyright 2003.

[105] Kenneth S. Kundert, Jacob K. White, and Alberto Sangiovanni-Vincentelli. *Steady-State Methods for Simulating Analog And Microwave Circuits*. Kluwer Academic Publishers, Boston, 1990.

[106] Albert Garcia i Tormo et.al. ,"Fundamental Modulation Limits for Minimum Switching Frequency Inband-Error-Free High-Efficiency Power Amplifiers", *Circuits and Systems I: Regular Papers, IEEE Transactions on*, Oct. 2011.

[107] Shouhei Kousai et. al." An Octave-Range, Watt-Level, Fully-Integrated CMOS switching Power Mixer Array for Linearization and Back-Off-Efficiency Improvement", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 44, NO. 12, DECEMBER 2009

[108] A. Kavousian, D. Su and B Wooley, "A Digitally Modulated Polar CMOS PA with 20MHz Signal BW", *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb. 2007.

[109] Raab, F.H.; , "High-efficiency linear amplification by dynamic load modulation," *Microwave Symposium Digest, 2003 IEEE MTT-S International* , vol.3, no., pp. 1717-1720 vol.3, 8-13 June 2003.

[110] Ken C. Pohlmann (2005). *Principles of Digital Audio*. McGraw-Hill Professional. ISBN 0071441565.

Publications

Journals

1. Statistical Analysis of Self Oscillating Power Amplifiers, published in *IEEE transactions on Circuits and Systems I, 2011.*
2. Low Frequency Dithering for Highly Efficient and Linear Transmitters, submitted to *IEEE transactions on Microwave Theory and Techniques (TMTT), 2012.*
3. Multi Frequency Averaging Technique for Nonlinearity Analysis of Switching Mixers, submitted to *on Circuits and Systems I, 2012.*

Conferences

1. Low Frequency Dithering Technique for Linearization of Current mode Class D amplifiers, *IMS, June 2012, Montreal, Canada.*
2. Fine Tuning of switching frequency for minimal distortion in high frequency PWM systems, *IMS, June 2011, Baltimore, USA.*
3. A New Behavioral Model for Nonlinear Analysis of Class D Amplifiers for PWM Applications, *EUMC 2010, Paris, France*.
4. A New Approach for Nonlinear Metric Estimation of Limit Cycle Amplifiers, *EUMC 2009, Rome, Italy.*
5. Extended Modeling for Time-Encoding Converters, *ISCAS 2010, Special Season, Paris, France.*
6. Analysis of self-oscillating class D amplifiers for random input signals*, PRORISC 2009, Veldhoven, Netherlands.*
7. A New Statistical Approach for Nonlinear Analysis of Limit Cycle Amplifiers*, IRWS 2009, San Diego, California.*
8. The Impact of Nonlinear Distributed Modeling on Transient Performance of Microwave Circuits, *2004 IEEE Mikon Conference, Poland.*
9. A New Nonlinear Distributed Noise Modeling for Millimeter Wave HEMT Oscillator, *APMC, 2004, Korea.*
10. A New Consideration of Correlation between External Noise Sources in HEMT Two Temperature Model, *IEEE AP-S Topical Conference on Wireless Communications Technology, Oct 2003, Hawaii, USA.*

Patent

1. F. A. Malekzadeh, Arthur van Roermund, Reza Mahmoudi, “Low Frequency dithering technique for high performance transmitters”, U.S. Patent, US 51/575,181, 8 May 2011.

Appendices

A.I TSIDF through Fourier integrals

According to definition of Fourier transform, the y, or the output of the nonlinear block versus its input, x, is given versus the following transformation

$$y(x) = \frac{1}{2\pi}\int_{-\infty}^{\infty} Y(ju).\exp(jux)\,du \tag{A.I-1}$$

and replacing x by equation 10, and Fourier expansion of the complex exponential function within the integral, the following frequency independent describing function pairs are achieved:

$$N_A(A,B) = \frac{j}{\pi A}\int_{-\infty}^{\infty} Y(ju)J_0(Bu)J_1(Au)du \tag{A.I-2-a}$$

$$N_B(A,B) = \frac{j}{\pi B}\int_{-\infty}^{\infty} Y(ju)J_0(Au)J_1(Bu)du \tag{A.I-2-b}$$

And the following symmetry always holds:

$$N_A(A,B) = N_B(B,A) \tag{A.I-2-c}$$

The integrals in 18 can be used for SIDF calculation as well, by setting A or B to zero [4].

A.II TSIDF and RSIDF calculation case studies

This is equivalent nonlinearity formulation of the ideal comparator, dithered by amplitude A [69]:

$$g_0(r,A) = \frac{D}{\pi} Sin^{-1}(\frac{r}{A}) \qquad for \qquad |r| \le A \tag{A.II-1}$$

$$= \frac{D}{2}.sgn(r) \qquad Elsewhere$$

$$y$$

And the describing function for a two-step stair case quantizer depicted in Fig. A.II-1 is as follows [4]:

$$N_B(A,B) = \frac{4D}{\pi}\sum_{m=0}^{\infty} \frac{mcos\left(2msin^{-1}\left(\frac{\delta}{B}\right)\right)}{\sqrt{1-\left(\frac{\delta}{B}\right)^2}} \cdot \sum_{n=0}^{\infty} \frac{(-1)^n \Gamma(n+m)}{n!(m-n)!\Gamma(n+1)} \left(\frac{A}{B}\right)^{2n} \quad {}_2F_1\left[-n,-n;2;(\frac{B}{A})^2\right]$$

In which ${}_2F_1$ is a 2-1 hypergeometric function [9].

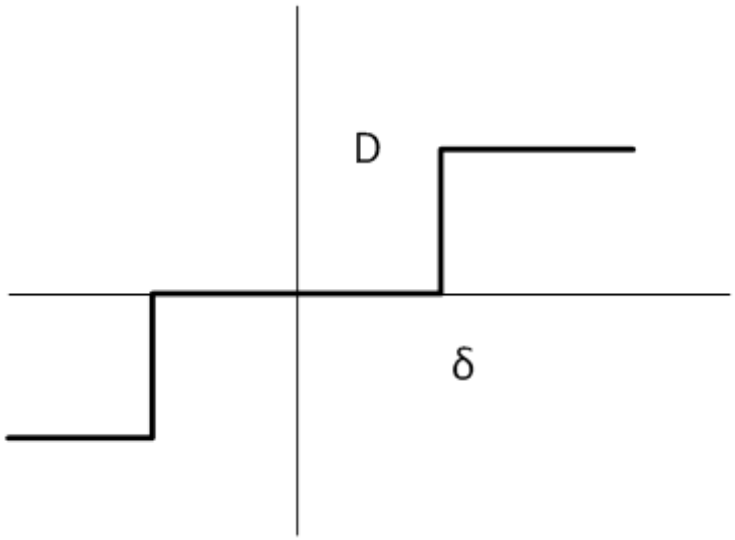


Fig. A.II-1: Two step stair case quantizer characteristics

A.III The coefficients of CMCD

The coefficients u, v and w are as follows [81]:

$$u = \frac{R_{dson}}{R_L} + 0.25 - \sum_{neven} \frac{4n^2}{\pi^2(n^2-1)^2\left[1+(R_{dson}.C_{ds}n\omega_r - \frac{2R_{dson}}{n\omega_r L_x})^2\right]} \quad \text{A.III-1-a}$$

$$v = 0.5\omega_r R_{dson} C_{ds} - \frac{0.5\omega_r}{R_{dson}.L_x} + \omega_r R_{dson} C_p - \frac{R_{dson}}{\omega_r L_y} + \sum_{neven} \frac{4n(2R_{dson}C_{ds}n\omega_r - \frac{2R_{dson}}{n\omega_r L_x})}{\pi^2(n^2-1)^2\left[1+(R_{dson}.C_{ds}n\omega_r - \frac{2R_{dson}}{n\omega_r L_x})^2\right]} \quad \text{A.III-1-b}$$

$$w = -\frac{R_{dson}}{R_L} - 0.25 + \sum_{neven} \frac{4}{\pi^2(n^2-1)^2\left[1+(R_{dson}.C_{ds}n\omega_r - \frac{2R_{dson}}{n\omega_r L_x})^2\right]} \quad \text{A.III-1-c}$$

$$L_x = 0.5L + 2L_{dc} \quad \text{A.III-2}$$

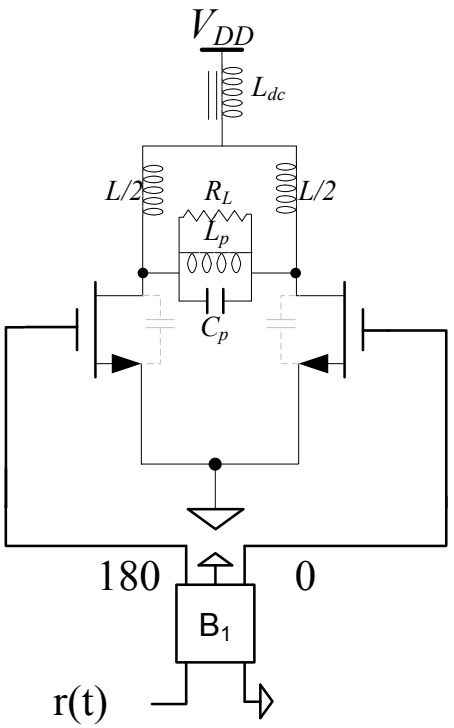


Fig. A.III-1: Schematic diagram of CMCD with even harmonic compensation

$$L_y = L(1 + \frac{0.25}{L_{dc}})$$ A.III-3

The circuit schematic diagram is re-illustrated for convenience in Fig. A.III-1.

A.IV Autocorrelation coefficients for real Gaussian input

The effect of the dithering signal (which is limit cycle in self oscillating structures) on linearization of the CDA can be explained with a new set of coefficients, relating the output of the CDA, resulting from a combination of limit cycle and random input signals to the amplifier.

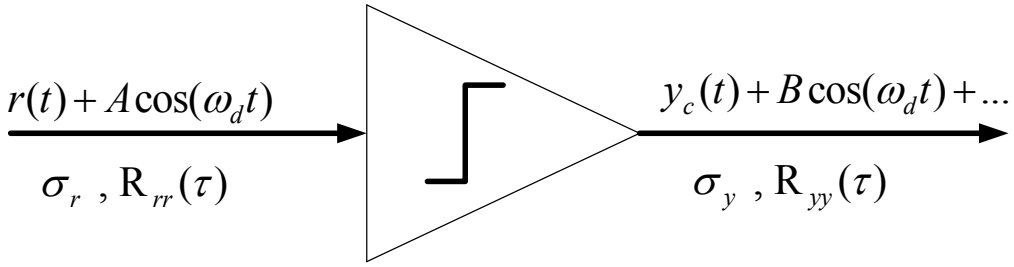


Figure (A.IV-1): The input and output notation for random plus sinusoidal dither excitation.

Figure (A.IV-1) illustrates the notation to describe the nonlinear behavior of the system. The random signal r(t) enters a hard nonlinear component, together with the linearizer signal, and the output consists of correlated signal, a dithering component and the rest is the distortion. Equations (A.IV-1) and (A.IV-2) show the relationship between the input and output autocorrelation functions and the formulation of the coefficients:

$$R_{yy}(\tau)=\sum_{k=1}^{M} c_k^2 R_{rr}^k(\tau) \tag{A.IV-1}$$

$$c_k(A,\sigma_r)=\frac{1}{2\pi\sigma_r\sqrt{2\pi k!}}\int_0^{2\pi} d\theta \int_{-\infty}^{\infty} y(\sigma_r r + A\sin(\theta))\exp(\frac{-r^2}{2})H_k(r)dr \tag{A.IV-2}$$

where $H_k(r)$ is the kth order hermite polynomial [9] and M is the maximum order of the nonlinearity calculated. Equation (A.IV-2) would be reduced to the well known static autocorrelation function relationship for a nonlinearity For A=0. For all of the coefficients, the integral of (8) is reduced to single integral in equation (A.IV-3):

$$c_k(A,\sigma_r)=\frac{D}{{\sigma_r}^k\pi\sqrt{2\pi k!}}\left(\int_{-A/\sigma}^{A/\sigma} H_k(r)e^{-r^2/2}Sin^{-1}(\frac{\sigma r}{A})dr+\pi\exp(-\frac{A^2}{4{\sigma_r}^2})\right) \tag{A.IV-3}$$

Equation (A.IV-1) can be expressed in frequency domain, as a summation of auto-correlations as denoted in equation (A.IV-4):

$$S_{ycyc}(\omega) = \sum_{k=1}^{M} c_k^2 S_{rr}{}^{k*}(\omega) \tag{A.IV-4}$$

Where S_y and S_x are the power spectral densities and k* superscript is the k'th order self-convolution of the operand. Based on equation (A.IV-4), the nonlinear analysis of the structure is reduced to calculation of weighted sum of self convolved spectral densities. The correlation coefficients for third to seventh order distortions, for an ideal limiter are written in equations (A.IV-5-a, b, c):

$$c_3 = \frac{De^{-\frac{A^2}{4\sigma_r{}^2}}}{2\sqrt{3\pi}\sigma_r{}^3}\left(1+\frac{\left(A^2-2\sigma_r{}^2\right)I_0\left(\frac{A^2}{4\sigma_r{}^2}\right)-A^2I_1\left(\frac{A^2}{4\sigma_r{}^2}\right)-2(A^2-\sigma_r{}^2)e^{-\frac{A^2}{4\sigma_r{}^2}}}{2\sigma_r{}^2}\right) \tag{A.IV-5-a}$$

$$c_5 = \frac{De^{-\frac{A^2}{4\sigma_r{}^2}}}{4\sqrt{15\pi}\sigma_r{}^5}\left(1+\frac{\left(A^4-6A^2\sigma_r{}^2+6\sigma_r{}^4\right)I_0\left(\frac{A^2}{4\sigma_r{}^2}\right)-A^2\left(A^2-4\sigma_r{}^2\right)I_1\left(\frac{A^2}{4\sigma_r{}^2}\right)-2\left(A^4-6A^2\sigma_r{}^2+3\sigma_r{}^4\right)e^{-\frac{A^2}{4\sigma_r{}^2}}}{2\sigma_r{}^4}\right) \tag{A.IV-5-b}$$

$$c_7 = \frac{De^{-\frac{A^2}{4\sigma_r{}^2}}}{12\sqrt{70\pi}\sigma_r{}^7}\left(1+\frac{\left(A^6-14A^4\sigma_r{}^2+45A^2\sigma_r{}^4-30\sigma_r{}^6\right)I_0\left(\frac{A^2}{4\sigma_r{}^2}\right)-A^2\left(A^4-12A^2\sigma_r{}^2+23\sigma_r{}^4\right)I_1\left(\frac{A^2}{4\sigma_r{}^2}\right)}{2\sigma_r{}^6}+\frac{(-2A^6+30A^4\sigma_r{}^2-90A^2\sigma_r{}^4+30\sigma_r{}^6)e^{-\frac{A^2}{4\sigma_r{}^2}}}{2\sigma_r{}^6}\right) \tag{A.IV-5-c}$$

In which I_0 and I_1 are modified Bessel functions of the first kind.

A.V Mixer gain with MFA method

A special case is of importance, when the i_D current is only a function of v_{GS}. This can either happen when the source voltage swing is negligible or the channel length modulation is insignificant, which is the case for long-channel process technologies. In such occasions, solution of A.V-1-a, will result in a closed form analytical solution. The solution is expressed in equation A.V-7-(a, b, c).

$$P = ((A_{LO}^2 A_{RF}^2 R_L^2((R_L^2(1.p_2 + 3.p_3 V_{G0} - 3.p_3 V_{S0} + p_4(0.375A_{LO}^2 + 1.5A_{RF}^2 + 6.V_{G0}^2 + 6.V_{S0}^2 - 12.V_{G0}V_{S0}))\omega_r^2 C_{gd}^3 + C_L R_L^2(3.p_2 + 9.p_3 V_{G0} - 9.p_3 V_{S0} + p_4(1.125A_{LO}^2 + 4.5A_{RF}^2 + 18.V_{G0}^2 + 18.V_{S0}^2 - 36.V_{G0}V_{S0}))\omega_r^2 C_{gd}^2 + (p_4(1.125C_L^2 R_L^2 \omega_r^2 + 0.0234375)A_{LO}^2 + 0.375p_4 V_{G0}^2 + 0.375p_4 V_{S0}^2 + 4.5A_{RF}^2 C_L^2 p_4 R_L^2 \omega_r^2 + 18.C_L^2 p_4 R_L^2 V_{G0}^2 \omega_r^2 + 18.C_L^2 p_4 R_L^2 V_{S0}^2 \omega_r^2 + 9.C_L^2 p_3 R_L^2 V_{G0} \omega_r^2 - 9.C_L^2 p_3 R_L^2 V_{S0} \omega_r^2 - 36.C_L^2 p_4 R_L^2 V_{G0} V_{S0} \omega_r^2 + 0.09375A_{RF}^2 p_4 + 0.1875p_3 V_{G0} - 0.1875p_3 V_{S0} - 0.75p_4 V_{G0} V_{S0} + p_2(3.C_L^2 R_L^2 \omega_r^2 + 0.0625))C_{gd} + C_L(p_4(0.375C_L^2 R_L^2 \omega_r^2 + 0.0234375)A_{LO}^2 + 0.375p_4 V_{G0}^2 + 0.375p_4 V_{S0}^2 + 1.5A_{RF}^2 C_L^2 p_4 R_L^2 \omega_r^2 + 6.C_L^2 p_4 R_L^2 V_{G0}^2 \omega_r^2 + 6.C_L^2 p_4 R_L^2 V_{S0}^2 \omega_r^2 + 3.C_L^2 p_3 R_L^2 V_{G0} \omega_r^2 - 3.C_L^2 p_3 R_L^2 V_{S0} \omega_r^2 - 12.C_L^2 p_4 R_L^2 V_{G0} V_{S0} \omega_r^2 + 0.09375A_{RF}^2 p_4 + 0.1875p_3 V_{G0} - 0.1875p_3 V_{S0} - 0.75p_4 V_{G0} V_{S0} + p_2(1.C_L^2 R_L^2 \omega_r^2 + 0.0625)))^2 + R_L^2 \omega_r^2 (R_L^2(2.p_2 + 6.p_3 V_{G0} - 6.p_3 V_{S0} + p_4(0.75A_{LO}^2 + 3.A_{RF}^2 + 12.V_{G0}^2 + 12.V_{S0}^2 - 24.V_{G0}V_{S0}))\omega_r^2 C_{gd}^4 + C_L R_L^2(8.p_2 + 24.p_3 V_{G0} - 24.p_3 V_{S0} + p_4(3.A_{LO}^2 + 12.A_{RF}^2 + 48.V_{G0}^2 + 48.V_{S0}^2 - 96.V_{G0}V_{S0}))\omega_r^2 C_{gd}^3 + (p_4(4.5C_L^2 R_L^2 \omega_r^2 + 0.046875)A_{LO}^2 + 0.75p_4 V_{G0}^2 + 0.75p_4 V_{S0}^2 + 18.A_{RF}^2 C_L^2 p_4 R_L^2 \omega_r^2 + 72.C_L^2 p_4 R_L^2 V_{G0}^2 \omega_r^2 + 72.C_L^2 p_4 R_L^2 V_{S0}^2 \omega_r^2 + 36.C_L^2 p_3 R_L^2 V_{G0} \omega_r^2 - 36.C_L^2 p_3 R_L^2 V_{S0} \omega_r^2 - 144.C_L^2 p_4 R_L^2 V_{G0} V_{S0} \omega_r^2 + 0.1875A_{RF}^2 p_4 + 0.375p_3 V_{G0} - 0.375p_3 V_{S0} - 1.5p_4 V_{G0} V_{S0} + p_2(12.C_L^2 R_L^2 \omega_r^2 + 0.125))C_{gd}^2 + C_L(p_4(3.C_L^2 R_L^2 \omega_r^2 + 0.09375)A_{LO}^2 + 1.5p_4 V_{G0}^2 + 1.5p_4 V_{S0}^2 + 12.A_{RF}^2 C_L^2 p_4 R_L^2 \omega_r^2 + 48.C_L^2 p_4 R_L^2 V_{G0}^2 \omega_r^2 + 48.C_L^2 p_4 R_L^2 V_{S0}^2 \omega_r^2 + 24.C_L^2 p_3 R_L^2 V_{G0} \omega_r^2 - 24.C_L^2 p_3 R_L^2 V_{S0} \omega_r^2 - 96.C_L^2 p_4 R_L^2 V_{G0} V_{S0} \omega_r^2 + 0.375A_{RF}^2 p_4 + 0.75p_3 V_{G0} - 0.75p_3 V_{S0} - 3.p_4 V_{G0} V_{S0} + p_2(8.C_L^2 R_L^2 \omega_r^2 + 0.25))C_{gd} + C_L^2(p_4(0.75C_L^2 R_L^2 \omega_r^2 + 0.046875)A_{LO}^2 + 0.75p_4 V_{G0}^2 + 0.75p_4 V_{S0}^2 + 3.A_{RF}^2 C_L^2 p_4 R_L^2 \omega_r^2 + 12.C_L^2 p_4 R_L^2 V_{G0}^2 \omega_r^2 + 12.C_L^2 p_4 R_L^2 V_{S0}^2 \omega_r^2 + 6.C_L^2 p_3 R_L^2 V_{G0} \omega_r^2 - 6.C_L^2 p_3 R_L^2 V_{S0} \omega_r^2 - 24.C_L^2 p_4 R_L^2 V_{G0} V_{S0} \omega_r^2 + 0.1875A_{RF}^2 p_4 + 0.375p_3 V_{G0} - 0.375p_3 V_{S0} - 1.5p_4 V_{G0} V_{S0} + p_2(2.C_L^2 R_L^2 \omega_r^2 + 0.125)))^2)) \quad \text{A.V-7-a}$$

$$Q = ((4.C_{gd}^5 + 20.C_L C_{gd}^4 + 40.C_L^2 C_{gd}^3 + 40.C_L^3 C_{gd}^2 + 20.C_L^4 C_{gd} + 4.C_L^5)R_L^4 \omega_r^4 + (1.25C_{gd}^3 + 3.75C_L C_{gd}^2 + 3.75C_L^2 C_{gd} + 1.25C_L^3)R_L^2 \omega_r^2 + 0.0625C_{gd} + 0.0625C_L)^2 \quad \text{A.V-7-b}$$

$$Gain = \sqrt{\frac{2P}{Q}}.(\frac{1}{A_{LO}}) \quad \text{A.V-7-c}$$

In which R_L and C_L are the load (current buffer) input equivalent resistance and capacitance and p_0 to p_4 are the coefficient of the fourth order polynomial curve fit for i_D versus v_{GS}, in ascending order. The achieved gain is plotted versus the RF amplitude, for a designed mixer in 60GHz. In order to be able to neglect the channel modulation, drain voltage was modulated according to RF input amplitude.

A.VI Supply tracking and linearity

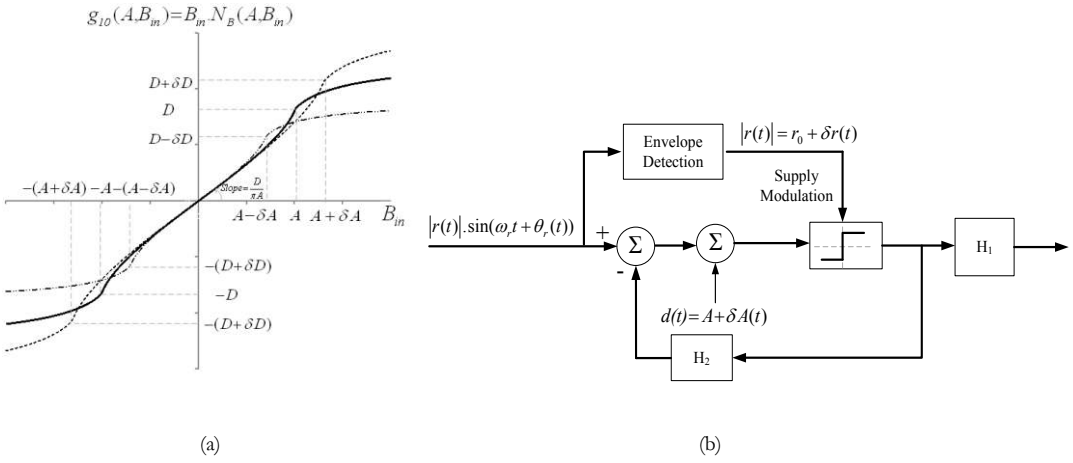
Supply tracking can be utilized to improve the average efficiency for non-constant envelope signals. In order to keep the dithered gain constant, it is necessary to track the dither signal dynamically along with the input signal and supply variations. Fig. A.VI-1 -(a) shows the variations in the sinusoidal dithered gain of an ideal limiter, versus variations in the supply voltage and the dither sinusoid simultaneously. After injection of the dither sinusoid signal, the slope gain of the smoothed characteristic at the origin is:

$$slope\ gain = \frac{d}{dB}\left(g_0(B,A)\right)\Big|_{B=0} = \frac{D}{\pi A}.$$

And the condition for constant gain is as follows:

$$\frac{D}{A} = \frac{D+\delta D}{A+\delta A} = \frac{\delta D}{\delta A} \tag{A.VI-1}$$

Equation (A.VI-1) is the sufficient condition for constant small signal gain of the dithered amplifier. Therefore both dither and supply voltage need to be modulated with the same index in order to preserve linearity.



(a) (b)

Fig. A.VI-1 (a): Keeping the describing function slope-gain constant with envelope modulation, with a dithering injected to an ideal relay (b): Dynamic dithering scheme for improved linearity-efficiency compromise.

Summary

The current research project is about investigation of new methods and techniques to be able to utilize the switched mode amplifiers, for linear and efficient applications. Switched mode amplifiers benefit from low overlap between the current and voltage wave forms in their output terminals, but they seriously suffer from nonlinearity. This makes it impossible to use them to amplify non-constant envelope message signals, where very high linearity is expected.

In order to do that, dithering techniques are studied and a full linearity analysis approach is developed, by which the linearity performance of the dithered amplifier can be analyzed, based on the dithering level and frequency. The approach was based on orthogonalization of the equivalent nonlinearity and is capable of prediction of both co-channel and adjacent channel nonlinearity metrics, for a Gaussian complex or real input random signal.

Behavioral switched mode amplifier models are studied and new models are developed, which can be utilized to predict the nonlinear performance of the dithered power amplifier, including the nonlinear capacitors effects.

For HFD application, self-oscillating and asynchronous sigma delta techniques are currently used, as pulse with modulators (PWM), to encode a generic RF message signal, on the duty cycle of an output pulse train. The proposed models and analysis techniques were applied to this architecture in the first phase, and the method was validated with measurement on a prototype sample, realized in 65 nm TSMC CMOS technology.

Afterwards, based on the same dithering phenomenon, a new linearization technique was proposed, which linearizes the switched mode class D amplifier, and at the same time can reduce the reactive power loss of the amplifier. This method is based on the dithering of the switched mode amplifier with frequencies lower than the band-pass message signal and is called low frequency dithering (LFD). To test this new technique, two test circuits were realized and the idea was applied to them. Both of the circuits were of the hard nonlinear type (class D) and are integrated CMOS and discrete LDMOS technologies respectively. The idea was successfully tested on both test circuits and all of the linearity metric predictions for a digitally modulated RF signal and a random signal were compared to the measurements. Moreover a search method to find the optimum dither frequency was proposed and validated.

Finally, inspired by averaging interpretation of the dithering phenomenon, three new topologies were proposed, which are namely DLM, RF-ADC and area modulation power combining, which are all nonlinear systems linearized with dithering techniques. A new averaging method

was developed and used for analysis of a Gilbert cell mixer topology, which resulted in a closed form relationship for the conversion gain, for long channel devices.

Samenvatting

Het huidige onderzoek gaat over onderzoek naar nieuwe methoden en technieken om te kunnen de geschakelde versterkers gebruiken, voor lineaire en efficiënte toepassingen. Geschakelde versterkers profiteren van de lage overlap tussen de stroom en de spanning golfvormen in hun uitgangen, maar ze serieus last van niet-lineariteit. Dit maakt het onmogelijk om ze te gebruiken om niet-constante enveloppe boodschap signalen, waar zeer hoge lineariteit wordt verwacht versterken.

Om dat te doen, zijn dithering technieken bestudeerd en een volledige analyse lineariteit aanpak is ontwikkeld, waardoor de lineariteit prestaties van de gerasterd versterker kan worden geanalyseerd, op basis van de dithering niveau en de frequentie. De aanpak was gebaseerd op orthogonalisatie van de equivalente niet-lineariteit en is in staat de voorspelling van zowel de co-channel en de aangrenzende kanaal niet-lineariteit metrics, voor een Gaussian complex of daadwerkelijk een inbreng willekeurig signaal.

Behavioral geschakelde versterker modellen zijn bestudeerd en nieuwe modellen worden ontwikkeld, die kunnen worden gebruikt om de niet-lineaire prestaties van de gerasterd eindversterker, inclusief de niet-lineaire condensatoren effecten te voorspellen.

Voor de toepassing HFD, zijn zelf-oscillerende en asynchrone sigma delta momenteel gebruikte technieken, zoals puls met modulatoren (PWM), om een generieke RF-signaal bericht coderen, op de duty cycle van een uitgangspuls trein. De voorgestelde modellen en analyse technieken werden toegepast om deze architectuur in de eerste fase, en de methode is gevalideerd met metingen aan een prototype steekproef, uitgevoerd in 65 nm TSMC CMOS technologie.

Daarna, gebaseerd op dezelfde dithering fenomeen, was een nieuwe linearisatie techniek voorgesteld, die linearizes de geschakelde klasse D-versterker, en tegelijkertijd kan het reactief vermogen verlies van de versterker te verminderen. Deze methode is gebaseerd op de dithering van de geschakelde versterker met frequenties lager dan de band-pass-bericht signaal en wordt genoemd een lage frequentie rasteren (LFD). Voor het testen van deze nieuwe techniek, werden twee test circuits gerealiseerd en het idee was op hen van toepassing. Zowel van de circuits waren van de harde niet-lineaire type (klasse D), en zijn CMOS en discrete LDMOS de respectievelijke technologieën. Het idee is succesvol getest op zowel de te testen circuits en alle van de lineariteit metrische voorspellingen voor een digitaal gemoduleerde RF-

signaal en een willekeurig signaal werden vergeleken met de metingen. Bovendien is een zoekmethode om de optimale dither frequentie te vinden was voorgesteld en gevalideerd.

Tot slot, geïnspireerd door het gemiddelde interpretatie van de dithering fenomeen, drie nieuwe topologieën werden voorgesteld, die voornamelijk worden DLM, RF-ADC en de oppervlakte modulatie kracht te combineren, die allemaal niet-lineaire systemen gelineariseerd met dithering technieken. Een nieuwe gemiddelde methode werd ontwikkeld en gebruikt voor de analyse van een Gilbert cell mixer topologie, wat resulteerde in een gesloten vorm relatie voor de conversie te krijgen, voor lange kanaal apparaten.

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Curriculum vitae

Foad Arfaei Malekzadeh was born in Tehran, Iran in 1979. He received the M.Sc. degree in high frequency electronics from Tehran Polytechnic University, Iran, in 2003 with a thesis entitled "Distributed Nonlinear Modeling of HEMT Oscillator in Ka band." He joined the MSM group of Eindhoven University of Technology, in the Netherlands, as a PhD candidate, in 2008. He has been involved in several industrial RF projects including base station transceiver design and RFID systems as an RF engineer before starting his PhD. He is now involved in a Postdoctoral Fellowship program with University of Waterloo in Ontario, Canada.