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# Analog Fault Diagnosis Based on Ramping Power Supply Current Signature Clusters

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**Abstract**—Measurement of power supply currents was found to be very useful for testing CMOS IC's because of its potential to detect a large class of manufacturing defects. However, this technique was used mainly for fault detection and was confined to digital circuits. In this paper, we present a suited methodology for fault diagnosis of analog circuits based on the observation of power supply currents. In the proposed technique, fault signature dictionaries are generated from the currents in the power supply bus. To obtain signatures rich in information for efficient diagnosis, the transistors in the circuit are forced to operate in all possible regions of operation by using a ramp signal at the supply instead of the conventional constant dc signal or ground voltage. The signatures are then clustered into different groups using a Kohonen neural network classifier. This technique has the potential to detect and diagnose single and multiple shorts as well as open circuits. The theoretical and experimental results of the proposed technique are verified using a CMOS Operational Transconductance Amplifier (OTA) circuit.

## I. INTRODUCTION

**F**AULT diagnosis of analog circuits has been a major field of interest for research in the past two decades. Although analog circuits came into being long before the advent of digital circuits, analog fault diagnosis techniques are still modest as compared to the advances in the digital domain. One important reason for this dramatic advancement in the digital domain is the ability to model a large number of faults with the stuck-at-0 or stuck-at-1 models [1], [2]. For analog circuits and systems, fault diagnosis techniques [3]–[5] are more complex when compared to their counterpart parts in digital circuits for various reasons: i) The requirement of measurements of current and voltage signals at internal nodes [6], ii) Diagnosis errors caused by soft-faults which are due to the tolerance of the components, and iii) The additional cost of increased silicon area for built-in-self-test techniques [7]. In the past, the lack of good transistor models was a severe problem. Fortunately, new advances have been made to create more accurate and versatile models [33], [34]. Hence, a new methodology that overcomes most of these limitations that can and still remain simple and easy to use, is needed.

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Measurement of power supply currents was found to be very useful for testing CMOS IC's because of its potential to detect a large class of manufacturing defects [8]–[10]. The power supply nodes are the universal nodes of any circuit in the sense that they are always accessible and provide the necessary bias currents for all the elements in the circuits. As the distribution of the bias currents will be altered upon the occurrence of a faulty condition in the circuit, observing the power supply currents can be fruitful. In digital circuits, current testing has emerged as a very useful tool in detecting delay faults and other process defects which cannot be modeled by the traditional stuck-at models. These techniques basically rely on the fact that, in digital circuits, under nominal conditions, there is little or no current through  $V_{dd}$  or GND terminals of the circuit. If appropriate input vectors are given, any deviations from this nominal behavior results in the flow of abnormal currents which can be used to detect the presence of a fault [11].

However, the supply current monitoring technique has found no practical applications in analog circuits [31]. The concept of " $I_{ddq}$  monitoring" has already been extended to the analog and mixed analog/digital fields [3], [35], [36]. However, because fault behaviors are not as pronounced as those in the digital case, special test vectors often have to be applied to increase fault coverage, in a special test mode, except for the technique presented in [36]. To apply the power supply current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques. This is because of two factors: i) the emphasis here is on fault diagnosis which requires more than a simple observation of abnormal currents and ii) unlike digital circuits, bias currents always exist between the power supplies in analog circuits and in most cases abnormal currents cannot be defined.

The application of a ramp signal at the power supply nodes instead of the conventional step (or dc voltage) can potentially make the majority of the transistors in the circuit operate in all the regions of operation, namely cutoff, weak inversion, linear and saturation, and hence, provides bias currents rich in information. Once the signatures are generated from these current responses, the fault clustering approach presented in [12] and [13] is used to create the fault dictionary. As the occurrence of short (single or multiple) or open circuits can drastically change the amount of current and its flow in the power supply bus, this technique can successfully diagnose opens and multiple faults as well.

In addition to the novelty offered by the proposed technique, it also overcomes most of the limitations of the existing analog fault diagnosis techniques. This technique is independent of the linearity or nonlinearity of the system, circuit or component. The vector mapping capability of the neural network helps in taking care of the process parameter drifts and component tolerance effects in this approach. A brief description of the Kohonen network and its pattern classification capabilities are given in the appendix. More details about the training algorithm and its features can be found in [14] and [15].

Section II gives a brief description of the current testing in digital circuits and discusses the requirements of analog fault diagnosis based on supply current measurements. Section III proposes the application of a ramp signal at the power supply and presents a detailed description of the theory involved. The proposed fault diagnosis procedure is given in Section IV and the practical aspects of the technique are verified in Section V. The features of this technique are presented in Section VI, and finally, conclusions are given in Section VII.

## II. REQUIREMENTS OF ANALOG FAULT DIAGNOSIS

For a successful fault diagnosis of analog systems, a fault dictionary needs to be created with the intention to isolate each Behavioral Condition and thus, locate the fault. This can be done by generating a family of signatures from the power supply currents, each corresponding to one fault case.

We refer to the faulty, as well as the fault free, cases as behavioral conditions (BC). If the signatures are generated with a greater possibility of their being different from each other, then the fault diagnosis process becomes easier and more efficient. The analog fault diagnosis technique presented in the following sections accomplishes this by using a ramp signal at the power supply node instead of the conventional constant power supply source. The presence of static bias currents in the power supply bus in analog circuits sets the operating point of the circuit. Any defect in the circuit may increase or decrease this current, hence, recording a significantly different bias current. The various paths, created (or deleted) by the defects in the circuit, can potentially have different resistances associated with them because of the various transistor sizes encountered in analog circuits. Hence, there is a larger probability of recording signatures significantly different from each other, where as in digital circuits, typically, all the PMOS transistors are of the same size, and the NMOS are of the size of PMOS transistors modified by the  $K_n/K_p$  ratio, where  $K_i = \mu_i C_{ox}(W/L)_i$ . As their resistances are inversely proportional to their sizes, their resistances will also be fixed in a similar fashion. Hence, all paths created by defects will have similar resistances. Although abnormal currents are recorded, the signatures will not be different from each other. Hence, the proposed technique takes advantage of the presence of bias currents in analog circuits.

Since the number of all possible fault cases can be enormous for any circuit with reasonable complexity, a limited set of faults which are highly likely to occur can be covered by using physical information such as proximity of nodes (for shorts),

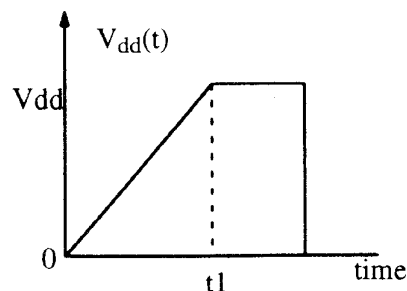


Fig. 1. Ramp signal.

thickness of metal routes (for opens) and the defect statistic specific to the fab.

Naturally, it can be noted that larger and more complex circuitry does not necessarily mean a larger number of fault cases. A larger set of fault cases may, in the worst case, need additional Kohonen networks for isolation. The results show that this technique can detect multiple faults as effectively as single faults.

Another requirement of analog fault diagnosis is the explicit definition of the input signal for signature generation purposes. Unlike digital circuits, no input other than the ones used for setting the operating point is needed for the analog circuits.

## III. POWER SUPPLY RAMPING

As mentioned before, fault diagnosis typically requires a set of signatures, each representing a BC, which are often significantly different from each other. For efficient fault diagnosis purposes, the application of a ramp signal at the power supply is investigated in this section. The bias currents existing in the supply bus are a function of the operating point as well as the topology of the circuit. For a constant supply voltage, this relationship can be represented as shown below:

$$i_{\text{bias}} = f(O, T) \quad (1)$$

where  $O$  is the operating condition of the circuit and  $T$ , the topology. If either  $O$  or  $T$  of (1) is perturbed, the supply current will be changed.

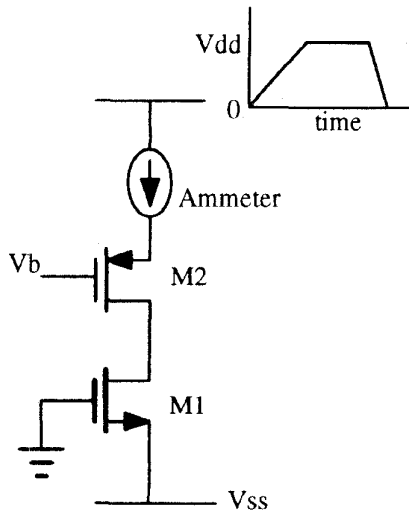
Now, consider the application of a ramp signal at one power supply. The ramp signal is shown in Fig. 1 and can be defined as a function of time as

$$\begin{aligned} V_{dd}(t) &= V^*t \quad \text{for } t < t_1 \\ V_{dd}(t) &= V_{DD} \quad \text{for } t \geq t_1 \end{aligned}$$

where  $V_{DD}$  is the desired positive supply voltage and  $V$  varies from 0 to  $V_{DD}$ . From basic CMOS transistor theory, the operating condition of a circuit can be seen as a function of gate-source ( $V_{gs}$ ), drain-source ( $V_{ds}$ ) and threshold ( $V_t$ ) voltages of each transistor. This can be represented as

$$O = f(V_{gs}, V_{ds}, V_t). \quad (2)$$

To illustrate the basic principles of using a ramp voltage supply, a simple circuit is shown. Fig. 2 shows a CMOS inverter circuit with a current source load implemented by M2P. If a ramp signal is applied at the positive supply voltage of the inverter, then the  $V_{gs}$  and  $V_{ds}$  of both of the transistors

Fig. 2.  $V_{dd}$  ramping on a CMOS inverter.

will also vary with time. Under nominal, fault free conditions, the region of operation of the transistors can be defined to be a function of time as shown below.

#### Transistor M2P:

$$\begin{aligned} O > V_b - v_{dd}(t) &\geq V_{tp} && \text{Subthreshold} \\ O > V_b - v_{dd}(t) - V_{tp} &> v_o(t) - v_{dd}(t), && \text{Saturation} \\ O > V_b - v_{dd}(t) - V_{tp} &< v_o(t) - v_{dd}(t), \\ V_b - v_{dd}(t) &< V_{tp} && \text{Linear} \end{aligned}$$

#### Transistor M1N:

$$\begin{aligned} O < V_{g1} - V_{ss} &\leq V_{tn} && \text{Subthreshold} \\ v_o(t) - V_{ss} &> V_{g1} - V_{ss} - V_{tn} &> O, && \text{Saturation} \\ O < v_o(t) - V_{ss} &< V_{g1} - V_{ss} - V_{tn} && \text{Linear.} \end{aligned}$$

These basic expressions can be used to obtain the different ranges of  $V_{dd}$  and the corresponding regions of operation of both transistors M1N and M2P of the inverter when  $V_{g1}$  has been set to 0. The expressions for the supply current  $I_{dd}$  can be easily obtained once the regions of operation of both the transistors are known. For  $V_{dd} > (V_b + |V_{tp}|) > V_o$  M2P will be in saturation, and M2P will be in the linear region if  $V_{dd} > (V_b + |V_{tp}|) < V_o$ .

Fig. 3 shows the output voltage response for a  $V_{dd}$  sweep of the inverter. The different ranges of  $V_{dd}$  can be identified in Fig. 3, where  $V_{SS} = -2.5V$ . At point A  $V_{dd} = V_b - V_{tp}$ . At point C  $V_{DD}$  is evaluated considering point B which corresponds to  $V_o = V_{tn}$ . For the inverter example, the different regions of operation of the transistors for different values of  $V_{dd}$  are shown in Table I.

In region ②, M2P is in the linear region and M1N is in the saturation region. In this experiment under normal conditions,  $V_{dd} = 2.5V$ ,  $V_{ss} = 2.5V$   $V_b$  was chosen to give  $V_{out} = 0V$ . So region ② is not possible for  $V_{dd} < 2.5V$ . The high gain of the inverter and also a three decimal point precision of the  $V_t$  used in this simulation resulted in seemingly impractical numbers for  $V_{dd}$ . It should be noted that this example is only

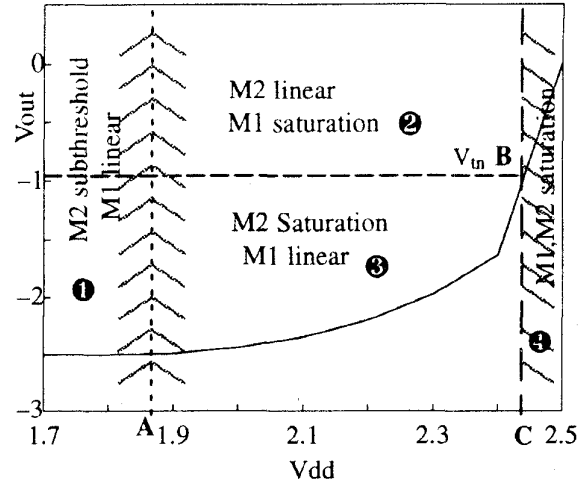
Fig. 3.  $V_{dd}$  versus  $V_{out}$ ; regions of Operation of M1 and M2.

TABLE I  
BOUNDARIES OF  $V_{dd}$  FOR THE INVERTER OF FIG. 3

REGION	$V_{dd}$ RANGE
1	0 to 1.867 V
2	Not Possible
3	1.868 to 2.435 V
4	2.456 to 2.5 V

to illustrate that ramping  $V_{dd}$  makes all the devices operate in *most* of the regions.

From the above discussion, it can be seen that at different points of time, the transistors will be working in different regions of operation depending on the value of the supply voltage at that time. Hence, the supply current flowing through an ammeter will differ from one time point to the other. Equations for the bias current,  $I_{dd}$ , for different regions of operations are well documented in the literature [22], [23]. The time dependency of the supply current can be defined as

$$I_{dd}(t) = f(O(t), T) \quad (3)$$

where

$$O(t) = f(v_{gs}(t), v_{ds}(t), V_t). \quad (4)$$

For the different regions of Table I, the supply current  $I_{dd}$  can be easily obtained from literature [24,25]. Most common defects such as bridging faults and open circuits change the topology of the circuit. For instance, consider a bridging fault between the drain and source of M2P. This fault can be modeled as a short circuit with a small resistor (typically of  $5\Omega$ ) between  $v_{dd}(t)$  and  $v_o(t)$ . Neglecting the small voltage drop across this resistor, we can obtain  $v_o(t) = v_{dd}(t)$ . As M2P is functionally eliminated in this topology, the region of operation of the remaining transistors (M1N in this case) will be different from the other topologies (caused by other BC's).

For the sake of illustration, the inverter circuit is simulated under nominal and faulty conditions and the corresponding plots are shown in Fig. 4. The top most plot in Fig. 4 shows the ramp signal applied at the power supply. The plot in the middle

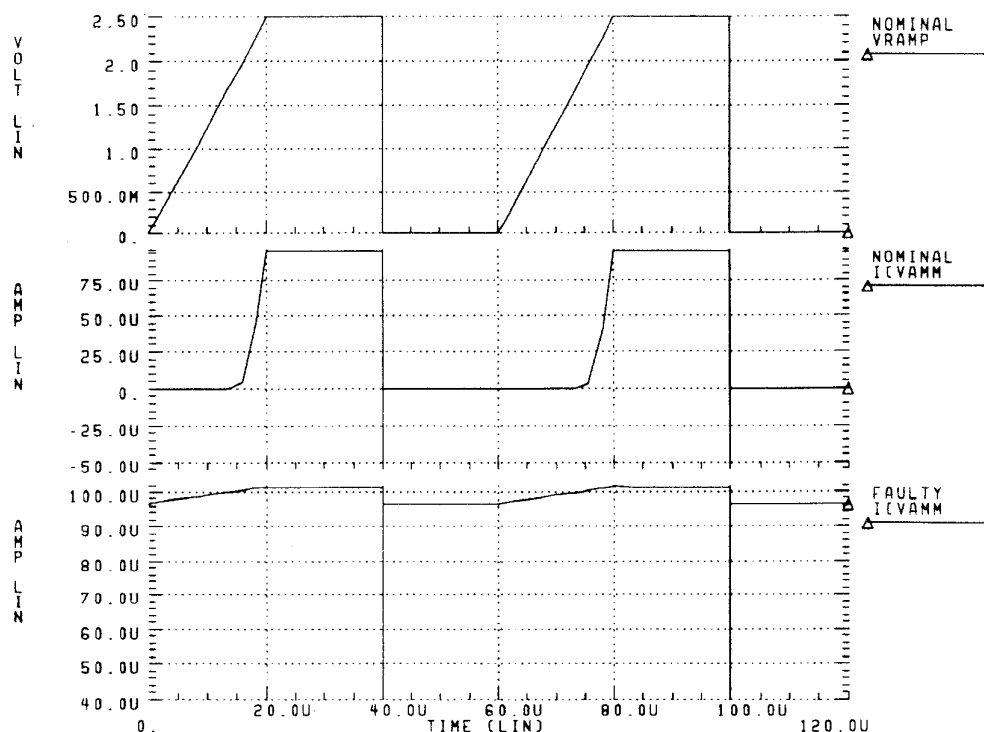


Fig. 4. Ramp signal at  $V_{dd}$ , nominal and faulty current responses through the ammeter.

shows the current flow through the ammeter under nominal conditions. The bottom most plot shows the flow of current for a defect resulting in the drain source short of transistor M2P. However, under the faulty condition, the topology of the circuit is altered and transistor M2P is effectively replaced by the bridging fault model. Hence, transistor MIN is always in saturation, and thus, sinks maximum current at all times as seen in Fig. 4. The results show that the circuit can be diagnosed correctly if the responses of the currents through the ammeter are used to obtain the signatures. Hence, from this example and a number of these cases [32], it can be concluded that the application of a ramp signal at the power supply node is an effective method of generating signatures rich in information, which has the potential to provide signatures of various BC's that can be significantly different from each other.

The slope of the ramp signal is also of significant importance. For reasonably large circuits, the number of BC's to be considered will be large. In order to have a better chance of separating the signatures, it is important to make the circuit operate in the transition regions of operation for a larger period of time. For example, if the slope of the ramp signal is very large, the transistors can skip some regions of operation, and the purpose of application of ramp signal will be defeated. On the other hand, if the slope is too small, the computation time becomes expensive. A tradeoff between these two extreme cases based on the application of a signal with a rise time equal to four times the width of the pulse is found to be reasonable. The width of the pulse is kept small to decrease redundant information as the currents remain constant during that period (as  $V_{dd}$  is constant).

It can be seen that the application of a ramp signal at the input of the circuit does not necessarily make all the transistors in the circuit operate in all regions. For example, it need not necessarily affect the region of operation of any transistor other than the input transistors, whereas the power supplies are the universal nodes in the sense that they are connected to all the stages, and define the currents through all the different stages in the circuit. Hence, the application of the ramp signal at the power supply node only is justifiable. The extension of the discussion presented in this section to the ramping of negative supply voltage or to both the supply voltages is direct, and hence, not shown in this paper.

#### IV. PROCEDURE

Having explained the philosophy behind the application of a ramp signal at the power supply node(s), the procedure of the proposed fault diagnosis methodology will now be presented. The proposed  $I_{dd}(t)$  current measurement technique consists of three stages.

- 1) Signature Generation;
- 2) Signature Classification;
- 3) Fault Diagnosis.

The first stage involves the definition of BC's to be considered, the generation of the responses for each BC, and the recollection of signatures from the responses. The BC definitions can be obtained from any approach that models the physical process defects, such as inductive fault analysis [26]. The circuit under test is simulated with each BC induced, and the current response in the power supply bus is noted at  $m$  different points of time with the ramp signal applied to the

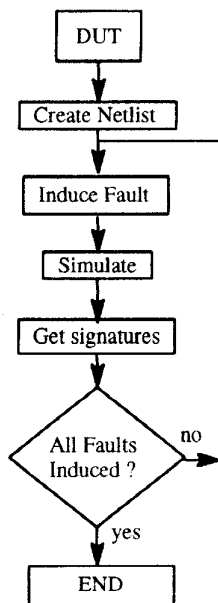


Fig. 5. Signature generation.

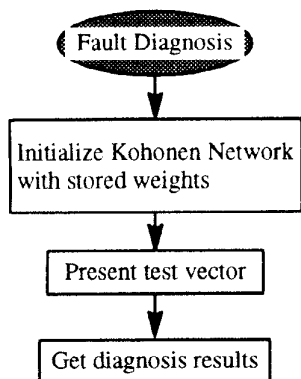
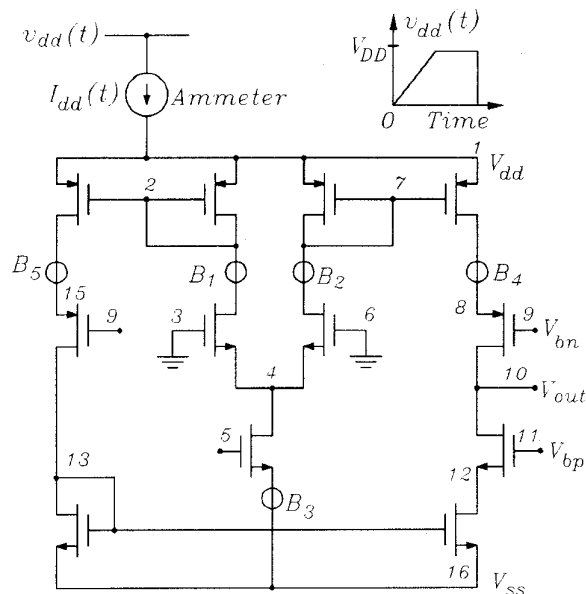


Fig. 6. Fault diagnosis procedure.

supply node. A set of  $n$  optimal sampling points can be chosen from these  $m$  points to form a signature of the response. A technique that performs the derivative of each response and forms a set of optimal test points at which there is a significant change in the response value with respect to its previous values is presented in [12].

Next, a Kohonen network with  $n$  inputs and  $N$  processing elements, where  $N$  is the number of BC's and  $n$  is the dimensionality of the signature, is trained. The Kohonen paradigm [14], [15] maps the signatures from the initial random vector space onto the processing elements. This vector mapping property of the Kohonen paradigm is used to classify the signatures, and thus, to identify the faults. Fig. 5 shows the flow diagram to generate the signatures. These signatures are then used to train a Kohonen network. A cluster table is generated by recording the winner processing unit for each input signature. If a unit wins for more than one signature, then the fault cases associated with those signatures are said to be *collapsing faults*. These faults cannot be isolated from

Fig. 7.  $V_{dd}$  ramping of the OTA circuit.

each other using only these signatures. This phenomenon of reducing the initial vector space, that includes all the signatures, to a vector space consisting of fewer signatures is denoted as *fault clustering*. If this new vector space represented by a unit consists of only a single signature, then the fault case associated with that signature can be isolated. Such a cluster is called an *isolated cluster*.

In practice, the fault diagnosis procedure involves measurement of the power supply current and generation of the test signature. This signature is then used as the input to the trained Kohonen network to obtain the cluster of BC's that best matches the test signature. Thus, the BC existing in the circuit can be successfully diagnosed. This procedure is shown in Fig. 6.

## V. SIMULATED AND EXPERIMENTAL RESULTS

One of the most popular building blocks in analog microelectronics is the operational transconductance amplifier (OTA), also known as unbuffered two-state Op Amp. The proposed fault diagnosis approach is verified on an OTA circuit shown in Fig. 7 with its BC definitions as given in Table III. This circuit is simulated using HSPICE with each BC induced one at a time. Data is obtained by measuring the current,  $I_{dd}(t)$ , through the ammeter. The ramp signal with a pulsewidth of  $6 \mu\text{s}$  and a rise time of  $24 \mu\text{s}$  is applied at the positive power supply of the circuit. The data is obtained by performing a transient analysis on the circuit swept from 1 to  $29 \mu\text{s}$  with increments of  $0.5 \mu\text{s}$ . These responses are obtained initially with 59 data points. The optimal sampling point analysis [12] on these responses yielded 52-dimensional signatures.

The signatures generated for these BC's are then used to train several Kohonen networks according to the Multiple Kohonen Single Analysis (MKSA) approach presented in [12].

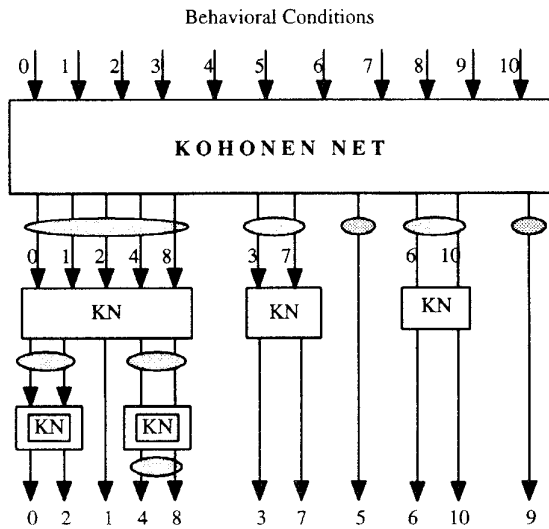


Fig. 8. Clustering of  $V_{DD}$  ramp signatures.

The clustering obtained is shown in Fig. 8. The figure shows that a Kohonen network was trained on the signatures of the 11 BC's considered and it clustered these BC's into 5 different groups (clusters). The first cluster consists of BC's 0, 1, 2, 4, and 8. The second cluster consists of BC's 3 and 7. The third cluster consists of BC 5, the fourth consists of BC's 6 and 10 and the last cluster is isolated and represents BC 9. The three non isolated clusters are used to train three different Kohonen networks to separate the BC's in each cluster. The final clustering consists of one nonisolated cluster representing BC's 4 and 8 and all the other clusters isolated. Hence, out of the 11 BC's considered, only two BC's (BC's 4 and 8) are collapsing and are clustered together, whereas all the other faults can be uniquely identified. This form of representation of the clustering results are denoted as KC-Base (Kohonen Cluster data base) diagrams.

To illustrate the multiple bridging fault and open circuit fault diagnosis capability of the proposed technique, the BC's considered in Table II are extended to include 4 types of open circuit faults and a few multiple faults. Table III gives the definition of the additional BC's considered. It should be observed that the term *branch open* is used instead of open drain or open source in Table III. A "branch" can be defined as a current path between supplies. In Fig. 7, four current paths can be identified. Consider the effect of an open circuit at node 10, or at node 12 or at node 8 in the OTA circuit. All these faults cause no current to flow through that branch (branch 5) and they all have the same effect on the current through the power supply bus. Similarly, open circuits at any node in branches 1 through 5 cause no current to flow through that path and through the branches they control. For instance, the bias current through branch 1 will provide the bias current through branch 5. Hence, if branch 1 is opened, then there will be no currents, through branch 5 as well. Note that the reverse is not true.

For the sake of fault injection, open circuits are typically modeled by a large resistor in parallel with a small capacitor. However, depending on the type of simulator used, one can

TABLE II  
BC DEFINITION FOR THE OTA CIRCUIT

BC	SHORT BETWEEN NODES
0	Fault Free
1	1 & 2
2	1 & 7
3	2 & 4
4	2 & 15
5	4 & 7
6	4 & 12
7	4 & 13
8	4 & 16
9	7 & 8
10	13 & 15

TABLE III  
EXTENDED BC DEFINITIONS FOR THE OTA CIRCUIT

BC	FAULT CASE
11	Branch 1 Open
12	Branch 2 Open
13	Branch 4 Open
14	Branch 5 Open
15	Short Between 4 & 13
	Short Between 2 & 15
16	Short Between 4 & 5
	Short Between 1 & 15
17	Short Between 1 & 4
	Short Between 1 & 7

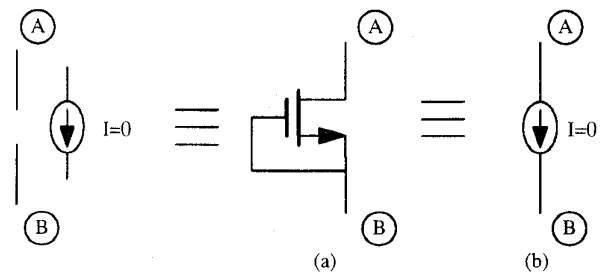


Fig. 9. Open Circuit. (a) Gate source short model 1. (b) Zero current source model.

also model the lack of current through a branch by the following methods: i) connecting a MOS transistor with its gate source tied together, such that the transistor is in cutoff, as shown in Fig. 9(a). ii) by placing a current source, with zero current through it, as shown in Fig. 9(b) [27]. The first method is more convenient to inject an open circuit experimentally as each branch has at least one transistor whose gate and source can be shorted. However, not all circuit topologies are so convenient, and hence, the second option might be used. In this work, the first option is used to simulate an open circuit. The KC-Base generated for all the 19 BC's, including the extended BC's presented in the Table III is shown in Fig. 10. It can be seen that there are only two non isolated clusters containing only 2 BC's each, (BC's 4, 8 and 11, 12).

The diagnosis procedure involves the measurement of test signatures from the circuit under test. The diagnosis capability will be as expected and shown in the KC-Base diagrams if

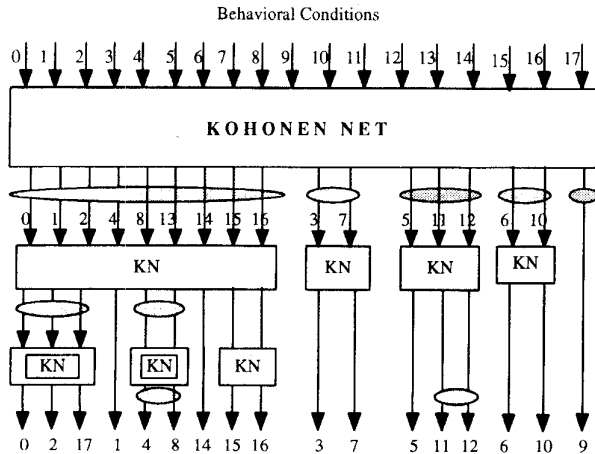


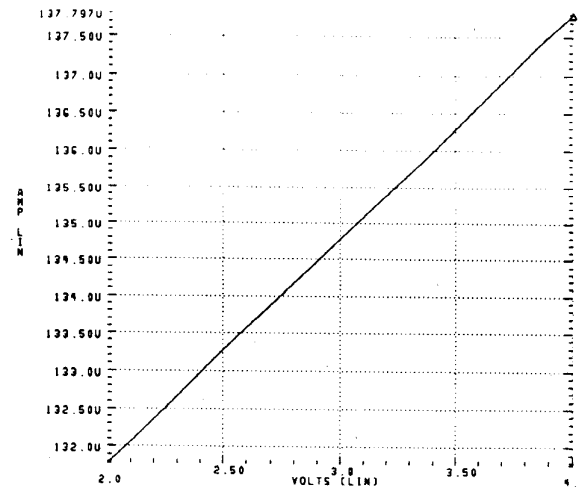
Fig. 10. Clustering of  $V_{DD}$  ramp signatures with multiple shorts and open circuit faults.

there is a good matching between the simulated and measured responses. The measured responses can be given as the input to the Kohonen networks in the KC-Base and the fault cases existing in the circuit can be identified. The OTA circuit was fabricated through the Mosis 2  $\mu\text{m}$  CMOS tiny chip. For the ease of fault injection, each node of the circuit was made accessible externally. The diagnosis results can be easily verified as the existing faults are known beforehand and can be compared with the diagnosis from the KC-Base. Test signatures were generated for each of the BC's listed in Table III. A comparison between the simulated responses and the measured responses of the supply currents for some BC's is shown in Figs. 11, 12, and 13. The test signatures obtained were given as input of the Kohonen network trained on the signatures from the simulations. For all the BC's considered, the diagnosis was precise and the induced fault was identified. All the 18 signatures generated from simulation of the circuit were given as inputs, one at a time, to the Kohonen networks in the KC-Base. Out of the 18 BC's, 14 were identified exactly. BC's 4 and 8, as well as 11 and 12, were clustered together and the diagnosis procedure did not distinguish between them.

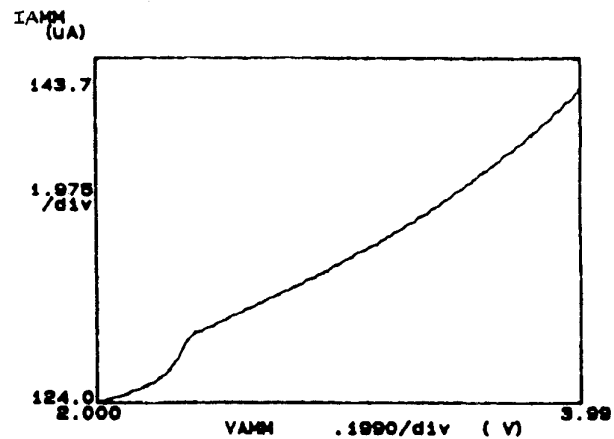
## VI. FEATURES OF THE PROPOSED METHODOLOGY

### A. Open Circuit Diagnosis Capability

The existing techniques for fault diagnosis of analog circuits do not have the potential to diagnose both shorts and open circuits at the same time. Any open branch in the circuit will result in zero current flowing in the output branch of the circuit. Hence, the stimuli-response based techniques will not be able to differentiate between the different open branches that can possibly occur in the circuit. As the proposed technique measures the total current in all branches, the occurrence of opens in various branches will result in different currents through the ammeter. Hence, efficient diagnosis of open circuits is possible with the proposed technique.



(a)



(b)

Fig. 11.  $I_{add}$  current  $V_s$ .  $V_{dd}$  for BC 5. (a) Simulation. (b) Experimental.

### B. No Additional Access Points are Necessary

In this technique, only the power supply node is needed externally for signature generation and measurement purposes. Hence, the additional cost of increased silicon area needed for more access points is avoided.

### C. Ease of Simulation

It is a well-known fact that the simulation of an analog circuit can be made much easier by increasing the dc voltage generators slowly from 0 to the dc values via a transient analysis. In this way, the sources are increased slowly and the capacitors are included in the solution. This is actually more similar to the real world and can be very appropriate for those circuits that need a finite setup time [28]. The dc convergence problems are avoided using this method, and hence, the simulation procedure becomes much easier. As the proposed technique involves the use of a ramp signal at the power supply node, all the properties mentioned here will apply to this technique.



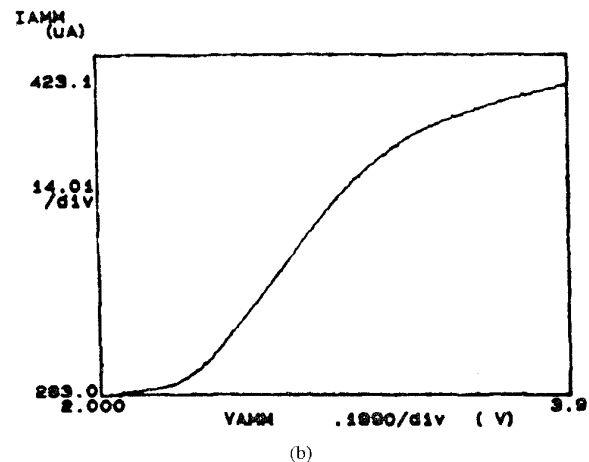
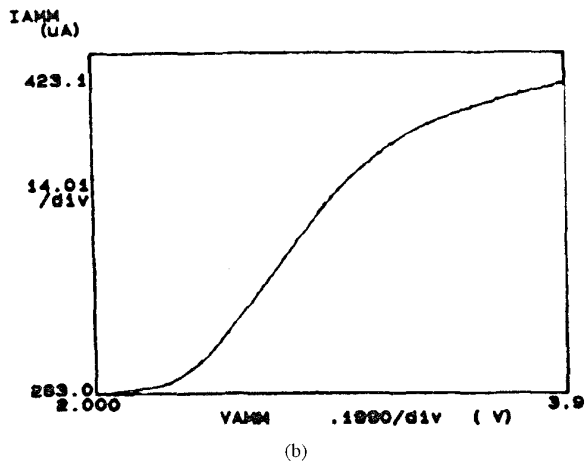
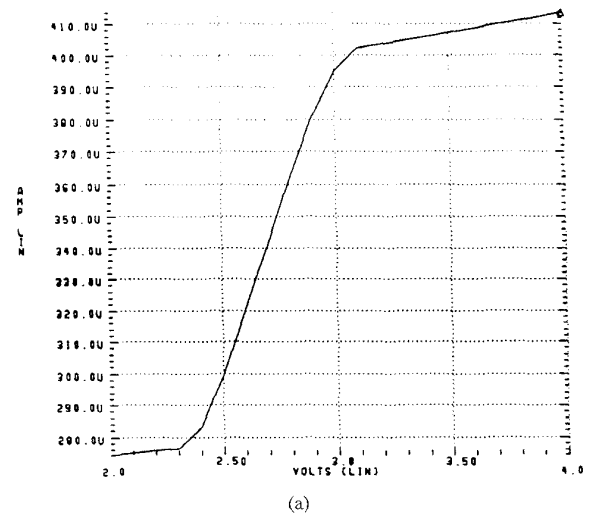
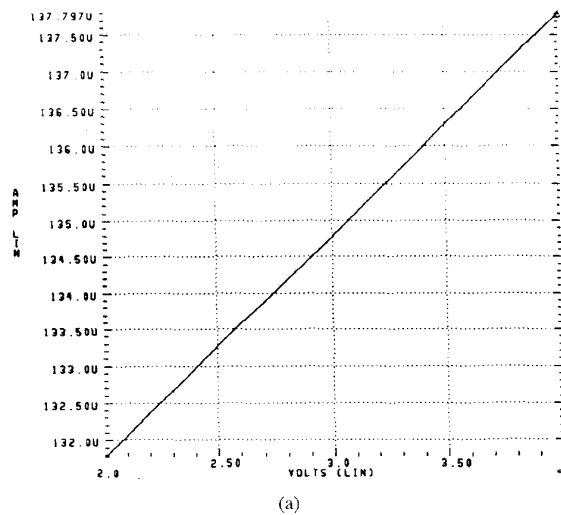


Fig. 12.  $I_{dd}$  current  $V_s$ ,  $V_{dd}$  for BC 14. (a) Simulation. (b) Experimental.

Fig. 13.  $I_{dd}$  current  $V_s$ ,  $V_{dd}$  for BC 10. (a) Simulation. (b) Experimental.

#### D. Process Variation Independence

Current Simulation Before Test (SBT) techniques are limited due to parameter drift and noise. Using these techniques, there is a chance that a given signature is not among the stored faults in the dictionary, in which case, fault diagnosis is not possible. In the proposed approach, as the mapping is from the whole signature vector space, and not from the signature itself, effective diagnostic results are easily obtained if the parameter drift due to process variation and noise are approximately<sup>1</sup> 20–30% of their nominal values. This can be seen in Fig. 14. The figure shows the initial random vector space consisting of individual vector spaces of the BC's. It can be seen that some of the BC's have overlapping vector spaces, and hence, cannot be separated. If the signature of a BC, when a component in the circuit is in tolerance, lies anywhere in the BC's marked space, it will be classified in the same cluster. For example, the signature of BC9, with a tolerant circuit component labeled as  $9^T$ , tolerance will still be classified in the same cluster as long as the tolerance is not large enough to make  $9^T$  lie outside the

<sup>1</sup>In practice, Kohonen Paradigm is trained over all the process corners, so these numbers will be smaller.

vector space of BC 9. Further splitting of BC's in a cluster could be obtained by using Multiple Kohonen Paradigms. How easy, or difficult, it is to split the signatures depends on each particular case.

#### E. Built-In Current Monitoring

The currents in the power supply bus can be monitored with additional circuitry. Several techniques have been proposed to measure the supply currents [21], [23], [25]–[27], [29]. Implementation of these current sensors permits automatic diagnosis capability and can be incorporated in automatic test equipment. Electron-beam probing can also be used to measure the power supply currents.

#### F. Limitations

The current observed through the power supply bus is the summation of the currents in all branches of the circuits. Hence, there is a possibility of more than one fault producing the same summation of currents (though the actual currents through different branches may be different for each fault). Such faults produce similar responses and cannot be isolated

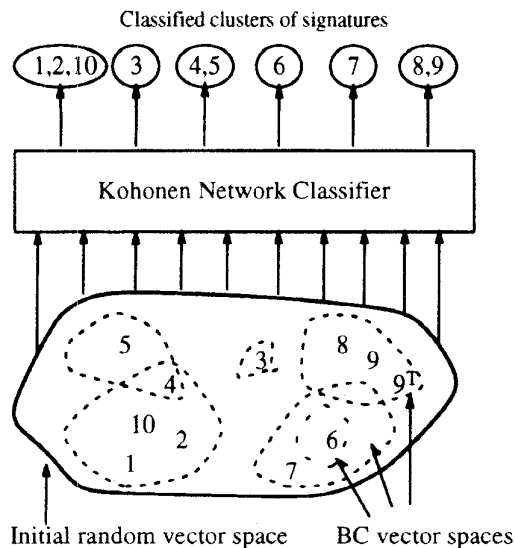


Fig. 14. Typical signature classification by the Kohonen network.

from each other. However, as the most commonly encountered circuits are not exactly symmetrical, this limitation does not prove to be a major disadvantage as can be seen in the theoretical and experimental results provided in the previous section.

## VII. CONCLUSION

A nonconventional analog fault diagnosis technique based on the application of a ramp signal at the power supply node, and the measurement of the supply current, is presented. The proposed methodology is verified with experiments involving a practical CMOS integrated OTA circuit. The features of this technique prove that it overcomes most of the limitations of the present diagnosis methods and that it can also diagnose open circuits. Additional tradeoffs to improve the splitting of a signature is possible by adding observable nodes.

## APPENDIX

A Kohonen network is a feature mapping self-organizing neural network [14], [15] with unsupervised competitive learning. The characteristic of this network is that it maps a given random input stimuli space to a *cluster* space composed of distinct cluster elements. For example, a Kohonen network can be used to highlight a letter, say "A," from a given set of characters consisting of letters and number and written in any calligraphic style. After training, the network should be able to group all "A's" of various calligraphic styles in one single cluster. Let us briefly describe the behavior of a Kohonen network. Fig. 15 shows its basic structure. The layer consists of  $N$  ordered processing elements; each receiving  $n$  inputs signals  $x_1, x_2, x_3, \dots, x_n$  coming from an  $n$ -dimensional Euclidean space. A weight  $w_{ij}$  is associated with the  $j$ th Kohonen processing element and the  $i$ th input signal. Each Kohonen processing element calculates a matching score  $M_i$

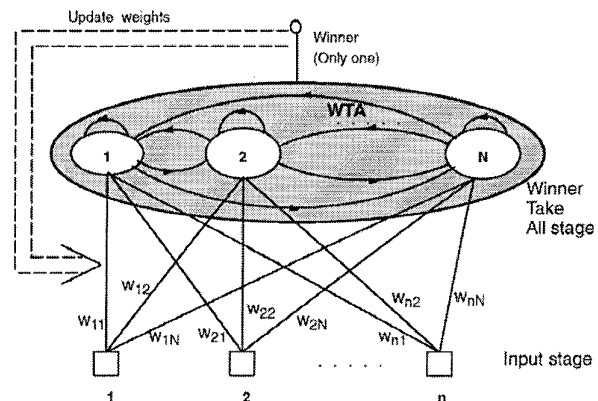


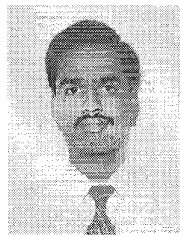
Fig. 15. Kohonen network architecture.

according to the formula:  $M_j = D(W_j, X)$ , where  $w_j = (w_{1j}, w_{2j}, w_{3j}, \dots, w_{nj})^T$ ,  $X = (x_1, x_2, x_3, \dots, x_n)^T$  and the function  $D(a, b)$  is a distance measurement function. The Euclidean distance,  $D(a, b) = |a - b|$ , is a common measure used in many applications. Input signal vectors  $X$ , randomly taken from the input space, are presented to the network one at a time. The number of input vectors can be  $Q$ ,  $Q \leq N$ . Once each Kohonen processing unit has calculated its matching score  $M_j$ , a competition takes place in the Winner-Take-All layer (WTA) to determine which of the units has the smallest matching score, i.e., to find out the weight vector  $W_j$  that most closely resembles the input vector  $X$ . Matching score ( $M_j$ ) ties are broken based on the processing unit index number. The unit with the smallest matching factor is called the *winner*. A unit can win for more than one input vector  $X$  or may not win at all. The winner for a particular vector(s) is said to represent that vector(s). The learning is implemented by updating the weights by a fraction  $\eta$  such that  $M_j$  is minimized.

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