Received 22 May 2019; revised 18 July 2019; accepted 7 August 2019. Date of publication 12 August 2019; date of current version 6 December 2019. The review of this article was arranged by Editor C. S. Tan.

Digital Object Identifier 10.1109/JEDS.2019.2934575

Analog Performance and Its Variability in Sub-10 nm Fin-Width FinFETs: A Detailed Analysis

MANDAR S. BHOIR [1] (Graduate Student Member, IEEE), THOMAS CHIARELLA [2], LARS ÅKE RAGNARSSON [2], JEROME MITARD [2], VALENTINA TERZEIVA [2], NAOTO HORIGUCHI [2], AND NIHAR R. MOHAPATRA [1] (Member, IEEE)

1 Department of Electrical Engineering, Indian Institute of Technology Gandhinagar, Gandhinagar 382355, India
2 Logic Technologies, Interuniversity Microelectronics Center, 3001 Leuven, Belgium

CORRESPONDING AUTHOR: M. S. BHOIR (e-mail: mandar.bhoir@iitgn.ac.in)

This work was supported in part by the Visvesvaraya Ph.D. Scheme, MeitY, Government of India and in part by the Horizon 2020 ASCENT EU Project (Access to European Nanoelectronics Network) under Grant 654384.

ABSTRACT This paper discusses in detail the effects of Sub-10nm fin-width (W_{fin}) on the analog performance and variability of FinFETs. It is observed through detailed measurements that the trans-conductance degrades and output conductance improves with the reduction in fin-width. Through different analog performance metrics, it is shown that analog circuit performance, in Sub-10nm W_{fin} regime, cannot be improved just by W_{fin} scaling but by optimizing source/drain resistance, gate dielectric thickness together with the W_{fin} scaling. We also explored the effect of process induced total and random variability on trans-conductance and output conductance of FinFETs. A systematic strategy to decouple different variability sources has been discussed and it is shown that mobility, source/drain resistance and oxide thickness are the critical parameters to reduce variability.

INDEX TERMS FinFET, sub-10nm fin-width, technology scaling, analog/RF, variability, trans-conductance, output conductance, series resistance, mobility.

I. INTRODUCTION

The FinFETs successfully replaced planar MOS transistors at 22nm CMOS technology node because of their superior short channel control and higher driving capability at a much smaller footprint [1]. Over the years, the fin-width (W_{fin}) has been scaled down to improve the gate-electrostatic control and to continue logic oriented technology scaling [2]. Furthermore, the applications like Long-term evolution (LTE) phones and emerging sub-6GHz 5G bands demand transistors with better analog/Radio-frequency (RF) performance [3]. Therefore, the development of analog/RF capabilities in advanced FinFET technology nodes is essential to reap the System-on-Chip (SoC) benefits like low power and high performance in smaller area [4], [5].

Note that the analog domain mainly benefits from gate-length scaling (improved trans-conductance (g_m)) and W_{fin} scaling (better gate-electrostatic control, lower output conductance (g_{ds})) of FinFETs [6], [7]. Recently, this W_{fin} scaling has entered sub-10nm regime. There are several literature on the impact of sub-10nm W_{fin} on logic performance [8], [9], [10]. However, the effect of sub-10nm W_{fin} on the analog performance of n and pFinFETs has not been discussed in detail. We had earlier reported the effect of W_{fin} scaling on the analog performance of nFinFETs [11] but the detailed analysis was not presented.

In this work, we have investigated in detail the effect of W_{fin} scaling on the analog performance metrics like g_m, g_{ds}, intrinsic gain (g_m/g_{ds}) and trans-conductance generation efficiency (g_m/I_d) for n and p-type FinFETs. It is shown that the W_{fin} scaling, by itself, cannot provide the necessary benefits in sub-10nm W_{fin} regime. We explored few process optimization methods and showed that the analog performance in sub-10nm W_{fin} regime can be improved

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

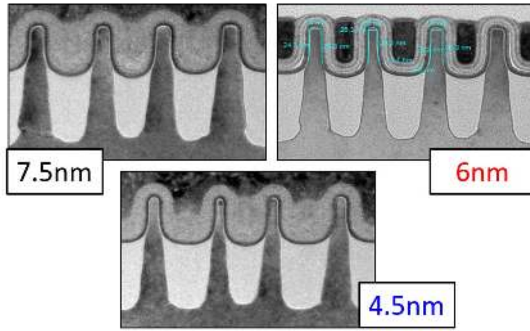

FIGURE 1. TEM image of FinFET devices used in this work. Different fin-widths (W_{fin} = 7.5, 6 and 4.5nm) are patterned using Self-Aligned Double Patterning (SADP) technique.

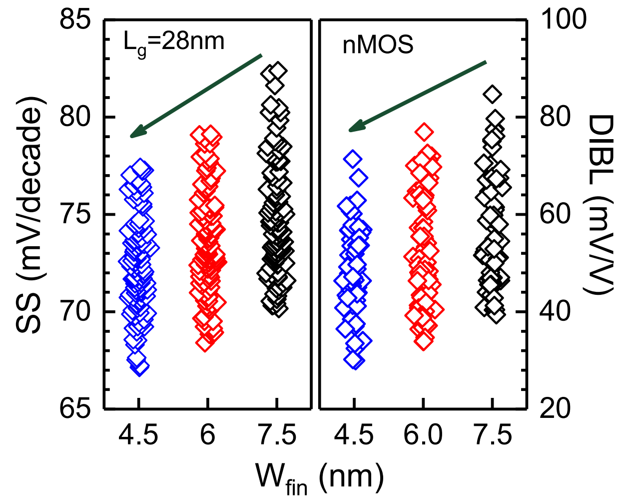

FIGURE 2. SS and DIBL for nFinFETs with different W_{fin}s. The SS and DIBL reduce for narrower FinFETs because of improved gate electrostatic control.

by optimizing the effective dielectric thickness (EOT) and source/drain (S/D) resistance.

Further, for analog circuits like current mirrors and differential amplifiers, transistor-level matching is of utmost importance. However, the process-induced variability cause mismatch between transistors placed on same die (Local/Random) and different dies (Total = Global + Local). This adversely affects the circuit performance and production yield [12], [13]. In this work, we have also investigated the total and random variability in g_m and g_{ds} for sub-10nm W_{fin} FinFETs. We have provided a systematic strategy to separate different sources of g_m variation. Using this strategy, we have shown that mobility (μ), source-drain series resistance (R_{SD}) and oxide-thickness (T_{ox}) are responsible for the variation in this regime. The knowledge about these variability sources is essential for, (a) reducing variability by process-parameter tuning and (b) modeling these variability sources for accurate prediction in circuit simulators.

The paper is organized as follows. Section II describes the device and measurement details. Section III discusses the effect of W_{fin} on different analog performance metrics. Section IV presents some process modifications to improve the analog performance for sub-10nm W_{fin} FinFETs. Section V discusses the device variability and different sources responsible for it followed by conclusion in Section VI.

II. DEVICE AND MEASUREMENT DETAILS

The FinFET devices used in this work are fabricated in a 300mm line at IMEC. The device fins with fin-height (H_{fin}) of ~26nm are patterned using Self Aligned Double Patterning (SADP) method. The FinFETs with 7.5, 6 and 4.5nm W_{fin} are used in this work and their TEM images are shown in Fig. 1. These FinFETs have an EOT of ~0.8nm. The final gate stack is fabricated by Replacement Metal Gate (RMG) technology with effective work-function set by different metal layers. The detailed process information can be found in [10].

The transistors measured in this work have L_g varying from 24 to 250nm. However, we have mainly focused on 28, 34nm for n and pFinFETs respectively. The measured devices have number of fins (N_{fin}) varying from 2 to 22. To investigate the analog performance metrics, the measurements are performed at room temperature on isolated FinFETs with different W_{fin} on 13 dies across the wafer. The g_m and g_{ds} are extracted from the transfer and output characteristics for different gate overdrive voltage (V_{ov}) with transistors biased in saturation regime ($V_{ds} > V_{ov}$).

For variability analysis, the measurements are performed on FinFETs across 145 dies in a single wafer. The identical FinFETs placed on different dies are measured to investigate the total variability. For random variability, the identical MOS transistor pair (MOS1 and MOS2) placed at a minimum possible distance (in identical environment) in the same die but with independent electrical connections are used. After electrical characterization, different device parameters are extracted from the measured transfer and output characteristics.

III. EFFECT OF FIN-WIDTH SCALING

Fig. 2 shows Sub-threshold swing (SS) and Drain-induced barrier lowering (DIBL) for nFinFETs with different W_{fin}. As shown, the SS and DIBL reduces for narrower W_{fin} FinFETs because of improved gate-electrostatic control. This improvement allows further L_g scaling. Although, the SS and DIBL are shown for the nFinFETs, similar behavior is also observed for pFinFETs.

A. G_M AND G_{DS}

Fig. 3 shows g_m as a function of L_g for FinFETs with different W_{fin}. Each point represents median of the measurements carried on 13 dies (across the wafers) at V_{ov}/V_{ds} = 0.2/0.6V. As shown, the g_m increases with reduction in L_g. However, the rate of increase saturates for shorter L_g and is almost zero for W_{fin} of 4.5nm. This saturation behavior is attributed to the increased role of velocity saturation and R_{SD} in shorter L_g FinFETs.

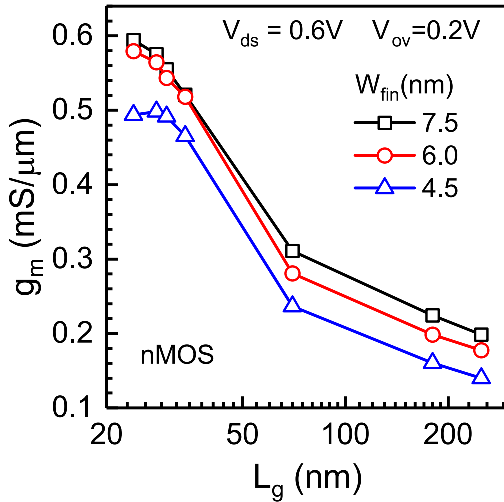

FIGURE 3. Normalized g_m as a function of L_g plotted for FinFETs with different W_{fin}. Note, each point represents the median of the measurement from 13 different dies. The g_m improves with reduction in L_g but the rate of improvement saturates for shorter L_gs.

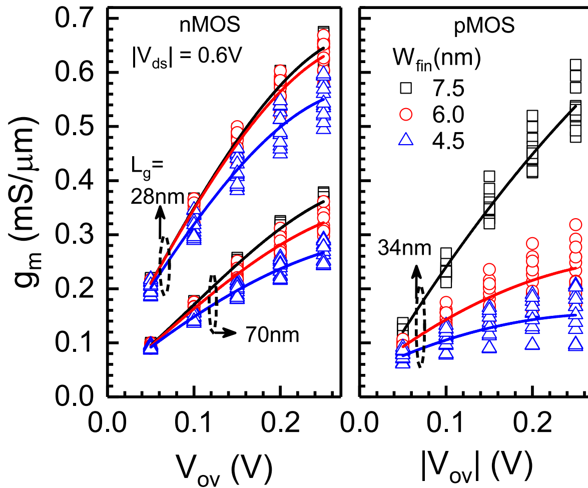

FIGURE 4. Normalized g_m as a function of V_{ov} for n and pFinFETs with different W_{fin}. The g_m reduces for narrower fin because of μ and R_{SD} degradation.

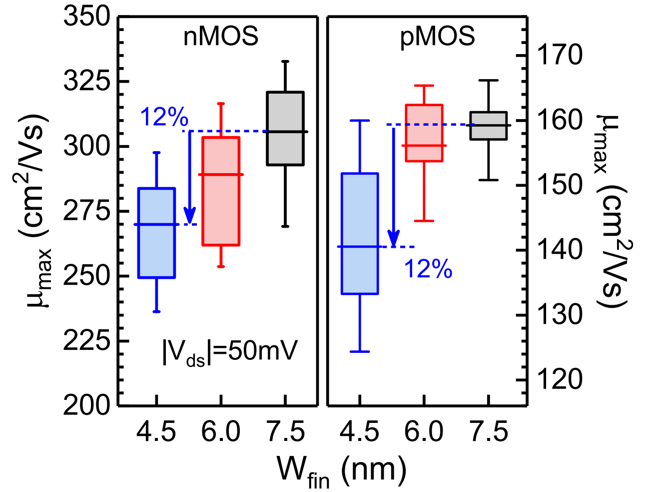

FIGURE 5. The box-plot showing the impact of W_{fin} scaling on maximum electron and hole mobility. The μ_{max} reduces for narrower fins owing to increased phonon and surface-roughness scattering.

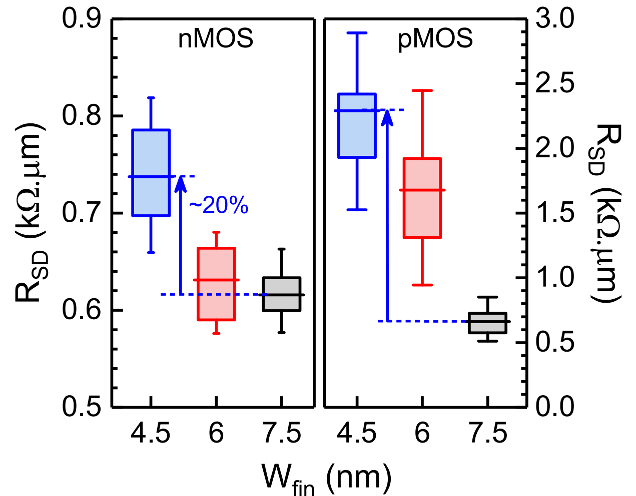

FIGURE 6. The box-plot showing the impact of W_{fin} scaling on S/D series resistance. R_{SD} increases for thinner fins resulting in degradation of FinFET performance.

Fig. 4 shows g_m as a function of V_{ov} for FinFETs (L_g of 28, 34 and 70nm) with different W_{fin}. As shown, the g_m increases non-linearly with V_{ov}. Also, at a particular V_{ov}, the g_m reduces with W_{fin} and this trend is same for both n and pFinFETs of different L_g (Fig. 3). Since the slope of g_m-V_{ov} curve is proportional to μ and R_{SD}, the observed non-linearity and degradation is attributed to these factors. To confirm this, we have extracted μ and R_{SD} for different W_{fin}s. The μ is extracted using the Split-CV measurement technique [14] and the maximum mobility (μ_{max}) for different W_{fin} is shown in Fig. 5. As shown, μ_{max} degrades by ~12% for 4.5nm W_{fin} compared to the 7.5nm W_{fin}. Note that with W_{fin} scaling, the electrons (holes) get confined inside the silicon body resulting in enhanced electron (hole)-phonon interactions. Moreover, the increased proximity of electron/hole to Si-SiO_2 interface enhances surface roughness scattering thereby resulting in mobility degradation [9], [15].

For R_{SD}, we first extracted the on-state resistance, R_{on} (V_{ds}/I_d at V_{ds} = 50mV and V_{ov} = 0.4V) for FinFETs with different L_g on each die. The R_{on} includes resistance contribution from channel (R_{ch}) and source/drain (R_{SD}). By linearly extrapolating the R_{on}-L_g to L_g = 0, the R_{SD} is extracted from the y-intercept [16]. Note that the R_{SD} includes contribution from S/D extension region, S/D epi-layer and contact resistance. Fig. 6 shows the R_{SD} for FinFETs with different W_{fin}. As shown, the R_{SD} increases by ~20% for nFinFET and multiple times for pFinFET when W_{fin} is scaled from 7.5nm to 4.5nm. This R_{SD} degradation for thinner fins is because of higher extension region resistance (thinner W_{fin}) and lower epi-volume (as mentioned in [10]).

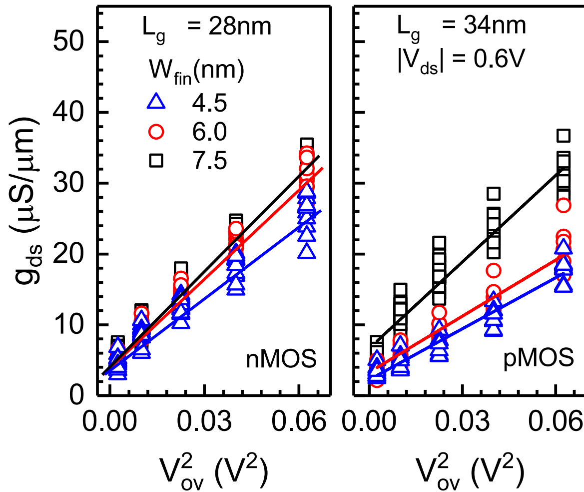

FIGURE 7. Normalized g_{ds} as a function of V_{ov} for n/p type FinFETs with different W_{fin}. The better gate-electrostatic control in narrower fins, reduces the slope of g_{ds}-V_{ov}^2 curves.

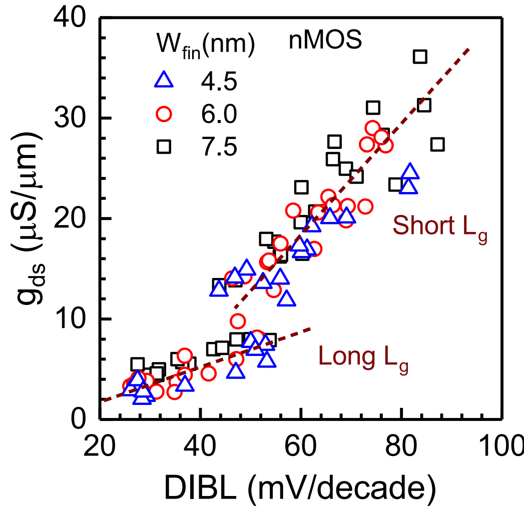

FIGURE 8. The correlation between g_{ds} and DIBL for FinFETs with different W_{fin}s and L_gs. The strong g_{ds}-DIBL correlation for shorter L_g confirms that DIBL is responsible for g_{ds} in this L_g regime.

The different R_{SD}-W_{fin} behavior in n and pFinFETs can be attributed to different S/D extension-implant dose retention, dopant diffusion and an additional component in extension and S/D regions [10]. To summarize, the g_m reduces for narrower W_{fin} FinFETs because of μ and R_{SD} degradation in sub-10nm W_{fin} regime.

Fig. 7 shows g_{ds} as a function of V_{ov}^2 for n/p-FinFETs. As shown, the g_{ds} reduces for narrower W_{fin} for all the V_{ov}s. A strong correlation between g_{ds} and DIBL for shorter L_g FinFETs with 4.5nm, 6nm and 7.5nm W_{fin}s in Fig. 8, confirms the role of DIBL (gate electrostatic control) on g_{ds}. The reduction in DIBL with W_{fin} scaling (Fig. 2) explains the g_{ds} reduction with W_{fin}.

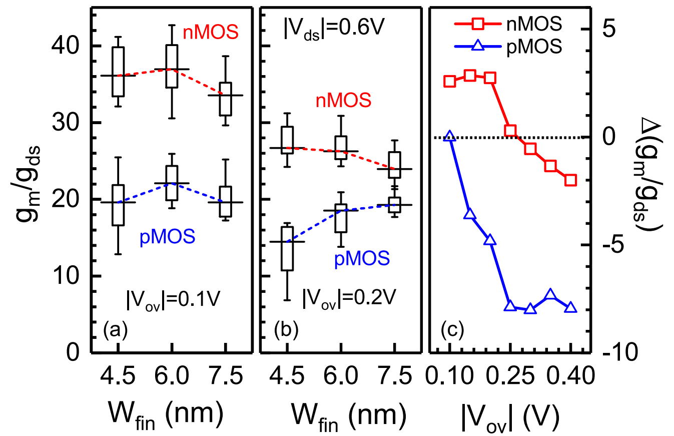

FIGURE 9. (a), (b) The box-plot showing the effect of W_{fin} scaling on FinFETs g_m/g_{ds} extracted for different V_{ov}s and (c) The change in g_m/g_{ds} $[(g_m/g_{ds})_{Wfin=4.5nm} - (g_m/g_{ds})_{Wfin=7.5nm}]$ as function of V_{ov} for n and pFinFETs. With W_{fin} scaling, no significant improvement in g_m/g_{ds} is observed for nFinFETs while it degrades for pFinFETs.

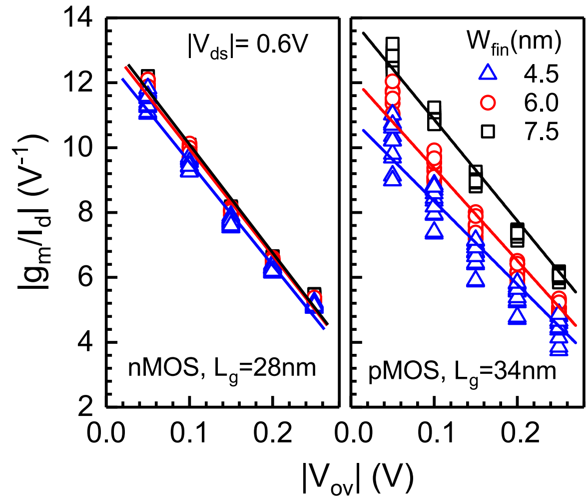

FIGURE 10. The trans-conductance generation efficiency, g_m/I_d as a function of V_{ov} for FinFET with different W_{fin}. No improvement in g_m/I_d is observed with W_{fin} scaling.

B. G_M/G_{DS} AND G_M/I_D

Some analog circuits like amplifiers need higher transistor intrinsic gain (g_m/g_{ds}) while power efficient analog circuits need higher gain at smaller bias current. Therefore, the higher trans-conductance generation efficiency (g_m/I_d) is an important performance metric. We have studied the effect of W_{fin} scaling on both these metrics. Fig. 9 shows g_m/g_{ds} as a function of W_{fin} for different V_{ov}. With W_{fin} scaling, no significant improvement in g_m/g_{ds} is observed for nFinFETs while some degradation is observed for pFinFETs. In-spite of g_{ds} improvement, the g_m degradation is the main reason behind this behavior.

Fig. 10 shows g_m/I_d as a function of V_{ov} for different W_{fin}s. As shown, the g_m/I_d is almost constant with W_{fin} scaling for nFinFETs while it degrades for pFinFETs. The higher g_m reduction for thinner W_{fin} pFinFETs is mainly responsible for this behavior.

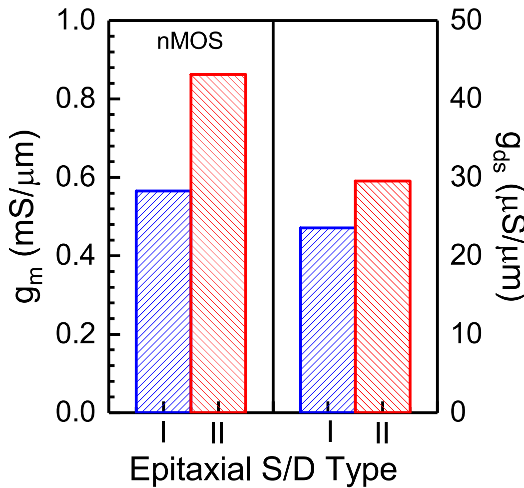

FIGURE 11. The g_m and g_{ds} for 28nm long n-FinFETs with different S/D Epi. stacks. Lower R_{SD} and higher L_{ov} length in Epi-II results in ~53% higher g_m and ~26% higher g_{ds}.

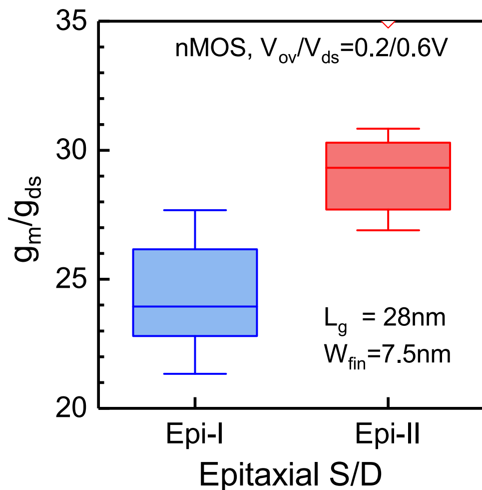

FIGURE 12. The g_m/g_{ds} for 28nm long nFinFET with different S/D Epi. stack. ~21% improvement in g_m/g_{ds} is achieved with R_{SD} optimization for Epi-II.

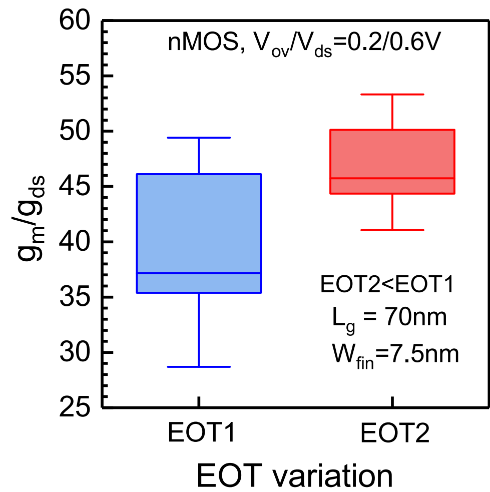

FIGURE 13. Impact of EOT scaling on FinFET intrinsic gain (g_m/g_{ds}). A thinner EOT results in ~23% improvement in g_m/g_{ds} due to improved g_m and g_{ds}.

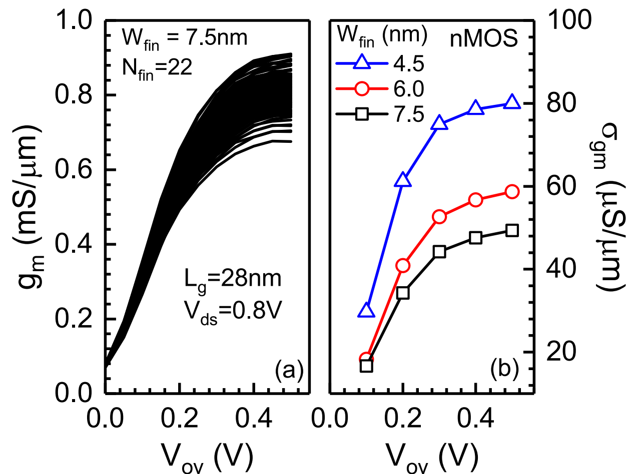

FIGURE 14. (a) Normalized g_m as a function of V_{ov} measured for nFinFETs (W_{fin} = 7.5nm, L_g = 28nm) on 145 different dies across a wafer (b) Standard deviation of g_m, σ_{gm} as a function of V_{ov} for FinFETs with different W_{fin}. The σ_{gm} increases with V_{ov} and thinner W_{fin}.

IV. PROCESS OPTIMIZATION TO IMPROVE THE ANALOG PERFORMANCE

Overall, the considerable improvement in FinFET analog performance achieved by scaling L_g for narrower fin devices, is no longer observed in sub-10nm W_{fin}s. In this section, we explored some process options to improve the analog performance.

For R_{SD} optimization, we investigated two different S/D epitaxial stacks (Epi-I and Epi-II). The Epi-II (~2×10^{21}cm^{-3}) has higher S/D doping compared to Epi-I (~3×10^{20}cm^{-3}). Both these Epis are grown with different process conditions [17] to enable different epi-doping. Fig. 11 shows g_m and g_{ds} for FinFETs having these Epi-stacks. The R_{SD} decreases and gate-S/D overlap length (L_{ov}) increases [10] with higher S/D doping. This improves g_m by ~53% and g_{ds} by ~26% as shown in Fig. 11. Overall, ~21% increase in g_m/g_{ds} is observed for Epi-II, which is shown in Fig. 12. Another technique to improve the analog performance is by EOT scaling. Thinner EOT improves the gate-control but reduces carrier mobility. The effect of thinner EOT (achieved by scaling the HfO_2 thickness from 1.8 to 1.5nm) is shown in Fig. 13. As shown, ~23% improvement is achieved in g_m/g_{ds} due to ~7.5% increase in g_m and ~15% reduction in g_{ds} for thinner EOT.

Further, the process innovations like smoothing of fin-sidewalls can be used to reduce the mobility degradation [18], increase g_m (for constant g_{ds}) and improve g_m/g_{ds}. Higher H_{fin} (taller fins) in tapered fin FinFETs can also improve g_m/foot-print and g_m/g_{ds} [19].

V. TOTAL AND RANDOM VARIABILITY

Fig. 14a shows g_m as a function of V_{ov} for 28nm long n-FinFETs measured across 145 different dies in a wafer.

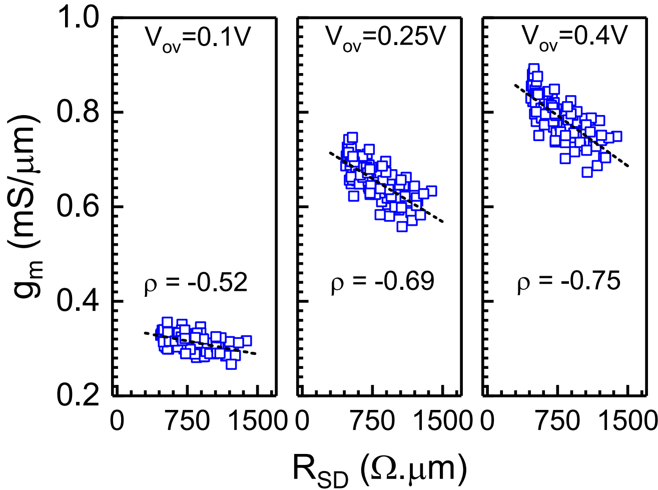

FIGURE 15. The correlation between g_m and R_{SD} plotted for different V_{ov}s. The increased correlation-coefficient (ρ) for higher V_{ov} indicates the increased impact of R_{SD} on g_m.

The spread in the g_m illustrates the total variations. Fig. 14b shows standard deviation of this g_m variation (σ_{gm}) for different V_{ov} and W_{fin}. As shown, σ_{gm} monotonically increases with V_{ov} for all the W_{fin}s. To investigate in detail, we correlated g_m with R_{SD} for each die. Fig. 15 shows the correlation for different V_{ov}s. As observed, the g_m correlates very well with R_{SD} and the correlation is stronger for higher V_{ov}s. This underlines the role of R_{SD} on variability and its V_{ov} dependence in sub-10nm W_{fin} regime.

Further, we provide a systematic strategy to decouple different sources responsible for g_m variations and quantify their impact. We separated g_m variability in terms of three components, SS, R_{SD} and μ variations. Note, since the g_m variations are investigated for constant V_{ov}, the effect of V_t on variation is eliminated. The SS component capture the variations in L_g, W_{fin} and T_{ox} occurred during the fabrication. By simplified error propagation law [20], the σ_{g_m} in terms of the three components can be written as,

$$(\sigma_{g_m})^2 \approx \left(\frac{\partial g_m}{\partial SS}\sigma_{SS}\right)^2 + \left(\frac{\partial g_m}{\partial R_{SD}}\sigma_{R_{SD}}\right)^2 + \left(\frac{\partial g_m}{\partial \mu}\sigma_{\mu}\right)^2 \quad (1)$$

The above equation assumes that SS, R_{SD} and μ variations are independent of each other and it has been verified. For each component (x), the first factor ($\frac{\partial g_m}{\partial x}$) is the regression-line slope obtained from g_m-x correlation. The standard deviation of component x represents the second factor (σ_x). The measured σ_{g_m} and the respective contribution from SS, R_{SD} and μ to σ_{g_m} for the 28nm long nFinFET at V_{ov}/V_{ds} = 0.2/0.8V is shown Fig. 16. Note, the contribution from μ is calculated by subtracting the SS and R_{SD} contribution from the measured σ_{g_m} using (1). As shown, the total variability in g_m is ∼12% and the variations in μ and R_{SD} are mainly responsible for it.

We have also looked at the effect of random variability on g_m ($\sigma_{\Delta g_m}$). For this, we used the same methodology as discussed in the previous paragraph. The components in (1) are calculated using measurement from matched transistor pairs, i.e., ΔSS, ΔR_{SD} and $\Delta\mu$ where $\Delta SS = SS_{MOS1}$-SS_{MOS2}, etc. as discussed in Section II. The measured $\sigma_{\Delta g_m}$ and the respective contribution from ΔSS, ΔR_{SD} and $\Delta\mu$ for nFinFET at V_{ov}/V_{ds} = 0.2/0.8V is shown in Fig. 17. As shown, the process induced random variability in g_m is ∼12%. The mobility variations are mainly responsible for the random variability followed by R_{SD} and SS variations.

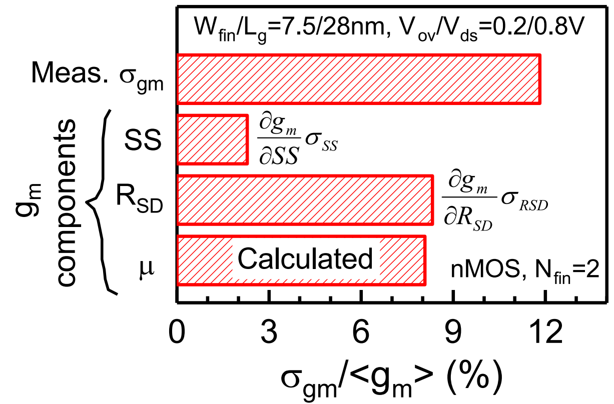

FIGURE 16. Measured total variability in g_m and its decomposition into SS, R_{SD} and μ components. The data has been normalized with mean of g_m (<g_m>). R_{SD} and μ plays a major role in total variability of g_m.

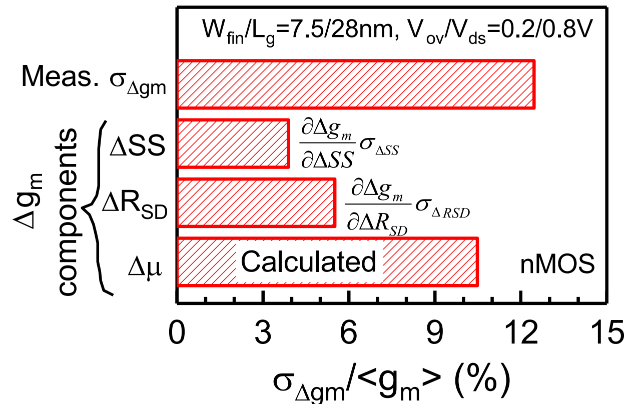

FIGURE 17. Measured random variability in g_m and its decomposition into ΔSS, ΔR_{SD} and $\Delta\mu$ components. The data has been normalized with mean of g_m (<g_m>). The μ followed by R_{SD} and SS plays a major role in random variability of g_m.

TABLE 1. Impact of L_g, W_{fin} and T_{ox} variation on g_m, SS and g_m-SS correlation.

Parameter	variation	SS	g_m	g_m-SS correlation
L_g	↑	↓	↓	Positive
	↓	↑	↑	
W_{fin}	↑	↑	↑	Positive
	↓	↓	↓	
T_{ox}	↑	↑	↓	Negative
	↓	↓	↑	

*Symbols ↑/↓ indicate increase/decrease in the parameter value.

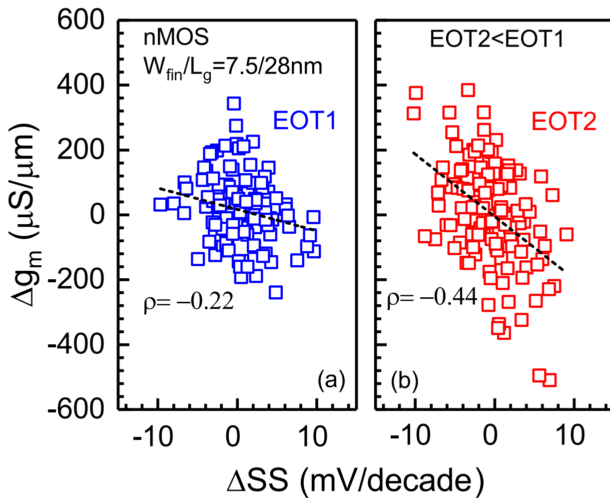

FIGURE 18. The correlation between Δg_m and ΔSS plotted for FinFETs with different EOT. The negative nature of Δg_m-ΔSS correlation and its strengthening for thinner EOT confirms the role of T_{ox} variations.

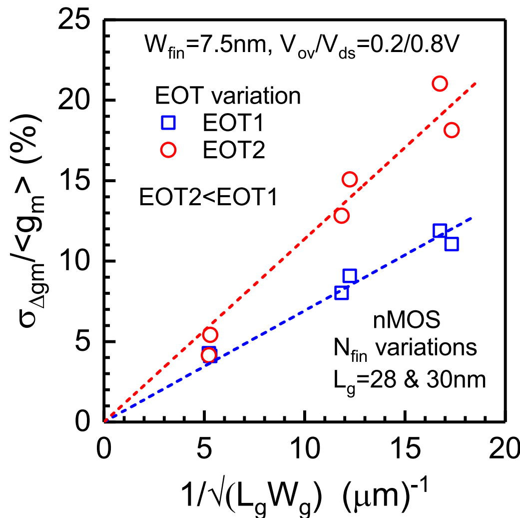

FIGURE 19. The g_m Pelgrom plot for FinFETs with different EOT. The Δg_m variability increases for FinFETs with thinner EOT.

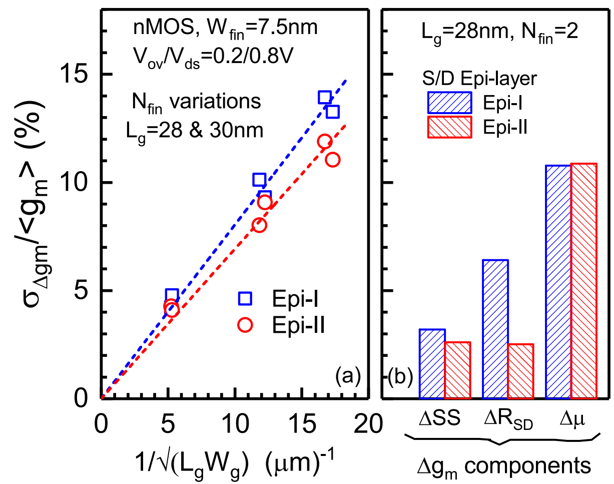

FIGURE 20. (a) The g_m Pelgrom plot and (b) Contribution of different components in Δg_m variability plotted for FinFETs with different S/D Epi. stack. The Δg_m variability is lower for FinFETs with Epi-II stack because of reduced ΔR_{SD} contribution.

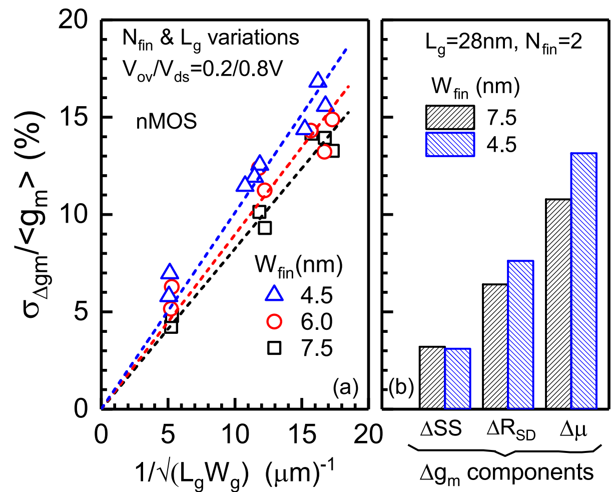

FIGURE 21. (a) The g_m Pelgrom plot and (b) Contribution of different components in Δg_m variability, plotted for FinFETs with different W_{fin}. The Δg_m variability is higher for narrower fins because of increased contribution from ΔR_{SD} and $\Delta\mu$.

We investigated further to find out the exact factor responsible for SS variation. Table 1 summarizes the effect of L_g, W_{fin} and T_{ox} variation on g_m-SS correlations while Fig. 18a shows the correlation between g_m and SS for a 28nm long nFinFET. The negative correlation observed for Δg_m- ΔSS ($\rho = -0.22$) can only be explained by T_{ox} variations (from Table I). To augment our understanding further, we have plotted Δg_m- ΔSS correlation for FinFETs with two different EOTs. This is shown in Fig. 18. The increased strength of Δg_m- ΔSS correlation ($\rho = -0.44$) for thinner EOT (where T_{ox} variations should be dominant) confirms the role of T_{ox} in SS and hence in g_m variations. Although, the correlation is shown for Δg_m and ΔSS, similar behavior is also observed for g_m and SS correlation. Fig. 19 shows the normalized g_m variation as a function of (Gate-Area)$^{-0.5}$ (similar to Pelgrom plot [21]). The zero intercept indicates that the variation have random nature while the slope of this plot ($A_{\Delta gm}$) indicates the magnitude of g_m variability. The increase in $A_{\Delta gm}$ for thinner EOT underlines the importance of T_{ox} variation in advanced technology nodes.

Fig. 20a shows the g_m Pelgrom plot for FinFETs with different S/D Epi. stacks (Epi-I and Epi-II as discussed in Section IV). The $A_{\Delta gm}$ for Epi-II decreases by $\sim$14%. This improvement is because of the reduced R_{SD} variation (higher Epi doping and optimized Epi-stack [17]) for Epi-II (refer Fig. 20b) confirming the role of Epi-layers in R_{SD} variations.

Fig. 21a shows the g_m Pelgrom plot for FinFETs with different W_{fin}s. As shown, the $A_{\Delta gm}$, i.e., g_m variability increases for narrower W_{fin}. The decomposed components of g_m variability for two different W_{fin}s are shown in Fig. 21b. The higher g_m variability for thinner W_{fin} is because of the

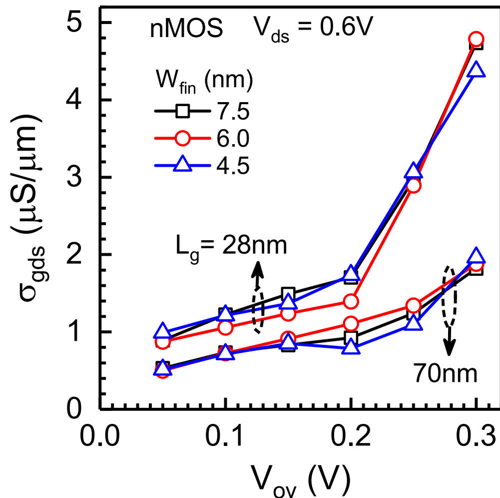

FIGURE 22. The standard deviation of g_{ds} (σ_{gds}) as a function of V_{ov} for different L_g and W_{fin}. For a particular L_g and V_{ov}, σ_{gds} is same for all W_{fin}s.

increased contribution of R_{SD} and μ variation. Overall, the R_{SD}, μ and T_{ox} variation will play a crucial role in g_m variability for upcoming technology nodes having narrower fins and thinner EOT.

Finally, to investigate the g_{ds} variability, we have plotted σ_{gds} as a function of V_{ov} for different W_{fin}s and L_gs, which is shown in Fig. 22. It is observed that for a particular L_g and V_{ov}, σ_{gds} is same for different W_{fin}s. Since, g_{ds} strongly correlates with DIBL (refer Fig. 8), the DIBL variation is mainly responsible for g_{ds} variation, which is same for different W_{fin} (refer Fig. 2).

VI. CONCLUSION

To summarize, we investigated in detail the effect of Sub-10nm fin width on FinFET analog performance and its variability. It was found that g_m degrades and g_{ds} improves for thinner fins resulting in less/zero analog performance benefit. Further, it was shown that the analog performance for thinner fins can be improved by proper optimization of R_{SD} and gate dielectric. The impact of process-induced total and random variability on g_m and g_{ds} was also explored. Using a systematic methodology, different sources responsible for g_m variation were separated. It was shown that μ, R_{SD} and T_{ox} variation were mainly responsible for the g_m variability and will become critical in upcoming technology nodes having narrower fins and thinner EOT.

REFERENCES

[1] M. T. Bohr and I. A. Young, "CMOS scaling trends and beyond," *IEEE Micro*, vol. 37, no. 6, pp. 20–29, Nov./Dec. 2017. doi: 10.1109/MM.2017.4241347.

[2] S. Wu *et al.*, "A 7nm CMOS platform technology featuring 4th generation FinFET transistors with a 0.027μm^2 high density 6-T SRAM cell for mobile SoC applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2016, pp. 2.6.1–2.6.4. doi: 10.1109/IEDM.2016.7838333.

[3] J. Singh *et al.*, "14-nm FinFET technology for analog and RF applications," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 31–37, Jan. 2018. doi: 10.1109/TED.2017.2776838.

[4] A. Wei *et al.*, "Challenges of analog and I/O scaling in 10nm SoC technology and beyond," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2014. pp. 18.3.1–18.3.4. doi: 10.1109/IEDM.2014.7047076.

[5] A. L. S. Loke *et al.*, "Analog/mixed-signal design challenges in 7-nm CMOS and beyond," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Diego, CA, USA, Apr. 2018, pp. 1–8. doi: 10.1109/CICC.2018.8357060.

[6] B. Parvais *et al.*, "Scaling CMOS beyond Si FinFET: An analog/RF perspective," in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2018, pp. 158–161. doi: 10.1109/ESSDERC.2018.8486857.

[7] V. Subramanian *et al.*, "Planar bulk MOSFETs versus FinFETs: An analog/RF perspective," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3071–3079, Dec. 2006. doi: 10.1109/TED.2006.885649.

[8] J. B. Chang *et al.*, "Scaling of SOI FinFETs down to fin width of 4 nm for the 10nm technology node," in *Symp. VLSI Technol. Dig. Tech. Papers*, Jun. 2011, pp. 12–13. doi: 10.1109/ESSDERC.2016.7599605.

[9] X. He *et al.*, "Impact of aggressive fin width scaling on FinFET device characteristics," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2017, pp. 20.2.1–20.2.4. doi: 10.1109/IEDM.2017.8268427.

[10] T. Chiarella *et al.*, "Towards high performance sub-10nm finW bulk FinFET technology," in *Proc. 46th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Lausanne, Switzerland, Sep. 2016, pp. 131–134. doi: 10.1109/ESSDERC.2016.7599605.

[11] M. S. Bhoir, N. R. Mohapatra, T. Chiarella, L. Å. Ragnarsson, J. Mitard, V. Terzeiva, and N. Horiguchi, "Effect of sub-10nm fin-widths on the analog performance of FinFETs," in *Proc. IEEE 3rd Electron Devices Technol. Manuf. Conf. (EDTM)*, 2019, pp. 7–9. doi: 10.1109/EDTM.2019.8731200.

[12] K. J. Kuhn *et al.*, "Process technology variation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2197–2208, Aug. 2011. doi: 10.1109/TED.2011.2121913.

[13] S. Dongaonkar, S. P. Mudanai, and M. D. Giles, "From process corners to statistical circuit design methodology: Opportunities and challenges," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 19–27, Jan. 2019. doi: 10.1109/TED.2018.2860929.

[14] P. Kushwaha *et al.*, "Predictive effective mobility model for FDSOI transistors using technology parameters," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Aug. 2016, pp. 448–451. doi: 10.1109/EDSSC.2016.7785304.

[15] M. S. Bhoir and N. R. Mohapatra, "Impact of BOX thickness and ground-plane on non-linearity of UTBB FD-SOI MOS transistors," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon (EUROSOI-ULIS)*, Mar. 2018, pp. 1–4, doi: 10.1109/ULIS.2018.8354769.

[16] T. Matsukawa *et al.*, "Fluctuation analysis of parasitic resistance in FinFETs with scaled fin thickness," *IEEE Electron Device Letters*, vol. 30, no. 4, pp. 407–409, Apr. 2009. doi: 10.1109/LED.2009.2014180.

[17] E. Rosseel *et al.*, "Selective epitaxial growth of high-P Si: P for source/drain formation in advanced Si nFETs," *ECS Trans.*, vol. 75, no. 8, pp. 347–359, 2016. doi: 10.1149/07508.0347ecst.

[18] T. Tezuka *et al.*, "Observation of mobility enhancement in strained Si and SiGe Tri-gate MOSFETs with multi-nanowire channels trimmed by hydrogen thermal etching," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2007, pp. 887–890. doi: 10.1109/IEDM.2007.4419092.

[19] Y. Wu *et al.*, "Optimization of fin profile and implant in bulk FinFET technology," in *Proc. Int. Symp. VLSI Technol. Syst. Appl. (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 2016, pp. 1–2. doi: 10.1109/VLSI-TSA.2016.7480517.

[20] T. Matsukawa *et al.*, "Decomposition of on-current variability of nMOS FinFETs for prediction beyond 20 nm," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2003–2010, Aug. 2012. doi: 10.1109/TED.2012.2196766.

[21] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989. doi: 10.1109/JSSC.1989.572629.