Analog Line Driver with Adaptive Impedance Matching

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***Abstract*— A new principle for an adaptive line driver is presented. This type of line driver can adapt its output impedance automatically to the applied load. This results in automatically corrected output impedance for different cables with terminations. Also, the line-driver output impedance becomes insensitive to process variations. As an example, a line driver for analog video signals has been designed. The circuit operates from a 2.4-V supply in a 0.35-μm CMOS technology. The realized circuit adapts between 38 and 85 Ω loads, has total harmonic distortion of < -50 dB at 1.2 V_{pp} for 0–10 MHz, 0.09-mm^2 area, and 9-mW static power consumption.**

***Index Terms*—Adaptive circuits, analog circuits, line driver.**

I. Introduction

TRANSMISSION lines are widely used for transportation of electrical signals. To minimize reflections, the source and load impedances of the transmission line have to be equal to the characteristic impedance of the line. For example, analog video applications typically use 75 and 50 Ω as a standard for instrumentation.

Fig. 1 shows two basic ways to drive a transmission line. In the configuration of Fig. 1(a), the line is driven by a voltage source with series resistance R_s [1]. The disadvantage of this configuration is that half the voltage $V_{\rm in}$ is lost across R_s. If an output voltage $V_{\rm out}$ of 1.5 V is desired, $V_{\rm in}$ must be 3 V. This becomes a problem if the supply voltage is lower than 3 V, which is the case for modern deep submicrometer CMOS processes. For low supply voltages, the configuration of Fig. 1(b) [2] is more attractive. Here, the line driver is replaced by its Norton equivalent, and no signal voltage is lost. However, half the signal *current* is lost through R_s. A 1.5-V signal across an R_s of 75 Ω results in a current loss of 20 mA, which is unattractive. If the resistor is integrated, both configurations have another disadvantage, which is sensitivity to process variations. Typical numbers for the spread of a poly-resistor are $\pm$30%, resulting in $\pm$30% spread in line-driver output impedance; and $\pm$15% spread in $V_{\rm out}$.

This paper describes a line driver without voltage or current loss in R_s. Furthermore, the line driver adapts its output impedance automatically to a value equal to the applied load. The advantages are impedance insensitivity to process variations and automatic adaptation of its output impedance if another load is applied. Consequently, if another (well terminated) cable with another characteristic impedance is connected, the line driver automatically tunes to the correct output impedance. For transporting digital signals over printed circuit boards, adaptive line drivers do exist [3], [4]. However, these need external components, a complex control scheme, and/or a separate return path from the receiving side. Moreover, these drivers are not suited for analog signals. The line driver presented in this paper is intended for *analog* signals.

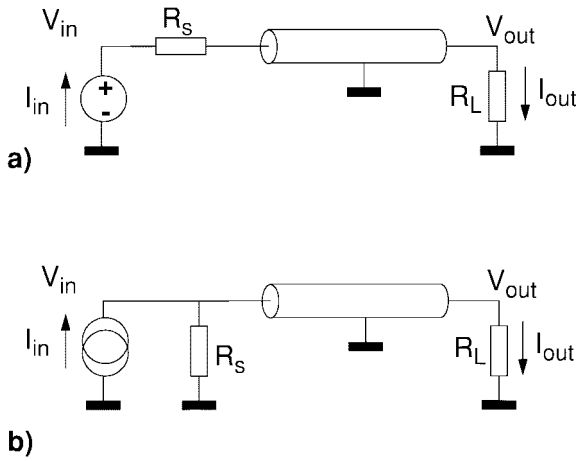

Fig. 1. Two classical ways to drive a transmission line: (a) Voltage source with series resistor R_s, resulting in voltage loss across R_s. (b) Current source with parallel resistor R_s, resulting in current loss in R_s.

In Section II, the basic idea of the line driver is explained. In Section III, this basic idea is applied in an analog baseband video line driver. In Section IV, the experimental results are given and conclusions are drawn.

II. Basic Idea

Fig. 2 illustrates the new line-driver architecture. For the sake of understanding, the line driver is explained in three steps. The first step in Fig. 2(a) shows a linear transconductor gm_1 with transconductance gm driving the line, which is modeled by a resistor R_L. The output current $gm \cdot V_{\rm in}$ is fed into R_L, resulting in an output voltage $V_{\rm out} = gm \cdot V_{\rm in} \cdot R_L$. Suppose the transconductance gm is electronically tunable via a "gm-control voltage" $V_{\rm control}$ and that by some means, gm is tuned to be equal to $1/R_L$. In that case, the voltage gain

Manuscript received April 28, 1998; revised July 21, 1998.

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Publisher Item Identifier S 0018-9200(98)08863-5.

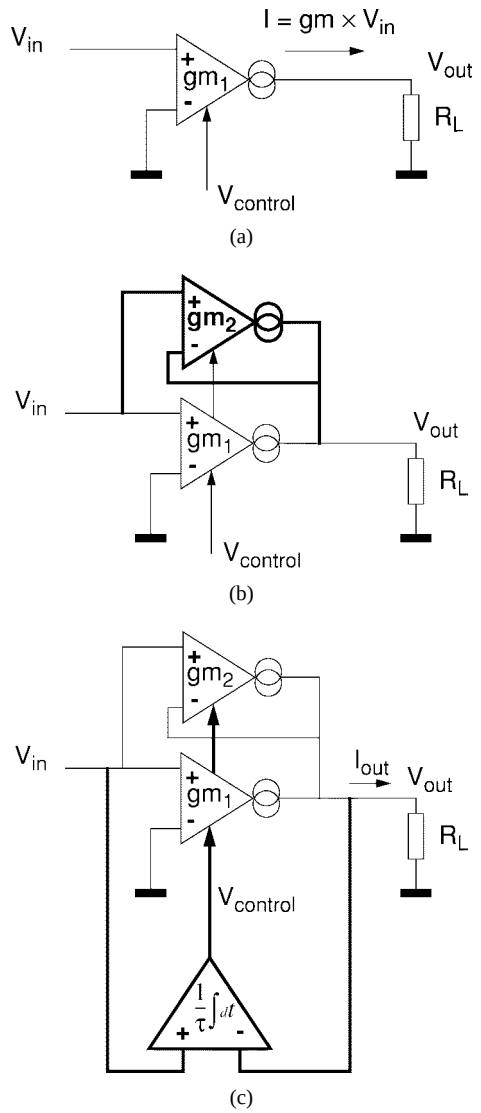


Fig. 2. The adaptive line driver principle in three steps. (a) A single transconductor gm_1 has an infinite output impedance. (b) Adding gm_2 results in an output impedance equal to $1/gm$. (c) The control loop tunes gm equal to $1/R_L$, and the output impedance is equal to R_L. No voltage or current is lost in the output impedance of the line driver.

equals one, and neither voltage nor current is lost. However, the output impedance of the circuit of Fig. 2(a) is infinite.

In Fig. 2(b), a second transconductor gm_2 is added. This transconductor is supposed to be equal to gm_1 and is connected to the same V_{control}. Now the output resistance of the circuit is

$$R_{\text{out}} = \frac{1}{gm} \tag{1}$$

which is equal to R_L if $gm = 1/R_L$. The gain of the circuit is defined as $V_{\text{out}}/V_{\text{in}}$ in the absence of a reflected wave

$$\text{gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2gmR_L}{1+gmR_L}. \tag{2}$$

If $gm = 1/R_L$, the gain is one. V_{out} of the line driver is now equal to

$$V_{\text{out}} = V_{\text{in}} + V_{\text{reflect}} \tag{3}$$

where V_{reflect} is a reflected wave. If $V_{\text{reflect}} = 0$, then $V_{\text{out}} = V_{\text{in}}$ and gm_2 has zero differential input voltage. The output current of gm_2 is thus zero. If V_{reflect} is unequal to zero, then gm_2 only sees the reflected wave and gm_2 provides the correct output impedance. Therefore, in this configuration, no voltage or current is wasted.[1] The remaining problem is guaranteeing that gm is equal to $1/R_L$. If $gm = 1/R_L$, then V_{out} equals V_{in}, assuming no reflected waves. This condition is met for dc and very low frequencies; at high frequencies, reflections may cause V_{out} to be unequal to V_{in}. If a control loop is added that controls gm in such a way that the average values of V_{in} and V_{out} are equal, then gm is automatically correct. This is shown in Fig. 2(c). Here, the control loop is implemented with an integrator. The resulting voltage V_{control} adjusts gm until it is equal to $1/R_L$. The control loop operates on the dc—or low frequency—content of the input and output voltages. For this reason, it is important that a dc path exists with correct load resistance from line-driver output to ground. This means the load must be resistive and equal to the characteristic impedance of the line. The load may not contain a coupling capacitor, or transformer. This limits the application of the line driver. For other applications, a different tuning loop, operating at a higher frequency, is needed. Also, for long cables, the dc resistance of the cable will affect the accuracy of the tuning mechanism.

The control loop of Fig. 2(c) has negative feedback as long as the average input voltage is positive. This is easy to guarantee if the buffer is driven by an on-chip signal. If the average input voltage is less than zero, the loop has positive feedback and is unstable. For positive average input signals, the loop can always be made stable as long as the integrator time constant τ is large enough. Since τ has no relation to the bandwidth of the line driver, this degree of freedom can be used for making the control loop stable.

Two important properties of a line-driver circuit are the gain and output impedance. Since the line driver of Fig. 2(c) contains a low-frequency control loop, gain and output impedance versus frequency require attention. The gain versus frequency of the circuit of Fig. 2(c) is plotted in Fig. 3(a). The gain is equal to one for all frequencies, assuming that the transconductors have infinite bandwidth. For low frequencies, the gain is one thanks to the control loop, which forces V_{out} to be equal to V_{in}. At high frequencies, the control loop is inactive and the gain is one according to (2) and $gm = 1/R_L$. In conventional line drivers, the gain varies if the output resistance or if the load resistor varies. This new architecture maintains a constant gain.

The output impedance of the line driver can be calculated assuming a reflected wave. The output voltage of the line driver is given by (3), where V_{in} is held constant. The integrator in Fig. 2(c) generates a control voltage in response to V_{reflect} equal to

$$V_{\text{control}} = \frac{-1}{\tau} \int V_{\text{reflect}}\, dt \tag{4}$$

[1] At the transistor level, the circuit of gm_1 and gm_2 needs bias currents, which are lost. How this can be minimized is shown in Section III.

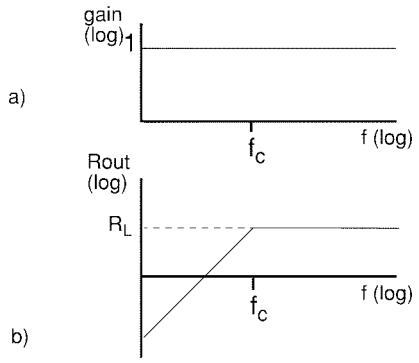


Fig. 3. (a) Voltage gain and output impedance (b) versus frequency of the line driver of Fig. 2(c).

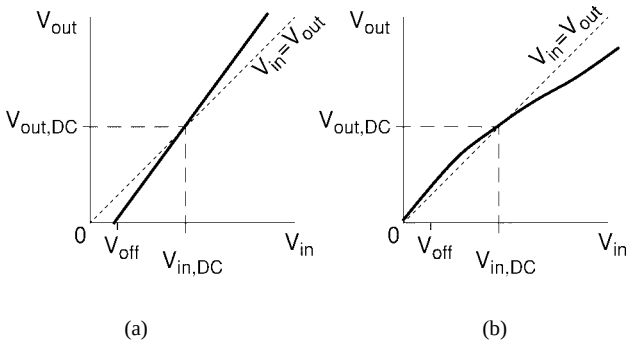


Fig. 4. (a) Illustration of the effect of offset on differential gain of the circuit of Fig. 2(c). (b) Illustration of the effect of distortion in gm on differential gain.

where τ is the integrator time constant. V_{reflect} in turn controls gm_1 and gm_2 to a value

$$gm_1 = gm_2 = gm_o + K_{gm}V_{\text{control}} \tag{5}$$

where gm_o and K_{gm} are constants. The output current I_{out} [see Fig. 2(c)] of the line driver consists of a constant part (I_{outDC}) and a part depending on V_{reflect} (or indirectly depending on V_{reflect} via V_{control}) denoted as I_{reflect}

$$I_{\text{out}} = I_{\text{outDC}} + I_{\text{reflect}} = gm_0V_{\text{in}} + K_{gm}V_{\text{control}}V_{\text{in}} - gm_0V_{\text{reflect}} - K_{gm}V_{\text{control}}V_{\text{reflect}}. \tag{6}$$

Since V_{control} depends on V_{reflect} as given by (4), it can be seen that

$$I_{\text{outDC}} = gm_o \cdot V_{\text{in}}. \tag{7}$$

Combining (6), (4), and (7), it can be seen that

$$I_{\text{reflect}} = \frac{-K_{gm}V_{\text{in}}}{\tau}\int V_{\text{reflect}}\,dt - gm_o \cdot V_{\text{reflect}} + \frac{K_{gm}V_{\text{reflect}}}{\tau}\int V_{\text{reflect}}\,dt. \tag{8}$$

Assuming that the first term dominates at low frequencies of V_{reflect} (i.e., $V_{\text{in}} \gg V_{\text{reflect}}$), it can be seen that—with (5)—the output impedance of the line driver of Fig. 2(c) behaves like an inductor (L_{out}) with a parallel resistor (R_L)

$$I_{\text{reflect}} = \frac{-1}{L_{\text{out}}}\int V_{\text{reflect}}\,dt - \frac{V_{\text{reflect}}}{R_L} \tag{9}$$

with

$$L_{\text{out}} = \frac{\tau}{K_{gm}V_{\text{in}}}. \tag{10}$$

Fig. 3(b) illustrates the output impedance versus frequency. At low frequencies, the output impedance is low due to L_{out} (the control loop tunes gm in such a way that V_{out} becomes equal to V_{in}, and thus the output impedance is low). At frequencies higher than a certain corner frequency fc, the control loop becomes inactive and the output impedance is equal to R_L. The corner frequency fc is given by

$$f_c = \frac{R_L}{2\pi L_{\text{out}}} = \frac{K_{gm}R_LV_{\text{in}}}{2\pi\tau}. \tag{11}$$

At low frequencies, the output impedance is low; however, no reflections will be present (assuming the cable is not extremely long). The reflections occurring at high frequencies will be correctly terminated.

The line driver of Fig. 2(c) has the correct output impedance for the frequency range of interest as long as the cable is perfectly terminated. If the cable is perfectly terminated, no reflections occur and the output impedance of the line driver is unimportant. However, if the line is not perfectly terminated (i.e., Z_L is *un*equal to Z_{cable}, where Z_{cable} is the cable impedance), a wave is reflected from the receiver side back to the line driver with a reflection coefficient ρ

$$\rho = \frac{Z_L - Z_{\text{cable}}}{Z_L + Z_{\text{cable}}}. \tag{12}$$

If the line driver operates correctly, its output impedance is equal to Z_L and the returning wave is reflected at the line-driver output back to the receiver side with the same reflection coefficient as given by (12). The result is that the receiver side sees a reflected wave of ρ^2V_{in}, which is small for reasonable matching of R_L to the cable. Therefore, it makes sense to have an adaptive output impedance, even if the cable is not perfectly terminated.

Offset and distortion in the transconductors affect the behavior of the tuning loop. If gm_1 or gm_2 have an offset voltage V_{off}, then the control loop will tune the differential gain to a value not equal to one. This is illustrated in Fig. 4(a). If the average input voltage is equal to V_{inDC}, then the loop controls gm in such a way that the average output voltage $V_{\text{out,DC}}$ is equal to $V_{\text{in,DC}}$. If offset is present, the differential gain of the circuit around $V_{\text{in,DC}}$ for small-signal frequencies higher than f_c is

$$\text{difgain} = \frac{V_{\text{in,DC}}}{V_{\text{in,DC}} - V_{\text{off}}}. \tag{13}$$

For example a 1-mV offset with $V_{\text{in,DC}} = 100$ mV results in a differential gain of 1.01 instead of 1. The error in differential gain is 1%.

Another nonideality is distortion in the transfer function of gm_1. This is illustrated in Fig. 4(b). The control loop tunes gm so that $V_{\text{in,DC}} = V_{\text{out,DC}}$. Since the transfer function for the combination of gm_1 and R_L is nonlinear, the differential gain will be unequal to one for signal frequencies higher than f_c. Distortion in gm_2 only affects the nonlinearity of the output impedance. Since gm_2 sees only a small V_{reflect}, this is not

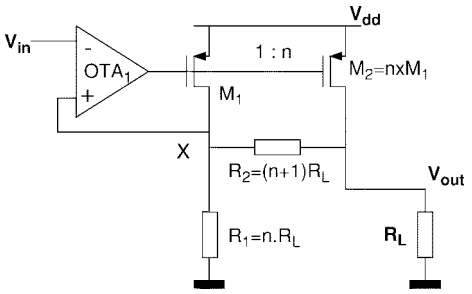


Fig. 5. Video line driver that is not yet tunable.

generally a problem. An analytical expression for predicting the differential gain error due to distortion in gm_1 is more complex since this effect depends on the type of distortion.

III. Analog Video Line Driver

In this section, a line driver is described for use as an analog output buffer for a resistive video digital-to-analog converter [1]. The technology is a standard digital 0.35-μm CMOS. The analog output voltage range is 0–1.4 V, with a THD less than -50 dB for a 1.2-V_{pp} signal up to 5 MHz. The cable impedance is fixed at 75 Ω, i.e., the line driver does not have to drive cables with different impedances.

In general, there is a tradeoff between linearity and tuning range for continuously tunable transconductors [5]. A high linearity results in a small tuning range, and a large tuning range has the drawback of poor linearity. To make an optimum circuit for this application, we chose to tune only for process variations. The transconductor must be tunable over such a range that the gm can be tuned to 13.3 mA/V (1/75 A/V) for all process spreads and temperature variations. For the process used, this tuning range is $\pm$30%.

If in Fig. 5 the resistor R_2 is ignored, this circuit is the implementation of the circuit in Fig. 2(a). The input voltage is copied to node x by OTA_1 and M_1. The resulting current flows through R_1 and is linearly proportional to the input voltage. This current is multiplied by a factor n in M_2 and driven to the load where a linear current-to-voltage conversion is obtained. The circuit is able to drive down to 0 V as required. The ratio n is typically large (in this case, 40) in order to save power and bias currents in the left half of the circuit. Normally, current mirrors have distortion due to finite output impedances and unmatched drain-to-source voltages. Here, both M_1 and M_2 have the same V_{gs} and the same V_{ds} so no distortion due to output impedance is present. If R_1 is equal to $n \cdot R_L$, then the transconductance of the circuit $n/R_1 = 1/R_L$ is correct. Tuning for process spreads in R_1 will be discussed later.

The next step is to implement the correct output impedance. Instead of adding another transconductor, as has been done in Fig. 2(b), the existing circuitry is used, with the addition of R_2. If R_2 is chosen to be equal to $(n+1)R_L = R_1 + R_L$, then the output impedance is equal to R_L. The voltage across R_2 is equal to V_{reflect}, and the current V_{reflect}/R_2 flows through M_1. This current is multiplied by the factor n of M_2 to the line driver output. The result is an output impedance equal to R_L. Note that the output impedance is provided by R_2, while no signal voltage or current is lost in R_2 because R_2 only sees reflections. The circuit of Fig. 5 is based on [6] and [7].

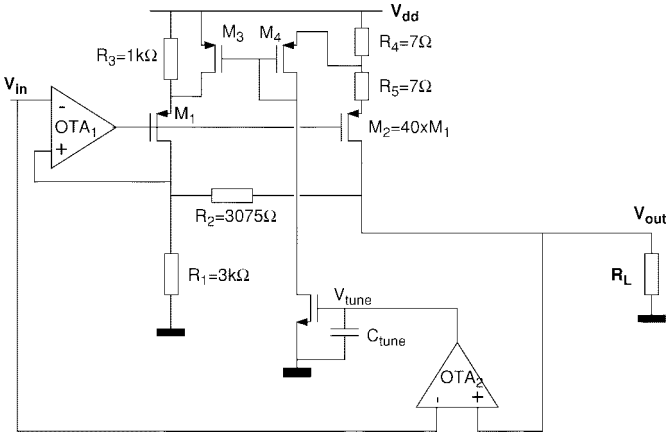


Fig. 6. Adaptive video line driver.

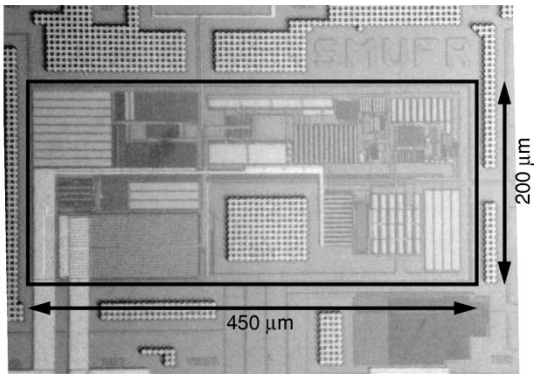


Fig. 7. Chip photograph.

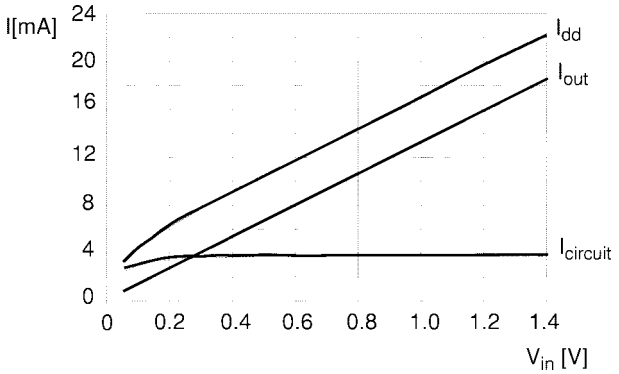
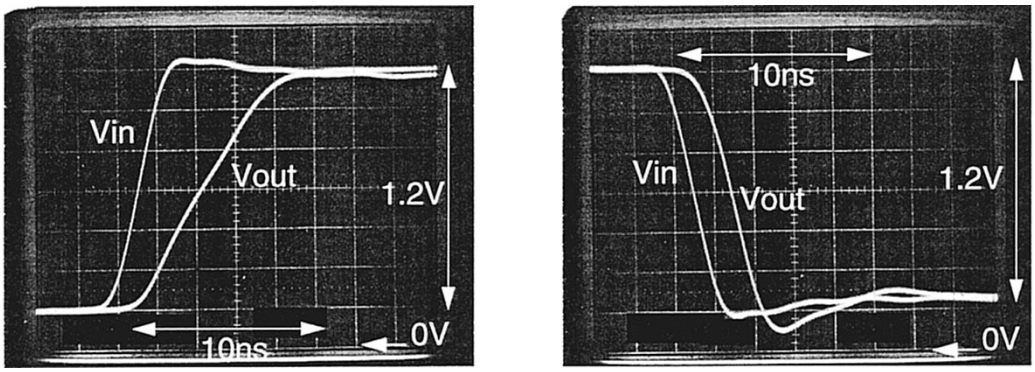


Fig. 8. DC measurements ($V_{dd} = 2.4$ V, $R_L = 75\ \Omega$), various currents versus input voltage.

Since the gain and output impedance are still sensitive to process variations in the circuit of Fig. 5, a tuning loop similar to that of Fig. 2(c) must be added. One way to implement a tunable gm is to replace R_1 and R_2 with MOSFET's acting as tunable resistors. However, it was difficult to achieve both the tuning range and the linearity, since the voltage over this circuit is relatively large (equal to the full swing input signal, at least for R_1). Therefore, the current ratio in M_1 and M_2 is tuned and R_1 and R_2 are fixed. An implementation of this principle is shown in Fig. 6.



(a) (b)

Fig. 9. Measured step responses ($V_{dd} = 2.4$ V, $R_L = 75\ \Omega$): (a) rising edge and (b) falling edge.

Here, the current ratio is electronically tunable via the voltage, V_{tune}. The two MOSFET's (M_1 and M_2) have source degeneration R_3 in parallel with M_3 and R_4 in series with R_5, respectively. The degeneration resistance of M_1 is electronically tunable via $V_{\text{tune}} \cdot M_3$, operating in the triode range, which behaves like a linear resistor since its gate-voltage variation equals half its drain-voltage variation. The drain current of an MOSFET in triode is given by

$$Id = \frac{K}{2}(2(V_{gs} - V_T)V_{ds} - V_{ds}^2). \tag{14}$$

If $V_{gs} = V_{gso} + (1/2)V_{ds}$, then

$$I_d = K(V_{gso} - V_T)V_{ds} \tag{15}$$

and M_3 acts as a linear, tunable resistor. Due to second-order effects, such as mobility reduction, distortion is present. By shunting R_3 in parallel to M_3, a tradeoff in tuning range and linearity is made. Transistor M_4 is used to generate the V_{gs0} of M_3; the resistors R_4 and R_5 generate the required 0.5 $V_{ds,M3}$.

The integrator of the control loop is implemented with OTA_2, whose output current is integrated in C_{tune}, resulting in V_{tune}; this in turn controls the current ratio. It is important that the bandwidth of the control loop is small. Therefore, gm_2/C_{tune} must be small, where gm_2 is the transconductance of OTA_2. OTA_1 and OTA_2 in Fig. 6 are simple folded-cascode amplifiers.

R_1 and R_2 are subject to process spreads. However, the control loop tunes the ratio of currents in M_1 and M_2 in such a way that the voltage gain is one. Matching between R_1 and R_2 will be inherently good thanks to integration. The output impedance of the line driver is slightly lowered by the drain-source resistance r_{ds2} of M_2 (operating in saturation). Therefore, R_2 has been designed to be somewhat larger than $R_1 + R_L$. Deviation from this designed value or spread in r_{ds2} will result in an error in output impedance and not in a gain error. This error in output impedance, however, is an order of magnitude less than it would be in an integrated nonadaptive line driver.

IV. Experimental Results

The line driver has been realized in a 0.35-μm standard CMOS process. A chip microphotograph is shown in Fig. 7. The area is 0.09 mm^2 including the bias generator. The circuit operates from a 2.4–3.6 V supply voltage. All resistors are implemented in polysilicon. M_1 is 54/0.4 and M_2 is 2160/0.4. All measurements described below have been taken at the minimum supply of 2.4 V.

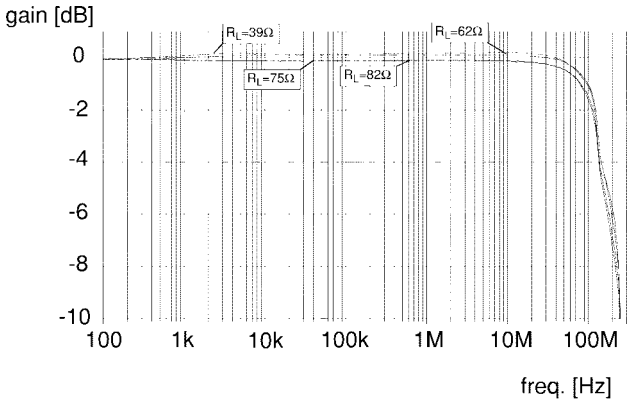
First, the line driver is characterized at dc for a 75-Ω load. This means that the control loop is active and thus $V_{\text{out}} = V_{\text{in}}$. Fig. 8 shows various currents. From this figure, it can be seen that the circuit draws a static current of 3.8 mA, while the output current is up to 19 mA.

Fig. 9 shows the large signal step response of the line driver when driving a 75-Ω load. This slew rate for rising edges is 167 V/μs. The slew rate is limited by OTA_1 driving the gate of M_2. The slew rate is more than sufficient for this application. The falling edge has a larger slew rate since the sink current through R_L can be large.

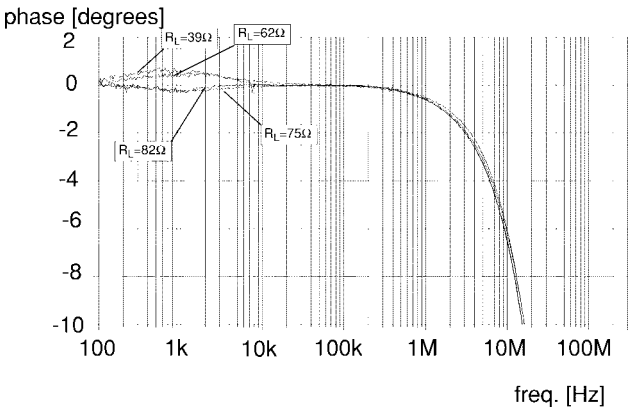
The tuning range of this line driver for large signals has been measured. The tuning range appeared to be from 38 to 85 Ω. Note that this tuning range may be different in another processed batch. The tuning range is that which is sufficient to guarantee that 75 Ω is within the tuning range for all process batches. The output voltage range is from 0 to 1.4 V.

The gain versus frequency was measured with an HP 4195 network analyzer. Fig. 10 shows the small signal gain for various loads for 0.7-V dc bias at the input. For low frequencies, the gain is 0 dB for all loads, thanks to the tuning loop. For frequencies higher than f_c, which is 4 kHz for 0.7-V input, the gain deviates 0.1 dB (1%) for different loads. This is due to offsets and nonlinearities in the line driver, as has been illustrated in Fig. 4. The small signal bandwidth of the circuit is 130 MHz and is determined by OTA_1 with its capacitive loading in Fig. 6.

The output impedance was measured with a HP 4195 network analyzer. Fig. 11 illustrates the output impedance (magnitude and phase) for different loads ranging over the complete tuning range. The dc input voltage is held constant at 0.7 V. For low frequencies, the output impedance is low due to the control loop. For frequencies higher than f_c (4 kHz), it is clearly seen that the circuit adapts to the load. The output impedance is resistive and almost equal to the applied load. At high frequencies, the bandwidth of OTA_1 in combination with its capacitive load results in inductive behavior of the



(a)



(b)

Fig. 10. (a) Measured voltage gain versus frequency for various loads of the line driver ($V_{dd} = 2.4$ V, $V_{\mathrm{in}\,\mathrm{DC}} = 0.7$ V). (b) Measured phase response of the line driver.

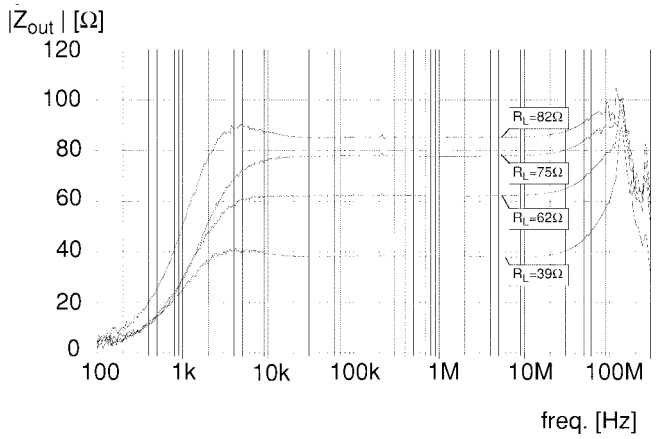
TABLE I
SUMMARY OF EXPERIMENTAL RESULTS ($V_{dd} = 2.4$ V)

parameter	value
Vdd range	2.4V .. 3.6V
Idd (static)	3.8mA
technology	0.35µm CMOS, 5AL, 1PS
area	0.09mm^2
impedance tuning range	38 .. 85Ω
output voltage range	0.. 1.4V @75 Ω
THD (1.2Vpp, 0..10MHz)	<-50dB @75 Ω
noise (0.. 5MHz)	67 µV @75 Ω
Dynamic range	77dB @75 Ω
-3dB bandwidth	130 MHz
Slew rate (rise)	167 V/µs @75 Ω
diff. gain (f=4.43MHz)	2% @75Ω
diff. phase (f=4.43MHz)	0.5° @75Ω

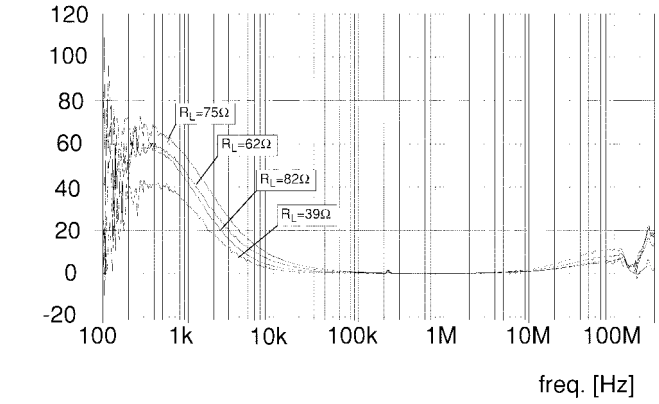
output impedance. For the frequency range of interest (up to 10 MHz), the output impedance is correct.

The distortion was measured with a spectrum analyzer. The distortion versus frequency is plotted in Fig. 12 for 1.2-V_{pp} sine waves around a 0.7-V dc bias. The distortion is mainly second order and is less than −50 dB for frequencies up to 10 MHz.

Table I summarizes the experimental results.



(a)



(b)

Fig. 11. (a) Measured magnitude of complex output impedance Z_{out} as a function of frequency for different loads. ($V_{dd} = 2.4$ V). (b) Measured phase of Z_{out} versus frequency for different loads.

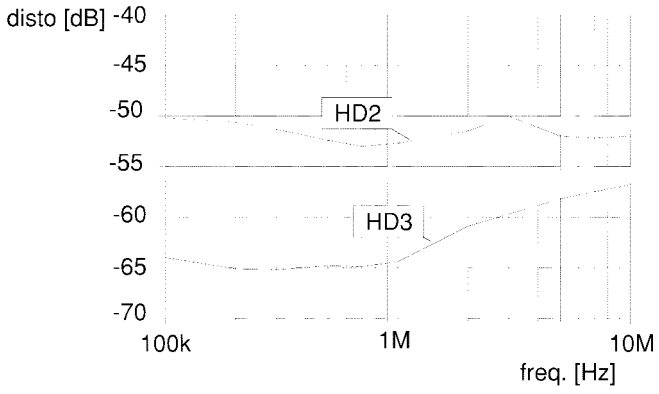


Fig. 12. Measured second and third harmonic distortion versus frequency. $V_{\mathrm{in}} = 0.7 + 0.6\sin(\omega t)$ [V].

V. CONCLUSIONS

A new principle for an adaptive line driver for analog signals has been presented. The main features of this line driver are the absence of voltage or current loss in output impedance and the adaptivity of its output impedance. This adaptive output impedance results in automatically correct output impedances

for different characteristic impedances. The output impedance is automatically tuned to a value equal to the applied load. So the line-driver output impedance also becomes insensitive to process variations. The effects of some nonidealities have been described.

As an application of the principle, a line driver for analog baseband video signals has been designed in a 0.35-μm CMOS technology. The circuit has been designed in such a way that the impedance tuning range is just enough to cover 75 Ω for all process corners. More tuning range would result in more distortion or a more complex circuit. For the given process run, the circuit adapts between 38- and 85-Ω loads. The circuit operates from a 2.4-V supply voltage and has a THD < -50 dB at 1.2 V_{pp} for 0–10 MHz, 0.09 mm^2 area, and 9-mW static power consumption.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their comments.

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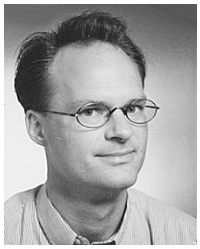

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