Analysing the Effect of Process Variation to Reduce Parametric Yield Loss

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Abstract – **For several decades, the output from semiconductor manufacturers has been high volume products with process optimisation being continued throughout the lifetime of the product to ensure a satisfactory yield. However, product lifetimes are continually shrinking to keep pace with market demands. Furthermore there is an increase in 'foundry' business where product volumes are low; consequently it is no longer feasible to optimise the process during the product lifetime resulting in an increase in parametric yield loss. This paper describes the use a combination of two statistical tools namely Design of Experiments (DoE) and Response Surface Modelling (RSM) which permit the identification and modelling of those process parameters whose variation which will impact most on the performance of a circuit. The efficiency of this approach, compared to using a Monte Carlo analysis, is demonstrated with respect to a Mutual Exclusion Element (MUTEX) which is used extensively in synchronisers where process variations can have considerable impact on circuit performance. To obtain the same modelling accuracy, the Monte Carlo approach would require large number of simulations compared to nine using the DoE scheme with the low computational overhead. This method can be used by semiconductor manufacturers and design house alike to bridge the gap between manufacture and design.**

Index Terms – **DFM, RSM, Strained silicon, Variability, Yield,**

1. INTRODUCTION

For the past 30 years or so, device scaling has been the mainstay for the semiconductor industry to continue delivering great functionality and performance at lower cost to the end user [1]. However, concomitant with the advantage offered by device scaling is the problem of process variability which creates wide fluctuations in circuit performance [1]. As the processing nodes become smaller the effects of variability are increasing [1]. In the pre-350 nm technology era, the two main sources of variability, namely layout and process, could be considered together to define the overall process variations [1]. However the layout dependent variations in the deep nanometre design node need to be considered as part of the design flow. Also in the past, the effect of different process steps on variability were lumped together in an overall variability model for a given characteristic, for example threshold voltage; it is now essential to consider effects, on any given characteristic, of the individual process steps (design for manufacturing). Furthermore the market place is also changing, previously this was dominated by high volume product runs such as memories and microprocessors where, by the time volume production was reached, any systematic yield losses were rendered insignificant. Today there is a growing increase in 'foundry' business comprising small numbers of diverse products.

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A new manufacturing yield loss called 'product systematic' yield loss has arisen which is very dependent upon the class of products for example microprocessors, memories, DSP chips, game chips etc. Consequently there is an increasing need for semiconductor process versatility, which can be adopted by a diverse customer base. Central to ensuring customer satisfaction of the manufactured product is an understanding of the effects of process variation on customer designs. Previously the effects of process variations were accounted for by incorporating artificial distributions in SPICE models [2]. Later Monte Carlo analysis [3] was introduced, however this is time consuming and computationally inefficient. An alternative approach, having reduced complexity is outlined in this paper, which can identify important processing parameters which affect specific device characteristics. Although the procedure is meant to be used, primarily, with semiconductor processing companies, it may also be used by design houses in order to identify the important processing parameter to give a predictive performance thereby bridging the gap between design and manufacture. Ideally, by employing the techniques discussed in this paper, a designer can analyse his design to identify the acceptable variation of the most important process parameters and seek out the semiconductor manufacture who could supply the required process to best satisfy the design performance specifications.

The paper describes an efficient statistical method that enables the identification of process variations which highly impact the circuit parameters that are deemed to be critical by the circuit designer in order to achieve some performance criteria; during the manufacturing process these parameters can be controlled more closely to within required limits hence enhance the overall yield. The technique for parameter identification is described in Section 2 and employs a combination of statistical methods namely Design of Experiments (DoE) and Response Surface Modelling (RSM) which are more computationally efficient than Monte Carlo methods [4]. The integration of DoE/RSM methods to find the impact of process variation on circuit parameters is described in Section 3, followed by the application of the method, in Section 4, to the characterisation of Mutual Exclusion Element (MUTEX) which is widely used circuit block in asynchronous circuit design. A discussion of the results is given in Section 5 followed by conclusions in Section 6.

2. METHOD OF PARMETER IDENTIFICATION

Previously Monte Carlo Analysis was the generally adopted approach used to study the effects of parameter variability in a wide range of applications [3]. However, when the number of parameters considered increases, this approach, although accurate, is computationally inefficient.

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The technique described in this paper to identify and model semiconductor process parameters whose variability would impact most on the circuit characteristics, considered critical by the designer, is realised through a two phase process using DoE and RSM statistical tools [5, 6]. DoE is a strategy to create a set of experiments in which the range of input variables can be altered systematically to enable any correlation between variables to be ascertained, to determine the main contributing factors to the variation for example, the design parameters of interest [7]. In this particular application the 'experiments' in DoE are simulations. Within the DoE procedure the Plackett-Burman (PB) screening technique is incorporated to screen the most significant parameters which will subsequently be used in the second phase [7].

Experimental design formally represents a sequence of experiments to be performed, expressed in terms of factors or design variables set at specified levels i.e. predefined values. It is represented mathematically by a matrix where the rows represent the experimental runs and the columns denote the particular factor setting for each factor in each run. The most basic experimental design is a full factorial design. The most common designs are the 2^k (for evaluating main effects and interactions) and 3^k designs (for evaluating main and quadratic effects and interactions) for *k* factors at 2 and 3 levels, respectively. Fractional factorial designs are used when the full factorial experiments are costly and the numbers of design points are large. The most common second-order design, aimed at reducing the number of design points is central composite design (CCD) which is used to undertake RSM in this work [6]. It is a two level factorial or fractional factorial design, augmented by centre points (all values of the factor are at their mid-range) and axial or star points which gives estimation of the curvature of the response surface. RSM involves mapping the input space into the response space and helps in studying statistical significance of each input parameter through second order regression analysis [6]. The polynomial function used to approximate the output parameter, y is a second order model of the form:

$$\hat{y} = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i=1}^{k} \beta_{ii} x_i^2 + \sum_{i=1}^{k} \sum_{j=1}^{k} \beta_{ij} x_i x_j$$

where k is the number of input variables, x_i is the i^{th} input variable and β is the RSM coefficient calculated using least squares regression analysis to fit the response surface approximation.

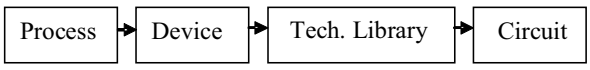

Fig. 1 CAD simulator flow

Having identified the most influential process parameters it is essential to reflect the effects of the process variations onto circuit performance. Hence it is necessary to generate a technology library which embodies the effect of process variations in the circuit models used at the higher levels of abstraction in the design hierarchy. In creating a technology library a number of CAD tools are used in sequence as shown in Figure 1; namely TSUPREM4 (Process Simulator) [8], MEDICI (Device Simulator) [9], AURORA (Parameter Extraction Program) [10] and PSPICE (Circuit Level Simulator) [11], DoE analysis is performed using the statistical package MINITAB [12].

3. ANALYSIS OF THE IMPACT OF PROCESS VARIATIONS ON CIRCUIT PARAMETERS

As a demonstration of the above procedures a Mutual Exclusion Element (MUTEX) was selected to study the impact of process variations on particular circuit parameters. The MUTEX circuit is an important building block in asynchronous circuit design and is used extensively in synchronisers; the MUTEX is also used in novel time measurement circuits [13-15]. In the design of the MUTEX two critical timing parameters, t_{off} (input time difference at which the MUTEX output changes) and t_m (time at which the output of the latch gets a valid voltage level), are important for the correct functioning of the circuit, although they are also susceptible to the effects of process variations.

The implementation technology chosen for the MUTEX is strained silicon (s-Si). In recent years industry has been considering the potential of 'band-gap' engineered [16 -20] s-Si devices in high speed low threshold circuits which results from improved carrier mobility and also for its compatibility with standard silicon process technology. The amount of strain in the s-Si device can be considered as a process parameter and hence gives an easy way of comparing the performance of the MUTEX implemented in the straightforward silicon process technology (0% strain) and one implemented in the s-Si technology.

The methodology followed to study the impact of process variations on the MUTEX is shown in Figure 2 in which there are two paths. The result from the first path is the benchmark from the MUTEX, and the second is the stochastic output based on the variability of process and device parameters using DoE. The best process parameters can then be selected, depending upon the application of the circuit, to ensure a good yield. In undertaking the analysis for yield enhancement a range of CAD tools were used. Process and device simulations were performed for a range of technology nodes, namely 300 nm down to 65 nm. The device dimensions and other physical parameters for deep submicron high performance devices were taken from MASTAR [21] and ITRS [22]. The MEDICI simulator was calibrated with previously published data to choose proper models from a variety of physical models [1] and the calibration of the model and other physical parameters for strain were based on previously published data [16-20, 23]. Details of device fabrication and electrical characterisation are described in [19, 20].

Figure 3 shows the steps undertaken in the analysis of the effects of process variation in the strained silicon process. The electrical characteristics of s-Si and conventional Si n- and p-MOSFETs are applied to AURORA parameter extraction simulator for optimization and extraction of PSPICE models. The s-Si and Si PSPICE transistor library based on different strain conditions and a range of technology nodes are developed as part of the work. These transistors are used in the design of a MUTEX

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in PSPICE. The simulations are performed to evaluate the t_m and t_{off} of s-Si and Si based MUTEX under different strain conditions, operating conditions and dimensions.

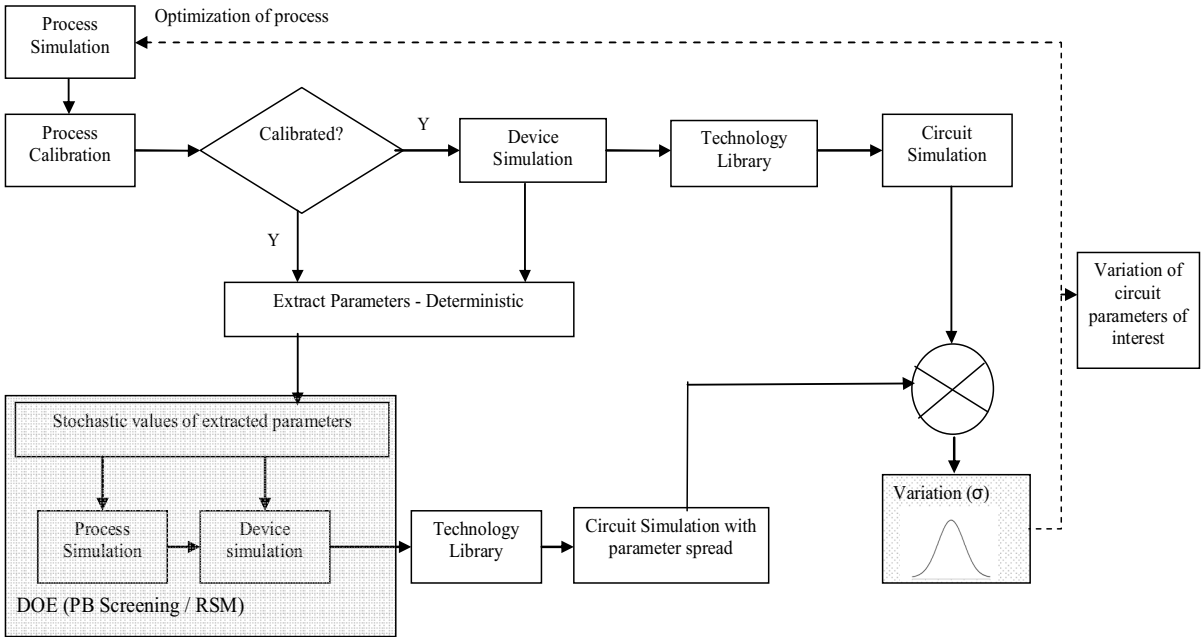

Fig. 2 Methodology to study the effect of process variations to reduce parametric yield loss

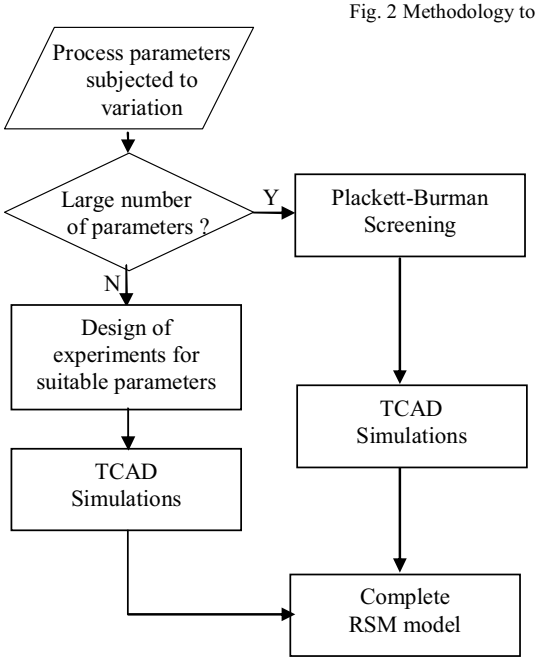

Fig. 3 Flow chart of the variability analysis

To study the impact of variability of process parameters on circuit characteristics the main process parameters were identified from a chosen 65nm process. Previously a Monte Carlo analysis would have been the obvious choice to study the effects of variability as it is the conventional statistical approach when considering large amounts of data. However, to study the effects of the variation of many processing parameters on a circuit, a large number of process, device and circuit simulations would need to be done which is highly complicated, computationally inefficient and time consuming but accurate using the Monte Carlo approach. This is due to the fact that the accuracy of the results from Monte Carlo analysis depends on the number of random samples, a large number of finite samples are necessary to get reasonable accuracy for a complex system. Consequently, a different statistical method called DoE [12] was used where there is a fixed number of simulations (2^n+2^n+1) to get very good accuracy compared to Monte Carlo approach [4]. Thereafter, in DoE any response and its distribution can be calculated for any number of control factors without the need for further simulation runs.

The DoE method involves screening the process parameters and modelling the screened ones using RSM. The state of the art 65nm technology is chosen as the technology node of choice as its variability is seen to be larger in comparison to similar 300nm technology node [1, 24]. Nineteen parameters were identified from the 65nm process as the important parameters at different process steps. The parameters were all varied over a range of 10% from their nominal values. However, the temperatures are varied as $\pm 5^oC$ from the nominal. If Monte Carlo Analysis was used in this instance over 600K simulations would have been required to achieve a reasonable accuracy to model the parameters. This is to be compared to just nine simulations (2^n+2n+1, where n is the number of parameters) [4, 5, 12, 24] in the case of DoE with comparable accuracy; only nine simulations are required as only two parameters are identified as the most significant parameters after the screening technique. Parameter screening is achieved using Plackett-Burman (PB) method. From the screening procedure the most significant parameters were identified as oxide thickness and substrate doping. The effective length (L_{eff}) is not considered separately as L_{eff} depends on substrate doping concentration and other process conditions. The significant parameters are chosen based on

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a threshold value, decide by the user, below which it is consider that the parameter is insignificant. The amount of strain was also considered as an important parameter, however it was added to the significant parameters obtained after screening to model the variability using RSM; this permitted a comparison between silicon and strained silicon technologies to be made.

4. ANALYSIS OF MUTEX DESIGN PARAMETERS WITH PROCESS VARAIBILITY

During the variability analysis the supply voltage was fixed at 1.2V as suggested by ITRS for 65nm technology node. Here the supply voltage conditions are not varied as the ultimate aim of undertaking DoE is to identify the significant process parameters (and their variations) which have the highest impact on t_m and t_{off}. Oxide thickness (t_{ox}), substrate doping (N_{sub}) and strain (amount of bi-axial strain in the channel due to an applied stress) have been identified as the significant parameters for the analysis. T_{ox} and N_{sub} are varied by ± 10% and strain is varied from 0% (conventional Si technology) to 0.99% (s-Si). The strain is limited to 0.99% as bi-axially strained devices are found to give no enhancement above 0.99% strain in terms of mobility of electrons (n-MOS devices) [16-18].

Table. 1 The linear, square and interaction effects of process parameters on t_m and t_{off} of MUTEX.

Effects	Process parameter	t_m	t_{off}
		P values	P values
Linear	t_{ox}	0.654	0.746
”	N_{sub}	0.140	**0.016**
”	strain (%)	**0.008**	0.196
Square	t_{ox} x t_{ox}	0.989	0.742
”	N_{sub} x N_{sub}	0.999	0.800
”	Strain (%) x strain (%)	**0.028**	0.181
Interaction	t_{ox} x N_{sub}	0.580	0.336
”	t_{ox} x strain (%)	0.912	0.628
”	N_{sub} x strain (%)	**0.004**	**0.010**

The statistical p-values obtained from the process variability analysis are shown in Table 1. P-values provide the way of testing the relationship between the predictor (input variable) and response (output variable) [12, 24]. They are used to determine statistically significant terms in the analysis. The linear, square and interaction effects are also shown in the Table1; the terms with p-values ≤ 0.5 are statistically significant [12, 24]. From the linear effects it can be seen that strain is the most significant process parameter which impacts on t_m, and for t_{off} it is $N_{sub.}$ For square effects; the process parameter strain is also having the highest impact on t_m and t_{off} of MUTEX. However, amongst the interaction effects N_{sub} and strain are the significant parameters for t_m and t_{off} variations. Hence, strain is the most significant parameter; the amount of strain in the channel can be adjusted in the IC process to obtain required t_m and t_{off}. Schematic of a MUTEX is shown in Figure 4.

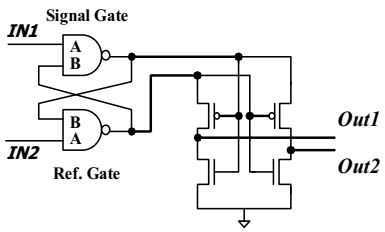

Fig. 4 Schematic of a MUTEX

Figure 5 shows the surface plot of the impact of the interaction effects of N_{sub} and strain on t_m of MUTEX. It can be seen that t_m is exhibiting a large range of variation for 0% strain (conventional Si) when N_{sub} is changing from -10% to +10% which is undesirable, with t_m decreasing when the amount of strain applied in the channel of transistors is increasing. It can also be seen that the variation of t_m with N_{sub} in 0.99% strain is not high compared to the lowest strain (0%) which indicates that strained silicon is, potentially, a better technology with which to implement the MUTEX compared to the conventional silicon process.

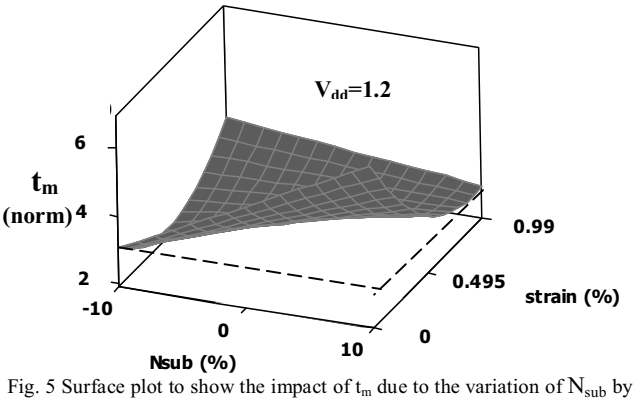

Fig. 5 Surface plot to show the impact of t_m due to the variation of N_{sub} by 10% and strain varying from 0.0% to 0.99% of MUTEX.

From the Figure 5 it can concluded that (see the dotted lines) if the transistors are used with 0.99% bi-axial strain in the channel with N_{sub} changed to 10% from the nominal value, we would obtain the best MUTEX with least t_m, thereby increasing the efficiency of circuits based on this MUTEX.

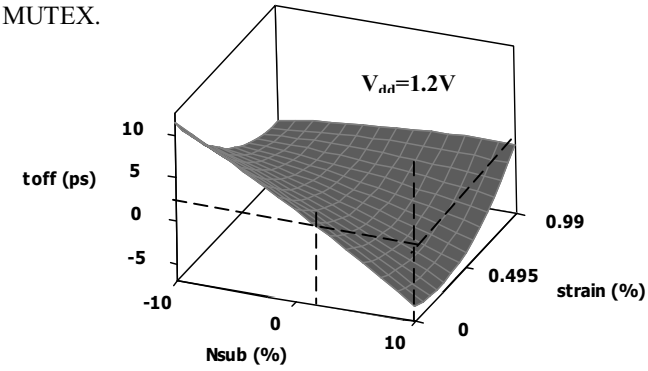

Fig. 6 Surface plot of the impact of t_{off} due to the variation of N_{sub} by 10% and strain varying from 0.0% to 0.99% of MUTEX.

In the design of the MUTEX the second critical parameter is t_{off}. Figure 6 shows the surface plot of the impact of interaction effects of N_{sub} and strain on t_{off}. It can be seen that, similar to t_m, t_{off} is exhibiting a large range of variation for 0% strain (conventional Si) when N_{sub} is changing from -10% to +10% which is undesirable. When the strain in the channel of transistors is increasing it can seen that the variation of t_{off} with N_{sub} is not high compared to the lowest strain (0%) which gives an edge for the s-Si technology over the conventional Si. This can be attributed to the fact that the enhancement of mobility of electrons and holes are not the same in the case of s-Si [16-18] and hence the transconductance ratio and the change in threshold

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voltage is not the same as in conventional Si. As mentioned above the strain is found to be the most significant parameter which impacts on t_{off}. This is advantageous due to the fact that the amount of stress applied to the channel to create strain can be controlled by the Ge% in the wafer (bi-axial strain) or by the process steps in local strain (uni-axial strain). Dotted lines are drawn in the Figure 6 to find the t_{off} and N_{sub} for an equivalent strain of 0.99% (which is considered as the best strain for the lowest t_{off}). The N_{sub} is found to be +2% from the nominal value to get the best MUTEX.

Table 2 shows the validity of analysis developed for studying the impact of process variation on t_{off} and t_m using DOE/ RSM methods to enhance the yield. The validity of the analysis results has been checked using the R-square statistics. R-square is known as the coefficient of determination and is a statistical measure of how well the regression line approximates the real data points. R-square and adjusted R-square statistics represent the amount of variation in the response that is explained by the model. The R-square value always increases with the addition of an input variable, regardless of whether the additional variable is statistically significant or not. Hence, large R-square values give poor predictions of new observations or estimates of the response. Adjusted R-square is a modified R-square metric for the number of terms in the model. Unlike R-square, adjusted R-square may become smaller when unnecessary or additional terms are added. It can be seen from Table 2 that adjusted R-square is less for both t_m and t_{off}. This is due to the fact that t_{ox} is included in the analysis and is found not to be significant compared to the other two process parameters, N_{sub} and the amount of strain in the channel. This analysis can be used to select the best circuit under typical process conditions thereby avoiding the process optimisation which will incur severe cost.

Table. 2 The validity of the model.

	R-sq	R-sq (adj)
t_m	93.36%	81.41%
t_{off}	87.49	64.98%

5. CONCLUSION

Market demands for higher performance devices together with continual changes in process technology, reduced product volumes, increased product diversity and shorter lifetimes has resulted in process optimisation being no longer feasible for a given product; consequently there are, now, increasing concerns over product parametric yield losses. A combination of two statistical tools, DoE and RSM, has been shown to be a computationally efficient method to identify those process parameter which highly impact on circuit performance. The method has been shown to be more efficient than Monte Carlo Analysis (600K simulations compared to 9 for DoE). As a result of the relative simplicity of the DoE/RSM approach design houses can readily determine the most critical process parameters for a circuit, and flag these to the 'foundry' in order to minimise the potential parametric yield loss; thus bridging the gap between design and manufacture.

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