Analysis and Cell-Level Experimental Verification of a 25 kW All-SiC Isolated Front End 6.6 kV/400 V AC-DC Solid-State Transformer

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***Abstract*—Solid-state transformers (SSTs) could serve as interfaces between a medium-voltage (MV) AC grid and a low-voltage (LV) DC load or source, i. e., could be employed in applications with power supply character such as traction auxiliary supplies or rack-level power supplies in future datacenters. For handling the high input-side AC voltage and output side current, SSTs are typically realized as input-series output-parallel (ISOP) arrangements of multiple converter cells, whereby each cell comprises a medium-frequency isolation stage. This paper presents such a multi-cell 25 kW all-SiC MVAC-LVDC SST (6.6 kV AC to 400 V DC) based on the isolated front end (IFE) approach, which is an interesting alternative to the isolated back end (IBE) configuration mainly discussed in literature so far. The IFE concept is briefly explained, the main component stresses are derived, and a converter cell prototype is designed and tested. The 5 kW prototype cell features a power density of 1.5 kW/l (24.6 W/in3) and a measured peak efficiency of 97.5%. This is significantly higher than previously published data for IFE-based SSTs, and in the same range as what has been reported recently for industrial IBE-based SSTs. Thus, this paper confirms that the IFE approach can be a feasible and interesting alternative for realizing MVAC-LVDC SST systems with low complexity.**

***Index Terms*—Isolated AC-DC converters, isolated front end, isolated power factor correction, solid-state transformer.**

I. Introduction

VARIOUS low-voltage (LV) DC loads or sources with higher power ratings could benefit from a direct connection to the medium-voltage (MV) AC grid. Such applications with power supply character are, e. g., future rack-level power supplies for datacenters with power flow from the AC to the DC side, larger PV installations with power flow from the DC to the AC side, or battery storage systems requiring bidirectional power flow. Especially for cases where the available space and/or weight for the power conversion equipment is constrained (e. g., datacenters [1], [2], traction applications [3], future shipboard power systems [4], or possibly future all-electric aircraft [5]), solid-state transformers (SSTs) that realize the galvanic separation by means of medium-frequency (MF) transformers are a highly interesting option [6]. In addition, such systems could operate with a power factor close to unity at the MV grid and/or minimize the effects on the mains.

A. Isolated PFC Functionality Partitioning

Realizing galvanic isolation of input and output, (single-phase) power factor correction (PFC) functionality, and output voltage control requires four distinct tasks [7]: folding (rectification) of the AC grid voltage into a |AC| voltage, shaping of the input current (current shaping, CS), galvanic isolation (I), and output voltage regulation (VR). As shown in Fig. 1, there are different variants of how these functional blocks can be arranged and/or combined.

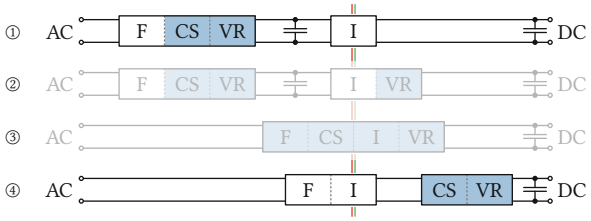

Fig. 1. Partitioning of the tasks required to perform isolation, PFC, and output voltage control: folding (F), current shaping (CS), isolation (I), and output voltage regulation (VR); blue stages are controllable.

Variant ① interfaces the AC grid with a folding (rectifier) stage with boost functionality that draws an appropriately shaped current from the grid to generate a regulated DC link voltage, which is then processed by a unregulated isolated DC-DC converter stage, e. g., by a half-cycle discontinuousconduction-mode (HC-DCM) series-resonant converter (SRC) [8], [9]. The isolation stage is positioned after the main controlling stage. Hence, the concept can be referred to as an isolated back end (IBE) system. Alternatively, the isolation stage can be controllable as well (variant ②), thereby facilitating a directly regulated output voltage, however, at the price of increased system complexity. Fig. 2(a) shows a realization example of such an IBE system.

Variant ③ is a fully integrated isolated AC-DC dual-active bridge converter (cf., e. g., [10]). Whereas such single-stage power conversion potentially achieves low losses, the complexity is high, especially considering a multi-cell arrangement.

Finally, variant ④ features an inverted sequence of the functional blocks compared to variant ① : a folding and iso-

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lation stage is directly connected to the MV AC grid, but the current shaping and the voltage regulation are performed by a controlled |AC|-DC conversion stage on the LV side. Thus, this arrangement is referred to as an *isolated front end* (IFE) system. Fig. 2(b) shows a realization example of such an IFE system.

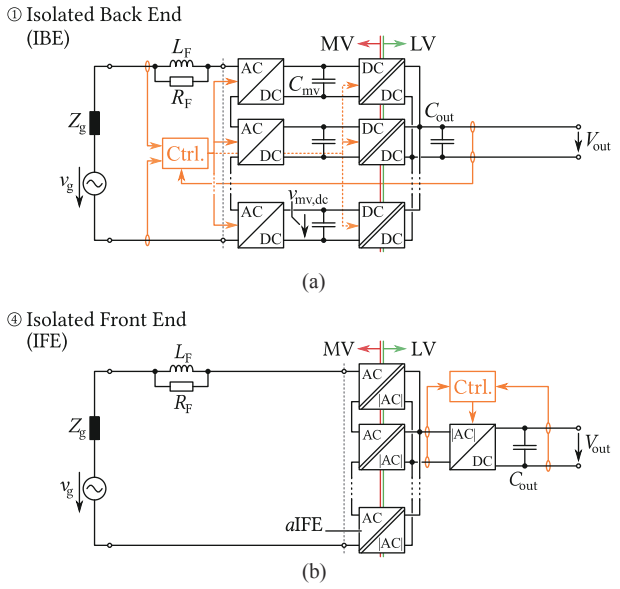

Fig. 2. Realization examples (a) of an IBE AC-DC SST, and (b) of an IFE AC-DC SST, both in multi-cell ISOP configuration.

B. Isolated Back End Multi-Cell SSTs

Fig. 2(a) shows a typical realization example of a multicell IBE SST, whereby an input-series output-parallel (ISOP) arrangement of converter cells is employed in order to handle the high voltage at the MV AC side and the high currents at the LV DC side. Such an IBE SST using an ISOP configuration has been first patented in 1996 [11], and since then been employed in various applications ranging from a 1.2 MVA SST for a locomotive achieving an AC-DC efficiency of 96% [3] to a 25 kW MVAC-LVDC power supply for datacenters with a peak AC-DC efficiency of 96.5% [1].

C. Isolated Front End Multi-Cell SSTs

In contrast, even though the IFE approach has first been proposed in 1985 for a traction application [12], it has so far not been given much attention in the engineering community. There are only recent publications discussing IFE-based multicell converter concepts with hard-switched isolation stages (i. e., non-resonant isolation stages), considering cascaded converter cells [13] and/or multi-winding transformers [14]. On the other hand, the application of an isolated HC-DCM SRC in AC-AC configuration, which allows for soft-switching operation of the power semiconductors, dates back to 1969 [8]. An ISOP configuration of such AC-AC conversion cells to realize a low-complexity AC-AC SST has been patented recently by GE [15]. The combination of these two ideas, i. e., the IFE approach and the AC-AC (or, specifically, AC-|AC|) operation of the soft-switched HC-DCM SRC converter has finally been proposed in 2013 by Han et al. [16], [17] to realize a multicell AC-DC SST, thereby demonstrating the feasibility of an IFE-based multicell SST in ISOP configuration. However, the corresponding IGBT-based small-scale (2 kVA) prototype achieved only a comparably low efficiency of 83.6%. Fig. 2(b) shows a typical realization of a multi-cell IFE SST. It should be noted that the entire control is handled on the LV side, which is in stark contrast to the IBE SST, whose control is hence more complex [7].

D. Scope of the Paper

In the scope of a research program funded by the Swiss government [18], an all-SiC realization of a 25 kW IFE SST (6.6 kV AC to 400 V DC)—the Swiss SST (S^3T)—is investigated, whereby a slightly simplified topology (no individual filter elements on the cells' AC sides as in [16], [17]) is considered [19]. TABLE I gives detailed specifications of the system. Continuing the research on IFE-based SST systems described in [7] and in [20], this paper first briefly describes the IFE concept in Section II. Then, Section III discusses the design and testing of one of the S^3T's five converter cells realized with latest silicon carbide (SiC) power semiconductors. Based on the measurement results, the IFE SST is finally evaluated against an IBE SST with same rated power [1]. Therefore, this paper contributes first a condensed overview on the IFE concept and its comparative evaluation against the well-known IBE approach. Second, the experimental part demonstrates that IFE-based AC-DC SST systems can achieve similar peformance as their counterparts employing the IBE approach. Finally, Section IV concludes the paper and gives an outlook on future research.

II. IFE Operation Principle

As indicated in Fig. 2(b), the S^3T features an ISOP configuration of converter cells, i. e., autonomous AC-|AC| isolation (front end) stages (*a*IFE), and a |AC|-DC boost converter stage. This boost converter stage can also be realized using several paralleled converters, e. g., with one boost converter per *a*IFE cell, as is considered in the following. Fig. 3 shows the detailed topology of one such converter cell consisting of an AC-|AC| *a*IFE and a |AC|-DC boost stage. Fig. 4 shows the corresponding key waveforms. The operating principle of the IFE is briefly explained in the following based on these figures; for a more detailed description please refer to [7].

The *a*IFE stage is realized as an SRC operated in HC-DCM, which has the property of tightly coupling its terminal voltages in open-loop operation (cf. [8], [9], [21] for details). On its MV side, the *a*IFE cell features a half-bridge with bidirectional switches to enable an AC input voltage, i. e., direct connection to the AC grid, by combining the folding of the grid voltage and the high-frequency switching for the

SRC operation. The second, capacitive AC-side leg consists of two (small) resonant capacitors, C_{r1} and C_{r2}. Hence, the envelope of the switched transformer voltage, v_T, is proportional to the grid voltage, and a scaled and rectified version of the grid voltage, v_{lv}, is obtained after rectification on the secondary side (active rectification is employed in order to reduce conduction losses). Accordingly, the *a*IFE is essentially acting as an isolated AC-|AC| converter.

The magnetizing current of the transformer, i_M, can be utilized for zero-voltage switching (ZVS) in order to reduce the switching losses and improve the EMI signature. However, since the switched voltage is varying over the grid period, the current available for ZVS varies, and so does the effective output capacitance of the MOSFETs. As comprehensively discussed in [20], it is nevertheless possible to realize ZVS during most of the grid period by properly designing the magnetizing inductance and the interlock time of the bridges; if a variable interlock time is employed, ZVS can be realized for the entire grid period (cf. also Section III and Fig. 5).

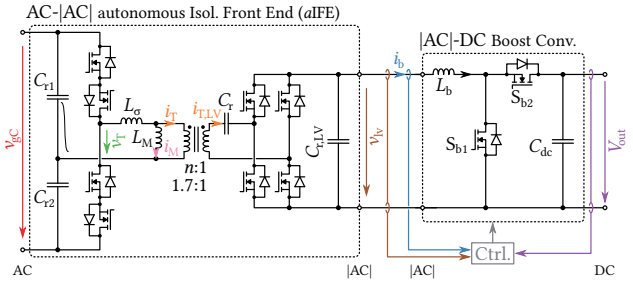

Fig. 3. Circuit schematic of one IFE converter cell. Note that C_{r1}, C_{r2} and $C_{r,LV}$ are resonant capacitors, not constant-voltage DC link capacitors. Fig. 4 shows corresponding waveforms.

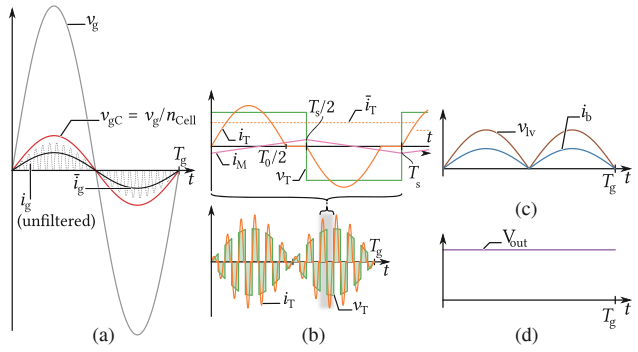

Fig. 4. Qualitative key waveforms of the IFE cell depicted in Fig. 3. (a) Cell AC input voltage v_{gC}, which is a fraction of the grid voltage due to the input-series connection of five cells; (b) HF transformer waveforms; (c) boost converter |AC|-side waveforms; (d) DC output voltage.

The input current, i_b, of the non-isolated |AC|-DC boost converter connected to the *a*IFE stage's LV |AC| terminals can be controlled such as to be in phase with v_{lv} and of appropriate magnitude to maintain the output DC voltage at a given value. Note again that thereby the entire control, including measurements, can be realized solely on the LV side of the converter. Since the *a*IFE only contains switching frequency energy storage elements, the power flow impressed by the |AC|-DC converter is directly translated to the grid. The local average value of the resonant current pulses, $\bar{i}_T$, is proportional to the boost inductor current, i_b (and hence also to the grid current, i_g), which can be assumed to be constant during a switching period. Neglecting the minor reactive power consumption of the capacitive leg, this results in unity power factor operation.

III. Prototype and Experimental Results

Based on these considerations and the specifications given in TABLE I, a prototype of a single converter cell of the S^{3}T IFE SST has been designed, constructed and tested.

A. Key Component Stresses

The stresses of the main components can be calculated analytically, which provides a basis for the system design [7].

TABLE I
Specifications of the S^{3}T and of the Converter Cell Prototype

Nom. powr, P	25 kW	Output volt., V_{out}	400 V
MV AC volt., V_N	6.6 kV	Number of cells, n_{Cell}	5
Cell power, P_{cell}	5 kW	Cell AC volt. (ampl.)	1.08 kV
SRC res. freq., f_0	52 kHz	SRC sw. freq., f_s	50 kHz
Turns ratio, n	1.7	Boost sw. freq., $f_{s,b}$	75 kHz

In a cascaded cells system, the number of required cells follows from the peak phase voltage, $\sqrt{2}V_{ph} = \sqrt{2/3}V_N$, the semiconductor blocking voltage capability, $V_{b,MV}$, and its utilization, u, as

$$n_{cell} = \frac{\sqrt{2}V_{ph}}{uV_{b,MV}}. \quad (1)$$

With $n_{cell} = 5$, the considered 1700 V SiC MOSFETs are utilized to about 65%, which is feasible regarding reliability [22].

1) Transformer: Assuming unity power factor operation, the instantaneous power of the single-phase system at the SST's AC side is

$$p_g(t) = 2P\sin(2\pi f_g t)^2. \quad (2)$$

Hence, the transformer RMS current of the IFE converter cell can be derived starting with the relation

$$\bar{i}_T(t)\cdot\bar{v}_T(t) \stackrel{!}{=} \frac{\bar{p}_g(t)}{n_{cell}}, \quad (3)$$

where $\bar{x}$ denotes a local average value over half a switching cycle of the SRC. In the case of a half-bridge configuration (factor 1/2),

$$\overline{v}_{\mathrm{T}}(t) = \frac{\sqrt{2}}{2n_{\mathrm{cell}}} V_{\mathrm{ph}} \sin(2\pi f_{\mathrm{g}} t) \tag{4}$$

holds, and thus the local average value of the MV side transformer current in a single cell becomes

$$\overline{i}_{\mathrm{T}}(t) = \frac{2\sqrt{2}P}{V_{\mathrm{ph}}} \sin(2\pi f_{\mathrm{g}} t). \tag{5}$$

Assuming piecewise sinusoidal transformer current pulses, the relation between local average and local RMS values is given by (cf. [9])

$$\tilde{i}_{\mathrm{T}}(t) = \frac{\pi}{2\sqrt{2}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}} \cdot \overline{i}_{\mathrm{T}}(t), \tag{6}$$

where f_0 and f_{s} are the resonant and the switching frequency of the SRC stage, respectively. The transformer RMS current over a grid period follows then as

$$\tilde{I}_{\mathrm{T}} = \sqrt{2f_{\mathrm{g}} \int_0^{\frac{1}{2f_{\mathrm{g}}}} \tilde{i}_{\mathrm{T}}(t)^2 dt} = \frac{\sqrt{2}}{2} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}. \tag{7}$$

Core loss densities can be estimated using the Steinmetz equation, $p_c = k f^{\alpha} \hat{B}^{\beta}$, where $\beta \approx 2...2.5$ for typical core materials suitable for MF transformers. In an IFE system, $\hat{B}$ varies with the grid voltage, i. e., $\hat{B}(t) = B_{\max} \sin(2\pi f_{\mathrm{g}} t)$, where $B_{\max}$ denotes the allowable peak flux density. Therefore, the core loss density can be found by averaging over a grid period as

$$p_{\mathrm{c}} = \frac{2}{T_{\mathrm{g}}} \int_0^{T_{\mathrm{g}}/2} k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta} \sin(2\pi f_{\mathrm{g}} t)^{\beta} dt. \tag{8}$$

For $\beta = 2$, this integral can be solved analytically, resulting in $p_{\mathrm{c}} = 1/2 \cdot k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta}$, i. e., the core loss density is lower than that of a transformer that would be operated with a constant voltage magnitude and the same $B_{\max}$.

2) aIFE Power Semiconductors: The RMS currents of the power semiconductors in the SRC bridges follow directly from the transformer current, and are given as

$$\tilde{I}_{\mathrm{SRC,MV}} = \frac{\pi P}{2V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}} \tag{9}$$

and

$$\tilde{I}_{\mathrm{SRC,LV}} = n \cdot \tilde{I}_{\mathrm{SRC,MV}}. \tag{10}$$

If an appropriate magnetizing inductance and interlock time, t_{il}, are selected, ZVS can be guaranteed over a certain range of the grid period as is shown in Fig. 5(a). Note that residual switching losses from partial ZVS in the vicinity of the grid voltage zero cross are typically neglible, if the maximum switched voltage is low. Full-range ZVS, e. g., in order to reduce EMI, would require a large magnetizing current and/or a long interlock time, which both would increase conduction losses, if a constant interlock time is used (Fig. 5(b)). Alternatively, a variable interlock time can be employed to achieve full-range ZVS without the mentioned drawbacks. Please refer to [20] for an in-depth discussion and theoretical analysis of ZVS in IFE converter cells.

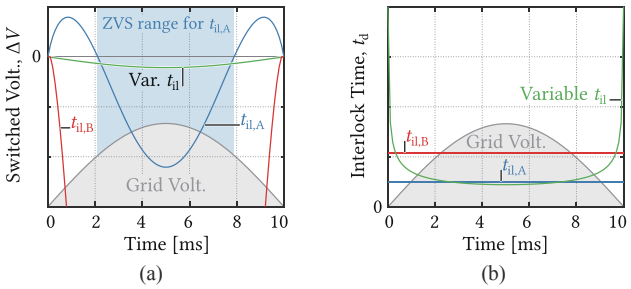

Fig. 5. *a*IFE ZVS (qualitative): (a) shows the switched voltage over half a grid period for two different constant interlock times, $t_{\mathrm{il,A}}$ and $t_{\mathrm{il,B}}$, as well as for a variable interlock time; (b) shows these interlock times over the grid period.

3) Boost Converter Power Semiconductors: The RMS currents (over one grid period) of the boost converter switches can be analytically calculated as

$$\tilde{I}_{\mathrm{Sb1}} = \frac{2\sqrt{3}Pn}{3V_{\mathrm{ph}}} \cdot \sqrt{3 - \frac{4\sqrt{2}V_{\mathrm{ph}}}{\pi n_{\mathrm{cell}} n V_{\mathrm{LV}}}} \tag{11}$$

for the shunt switch and as

$$\tilde{I}_{\mathrm{Sb2}} = \frac{4\sqrt{3}P}{3} \cdot \sqrt{\frac{\sqrt{2}n}{\pi V_{\mathrm{ph}} n_{\mathrm{cell}} V_{\mathrm{LV}}}} \tag{12}$$

for the series switch. Switching losses for hard-switching conditions can be obtained from the devices' datasheets.

4) Boost Inductor: The rms current of the boost inductor (neglecting the switching frequency ripple) is given by

$$\tilde{I}_{\mathrm{B}} = \frac{2Pn}{V_{\mathrm{ph}}} \quad \left(= \sqrt{\tilde{I}_{\mathrm{B,Shunt}}^2 + \tilde{I}_{\mathrm{B,Series}}^2} \right). \tag{13}$$

Its core losses can be estimated from the peak-to-peak current ripple, $\Delta I_{\mathrm{b\,,\,pp}}$, the number of turns, N_{b}, and the core cross section area, A_{Fe}, according to

$$\Delta B_{\mathrm{pp}} = \frac{L_{\mathrm{b}} \Delta I_{\mathrm{b,pp}}}{N_{\mathrm{b}} A_{\mathrm{Fe}}} \tag{14}$$

and

$$p_{\mathrm{c,b}} = k f_{\mathrm{s,b}}^{\alpha} \left(\frac{\Delta B_{\mathrm{pp}}}{2} \right)^{\beta}. \tag{15}$$

For typical current ripples, the resulting core losses are small compared to the winding losses.

B. Key Components of the Realized Prototype

Using the above considerations, a prototype of a converter cell with the topology given in Fig. 3 has been designed and constructed. Fig. 6 shows a photograph of the realized 5 kW prototype, which features an AC input voltage of 760 V (rms) and 1080 V (peak), and a DC output voltage of 400 V. The power density is about 1.5 kW/l (24.6 W/in^3).

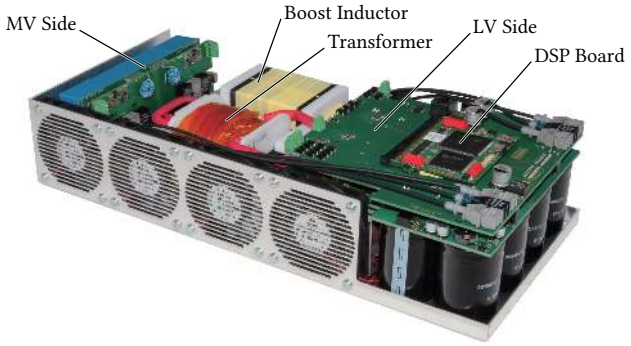

Fig. 6. Photograph of the constructed IFE cell prototype with a rated power of 5 kW The dimensions are 323 mm × 148 mm × 70 mm, corresponding to a power density of 1.5 kW/l (24.6 W/in^3). The measured peak efficiency is 97.5%, and the full efficiency curve is shown in Fig. 11.

The cell prototype employs latest SiC MOSFETS by Wolfspeed [23]: the bidirectional switches on the MV side are realized with 1700 V/45 mΩ (25 °C) devices (C2M0045170D), whereas the LV side switches (for both, active rectification in the *a*IFE and the boost stage) are realized with 900 V/13 mΩ (25 °C) devices (X3M0010090X-ES). The latter are available in a TO-247-4 package, i. e., they feature a Kelvin source that helps improving the switching behavior and reducing switching losses.

The transformer is based on an E80 core (Epcos N87 ferrite) and litz wire windings (22 turns of 900 × 0.1 mm litz wire on the MV side, 13 turns of 1400 × 0.1 mm litz wire on the LV side), with 3 mm of isolation material between the primary and secondary side windings. Note that no detailed isolation coordination such as in [2] is carried out, because the focus lies on evaluation of the IFE topology, not on the transformer design, which is covered by corresponding literature [2], [24]-[27].

In order to constrain the size of the boost inductor, a comparably high switching frequency of 75 kHz is used. The boost inductor can then be realized from three stacked E56 cores (Epcos N87 ferrite), and again using 14 turns of a litz wire winding (900 × 0.1 mm) and a 2.4 mm air gap. Please refer to TABLE II for more details on the main components of the prototype as well as their respective current and/or voltage stresses.

The control software is implemented on a custom control board that features a TMS320F28335 DSP from TI and a LFXP2-5E-T144 FPGA from Lattice. Optical fibers are used to transmit the gate signals from the control on the LV side to the gate drives of the switches on the MV side, and to transmit status signals from those gate drives back to the control board.

TABLE II
MAIN COMPONENTS AND THEIR KEY STRESSES.

MV res. cap., $C_{r1,2}$	2.7 µF, 8.7 A (rms), 565 V (peak)
Series res. cap., C_r	4.6 µF, 26.9 A (rms), 37 V (peak)
LV res. cap., $C_{r,LV}$	3 µF, 13.6 A (rms), 321 V (peak)
MV FETs	C2M0045170D (1700 V/45 mΩ)
MV *a*IFE FET cur.	11 A (rms)
LV FETs	X3M0010090X-ES (900 V/13 mΩ)
LV *a*IFE FET cur.	19 A (rms)
LV Boost low-side cur.	13.8 A (rms)
LV Boost high-side cur.	19 A (rms)
Transf. core.	E80/38/20, N87 ferrite
MV winding	22 turns, 15.5 A (rms), 900 × 0.1 mm litz
LV winding	13 turns, 26.4 A (rms), 1400 × 0.1 mm litz
Stray ind., L_σ	10 µH
Magn. ind., L_M	733 µH (0.2 mm air gap)
Boost. ind., L_b	140 µH (30% peak-peak cur. ripple)
Boost. ind. core	3 × E56/24/19 N87 ferrite
Winding	14 turns, 23 A (rms), 900 × 0.1 mm litz
Air gap	2.4 mm
LV DC cap., C_{dc}	5.45 mF, 13.1 A (rms), 400 V (DC)

C. Measurements

As no MV AC source was available, the converter cell has been tested with power flow from the DC to the AC side, i. e., a 400V DC power supply is connected to the LV DC terminals, and a resistive load is attached to the MV AC side terminals. The system is then operated in open-loop, i. e., by using a $|\sin 2\pi f_g|$-shaped reference for the PWM of the boost converter stage, and by gating the bidirecitional switches on the MV side such as to realize both, active recitification of the

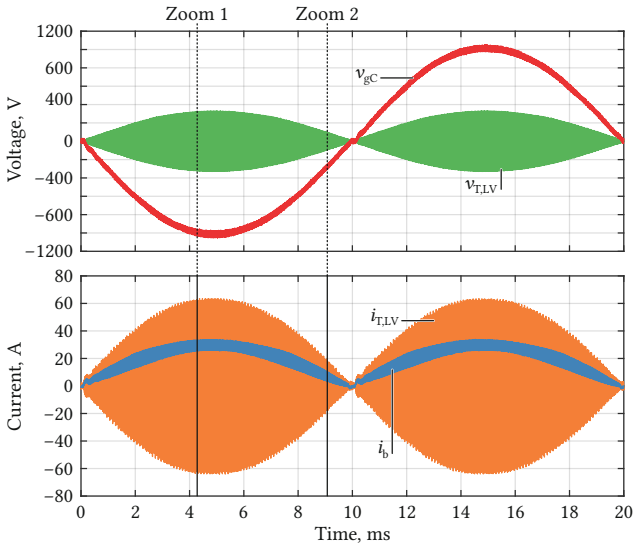

Fig. 7. Measured key waveforms at rated load in DC-AC operating mode, i. e., with power flow from the DC to the AC side. Fig. 8 shows zoomed views covering a few switching periods at the indicated locations.

HF voltage and unfolding of the resulting $|\sin 2\pi f_g|$-shaped waveform into an AC voltage at the MV terminals.

Fig. 7 shows the corresponding key waveforms over one fundamental period (50 Hz) at nominal load. The AC output voltage, v_{gC}, is sinusoidal and in phase with the boost inductor current, i_b, on the LV side, which, as discussed above, corresponds to unity power factor operation. Fig. 8 shows zoomed views of these key waveforms at two different points in time within the grid period. These measurements clearly verify the description of the IFE converter's operating principle described in Section II.

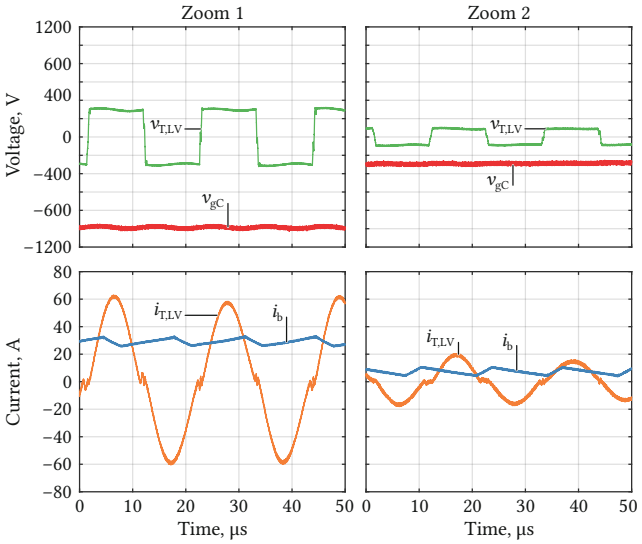

Fig. 8. Measured key waveforms at rated load in DC-AC operating mode at two different instants during the grid period as indicated in Fig. 4.

Fig. 9 shows two transitions of the transformer voltage at two different instants of the grid period, once at 50 V and once at 220 V. In both cases, an interlock time of 700ns is used—this is clearly too short to achieve ZVS in the first case, and clearly too long in the second, which confirms the theoretical considerations from [20] and the qualitative analysis in Fig. 5. Thus, the required interlock time has been measured for different switched voltages, which is an alternative to the simulation-based approach described in [20]. The results are

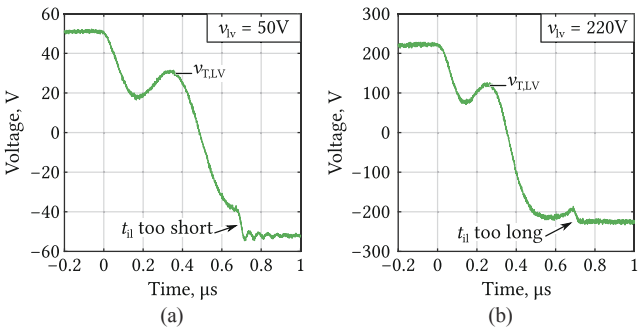

Fig. 9. Detailed view of transitions at different switched voltages of (a) 50 V and (b) 220 V. A constant interlock time of 700ns is employed, which is too short in case (a) but too long in case (b).

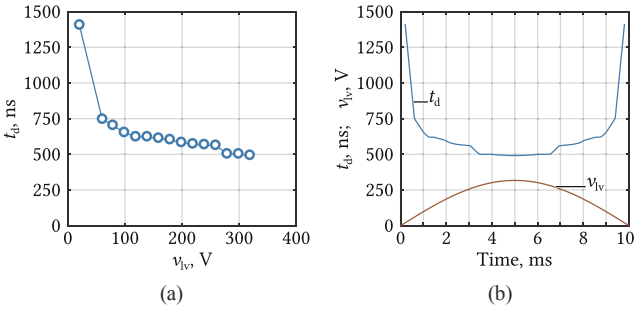

Fig. 10. (a) Required interlock time to ensure ZVS (measured); (b) required interlock time plotted versus time during one half grid period.

shown in Fig. 10(a) and match the qualitative curve shown in Fig. 5(b). The data is then stored in a lookuptable in order to adapt the interlock time of the *a*IFE bridge during the grid period as indicated in Fig. 10(b). The impact on losses is low, however, full-range ZVS may help in improving the EMI signature of the converter by limiting the appearing dv/dt during the transients.

Finally, the efficiency of the converter cell has been measured using a Yokogawa WT3000 power analyzer. The resulting dependeny of the efficiency on the supplied power for DC-AC operation with resistive loads is given in Fig. 11. The full-load efficiency is about 97%, and the peak efficiency observed between 50%...60% of rated load is 97.5%. Note that the efficiency for power flow from the AC to the DC side is expected to be similar, because active rectification is used.

Fig. 12 shows a calculated loss breakdown for nominal

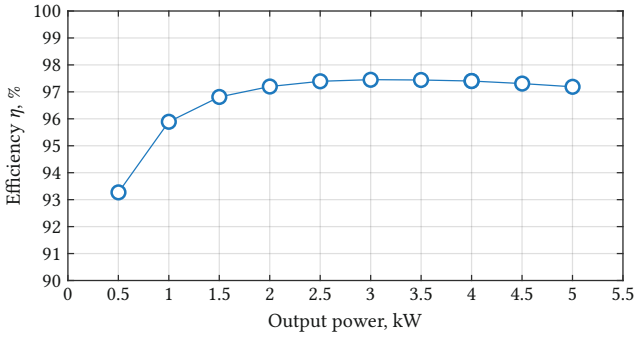

Fig. 11. Measured efficiency in DC-AC operation with V_{dc} = 400 V and a resistor load on the AC side.

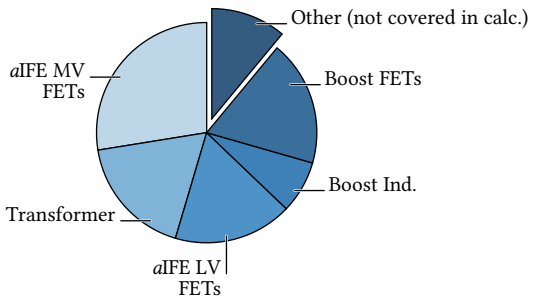

Fig. 12. Loss breakdown (calculated) at nominal power. The separated slice represents the losses not covered by the calculation, i. e., the difference between calculated and measured losses at rated power, corresponding to the calculations underestimating the losses by roughly 11%.

power transfer from the DC to the AC side. The loss share denoted as "Other" corresponds to the deviation between calculated and measured losses, and may be related to losses in the PCB traces, additional switching losses due to additional parasitic capacitance, and other effects not captured by the modeling of the main components. The efficiency could thus possibly be further increased by reducing the switching frequency of the boost converter stage, however, at the cost of lower power density. Also, since the *a*IFE MV MOSFET losses are only conduction losses, paralleling of two devices could contribute to a higher efficiency; the same is true, although to a lesser extent, for the *a*IFE LV MOSFETs.

D. Discussion

In [7], a generic theoretical comparison between equally rated IFE and IBE systems is given. The main findings are summarized in Fig. 13: considering the same specifications, an IFE system requires less cascaded converter cells than an IBE system, because the boost functionality is realized on the LV side in case of the IFE system. As a consequence, the IFE system also uses fewer individual switches and hence gate drive units. The overall transformer volume is similar. However, the relative VA rating of the power semiconductors, i. e.,

$$\mathrm{VA}_{\mathrm{rel}} \stackrel{\mathrm{def}}{=} \frac{1}{P} \cdot \sum i_{\mathrm{x,max}} v_{\mathrm{x,max}}, \tag{16}$$

is higher in case of the IFE, because of the higher peak current in the transformer resulting from the sinusoidal envelope of the transformer voltage. Similarly, considering equal cooling conditions, i. e., equal permissible loss densities, the required total semiconductor chip area is also slightly higher for the IFE system.

The considerations and the experimental results presented in this paper confirm that indeed an IFE-based SST can achieve similar performance as an IBE SST: The measured efficiency of the converter cell is significantly higher than previously reported efficiencies of IFE-based MVAC-LVDC SSTs (83.6% for a 2 kVA demonstrator [16], [17]), and similar to the efficiency published for a similarly rated IBE-based MVAC-LVDC SSTs (25 kW, 96.5% peak efficiency [1]). Considering that the complete IFE SST would contain also additional hardware for protection, measurements, etc., the overall efficiency would likely be slightly lower than the measured efficiency of the converter cell at hand, and hence similar to that of the IBE-based SST system.

The power density of converters connected to MV levels is influenced strongly by clearance and creepage distances required by corresponding standards. The isolation coordination for such systems, e. g., for the HF transformer itself, is a complex task that is similar for all MV-connected power electronic converters, i. e., not specific for IFE-based systems. Therefore, and for the sake of conciseness, these issues have not been considered here in detail. Instead, the interested reader is referred to the corresponding literature [2], [24]-[28]. Thus, the power density of the industrial IBE prototype

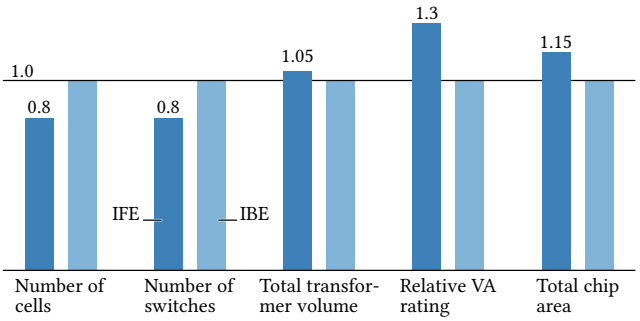

Fig. 13. Generic comparison of the realization offort of the IFE and the IBE concepts according to [7].

discussed above is only about 0.4 kW/l (6.6 W/in^3) (overall) and 0.83 kW/l (13.6 W/in^3) for one of its converter cells [1], i. e., only about half the power density achieved with the presented IFE converter cell. It is thus reasonable to expected that an inudstrialized version of the IFE SST could achieve similar power density as its IBE-based counterparts.

All in all, the IFE converter cell prototype design and the measurements show that it is possible to achieve decent efficiencies and power densities also with MVAC-LVDC SSTs based on the IFE approach.

IV. Conclusion and Outlook

This paper discusses the isolated front end (IFE) concept for realizing an MVAC-LVDC SST. First, the different options to partition the functionality requried for isolated AC-DC conversion with PFC are briefly discussed, before then the operating principle of IFE-based SSTs is explained in detail. In order to clarify the achievable performance of IFE-based SSTs, one converter cell of a 25 kW 6.6 kV AC to 400 V DC MVAC-LVDC IFE SST, denominated as Swiss SST (S^{3}T), is designed, constructed and tested. The 5 kVA converter cell prototype features a power density of 1.5 kW/l (24.6 W/in^3) and a peak efficiency of 97.5% for power flow from the DC to the AC side. This efficiency is significantly higher than previously published results for IFE-based SSTs, and comparable to reported efficiencies of IBE-based SSTs. Therefore, this paper demonstrates the competitiveness of the IFE approach for realizing MVAC-LVDC SST systems. Especially in case low complexity is desirable as, e. g., in applications where the focus is on weight and space reduction, not on controllability, i. e., in applications where the SST essentially acts as a MVAC-LVDC power supply, the IFE concept may be an interesting alternative approach worth considering. Such applications could be, among others, auxiliary power supplies in future trains to supply air conditioning units, lighting, etc. of individual coaches, or rack-level power supplies in future datacenters.

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