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Analysis and Compact Modeling of a Vertical Grounded-Base NPN Bipolar Transistor used as ESD Protection in a Smart Power Technology

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Analysis and Compact Modeling of a Vertical Grounded-Base n-p-n Bipolar Transistor Used as ESD Protection in a Smart Power Technology

Géraldine Bertrand, Christelle Delage, Marise Bafleur, Nicolas Nolhier, Jean-Marie Dorkel, Quang Nguyen, Nicolas Mauran, David Trémouilles, and Philippe Perdu

***Abstract*—A thorough analysis of the physical mechanisms involved in a vertical grounded-base n-p-n bipolar transistor (VGBNPN) under electrostatic discharge (ESD) stress is first carried out by using two–dimensional (2-D) device simulation, transmission line pulse measurement (TLP) and photoemission experiments. This analysis is used to account for the unexpected low value of the VGBNPN snapback holding voltage under TLP stress. A compact model based on a new avalanche formulation resulting from the exact resolution of the ionization integral is therefore proposed.**

***Index Terms*—Bipolar, compact modeling, ESD, smart power, two-dimensional (2-D) simulation.**

I. Introduction

THE NUMBER of circuit design iterations due to electrostatic discharge (ESD) failures increases with the complexity of VLSI technologies and their shrinking. To move toward "a first pass success" design, a predictive design methodology taking into account the ESD problem at an early stage of a project is required. The availability of an ESD protection library including both layouts and electrical models is part of the solution. Most of the publications related to ESD modeling concern the grounded-gate NMOS ESD protection structure, which involves the parasitic lateral bipolar transistor in CMOS technologies [1], [2]. However, very few are dedicated to smart power technologies and their vertical grounded-base bipolar ESD protection structure [3], [4]. In this paper, we propose a thorough analysis of the physical mechanisms involved under ESD stress in a vertical grounded-base bipolar ESD protection structure of a smart power technology. To get a deeper insight into high current mechanisms, we use 2-D device simulation as well as TLP measurement, failure analysis, and photoemission experiments. The strong snapback behavior observed under TLP measurement (25 V instead of 35 V in dc) can be theoretically accounted for and validated. The obtained results support the development of a new avalanche generation model and provide a physics-based compact model for the vertical grounded-base bipolar transistor as an ESD protection structure.

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II. The Vertical Grounded-Base n-p-n (VGBNPN)

The considered technology is a 1.8-μm 65-V smart power technology. It combines a p-well CMOS technology with a variety of optimized vertical and lateral bipolar transistors as well as both vertical and lateral DMOS power devices. As a vertical n-p-n bipolar device is available, it serves as ESD protection in grounded-base configuration. It is called vertical grounded-base n-p-n (VGBNPN). Fig. 1 shows the electrical schematic and cross section of the VGBNPN used as an ESD protection structure in this technology. Two modifications are introduced in this device with respect to the standard one: use of a single base contact and of an emitter ballast resistance by increasing the spacing between emitter edge and contact. When a negative ESD stress is applied to the collector of the VGBNPN, it behaves as a forward-biased diode. In this mode, the ESD robustness is high and there are no layout difficulties since the electric field is low. In the case of positive ESD stress, the VGBNPN is triggered when the voltage on the collector electrode reaches the base–collector breakdown voltage. The resulting avalanche current flowing through the internal base resistance then forward-biases the base–emitter junction and triggers the n-p-n bipolar transistor on. Once the n-p-n turns on, the avalanche and bipolar effects combine resulting in the decrease of collector voltage down to the snapback holding voltage. This structure provides very good ESD robustness ranging from 3.5 kV (26 V/μm) to more than 10 kV (75 V/μm) under positive human body model (HBM) stress [5] and from 700 V (5 V/μm) to 1300 V (9.5 V/μm) under positive machine model (MM) stress [6]. This good performance is achieved according to layout of the n-p-n transistor and by combining it with other circuit elements (Zener diode, resistor , etc.) and motivated us to adding this protection structure to the ESD protection library of the technology.

III. Analysis of Physical Mechanisms Involved Under an ESD Stress

To provide a compact model for the VGBNPN, a comprehensive knowledge of the electrical mechanisms involved is required. In addition to HBM and MM ESD testing, transmission line pulse (TLP) measurement is performed to get additional information on the dynamic electrical behavior of the structure such as: trigger voltage and current, snapback voltage, and

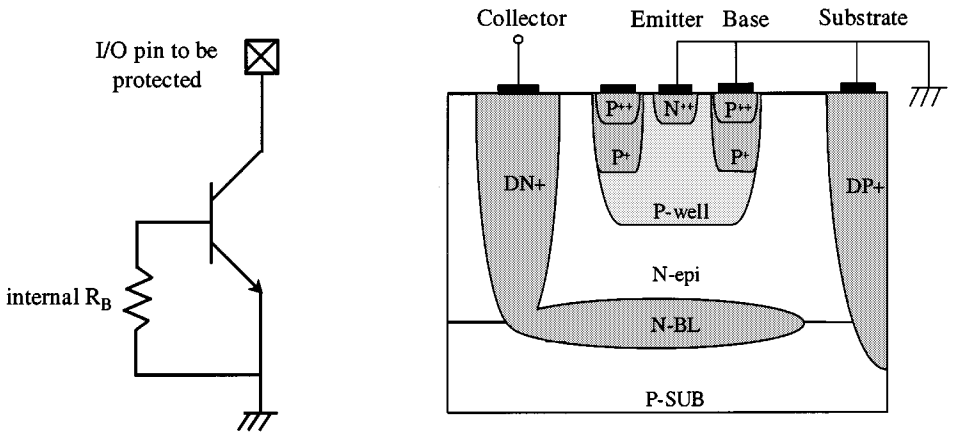


Fig. 1. Electrical schematic and cross section of the VGBNPN.

on-state resistance. This method uses a transmission line to generate current pulses comparable to the HBM discharge in terms of rise time (2–10 ns), pulse duration (∼120 ns), and amplitude (several amperes).

Fig. 2 first shows that the snapback trigger voltage (V_{t1}) occurs at a much higher voltage (67 V instead of 55 V) than BV_{CBo}, the collector–base breakdown voltage. The reasons for this high value will be explained later. Also, the most striking feature of this measurement is that the resulting snapback holding voltage (V_h) is much lower than the measured BV_{CEo}, the common emitter breakdown voltage: it is 25 V versus 32 V for BV_{CEo}.

It was first checked on several structures that this strong snapback was not related to a measurement artifact. Two-dimensional device simulations were performed with ATLAS [7] and DESSIS [8] to try to reproduce this unexpected behavior. Despite careful simulator calibration, it was not possible to reach such a strong snapback although the BV_{CEo} voltage value is perfectly retrieved in dc simulation. This discrepancy could be attributed to the inaccuracy of the avalanche model. Indeed, using hydrodynamic models, that are more appropriate to this high-energy phenomenon, a significant improvement in the measurement/simulation agreement was achieved. Nevertheless, a thorough analysis of the simulated results provides an understanding of the most likely reasons for the strong snapback behavior.

The analysis of the electric field at the base–collector junction right below the emitter (Fig. 3) shows the so-called Kirk effect [9] occurring when the current density exceeds the critical value $J_o = qv_l N_D$, N_D standing for collector doping and v_l for carrier saturation velocity. As shown in Fig. 3, this critical value is reached for $t = 0.7$ ns just before the VGBNPN snaps back at $t = 0.8$ ns.

Analysis of the corresponding impact ionization rate within the VGBNPN during a 2-kV HBM stress [Fig. 4(a)] confirms the Kirk effect causing the base widening. Indeed, although avalanche generation is initiated at the cylindrical base–collector junction facing the collector contact [Fig. 4(b)], its maximum rate rapidly moves to the N/N^+-buried layer boundary [Fig. 4(c) and (d)]. These simulation results show that the dominant avalanche mode which generates base current for the npn bipolar transistor is the avalanche injection [10] at the

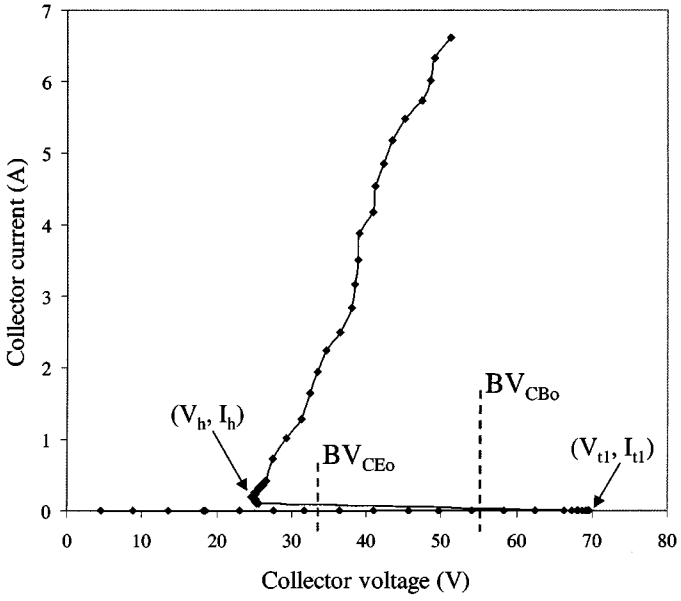


Fig. 2. TLP and dc measurements for the VGBNPN. BV_{CBo} and BV_{CEo} are measured at 10 μA.

N/N^+-buried layer boundary where the maximum base width is reached.

To get a deeper understanding of the involved phenomena, we have plotted the net doping, the free carrier density, and the electric field in the structure, both under low- and high-level injection [Fig. 5(a) and (b)]. Under low-level injection [Fig. 5(a)], the space charge of the reversed biased base–collector junction spreads out around the metallurgical junction, mainly into the collector side. The effective doping concentration, N_{eff}, determines the junction breakdown voltage value BV_{CBO} as well as the common emitter breakdown BV_{CE0} following the expression:

$$N_{\text{eff}} = \frac{N_A \cdot N_D}{N_A + N_D} \approx N_D \tag{1}$$

where N_A and N_D are the base and collector doping concentrations, respectively.

With the increase of the ESD current, the structure enters into high-injection conditions and Kirk effect occurs. Maximum electric field moves from the metallurgical junction [Fig. 5(a)]

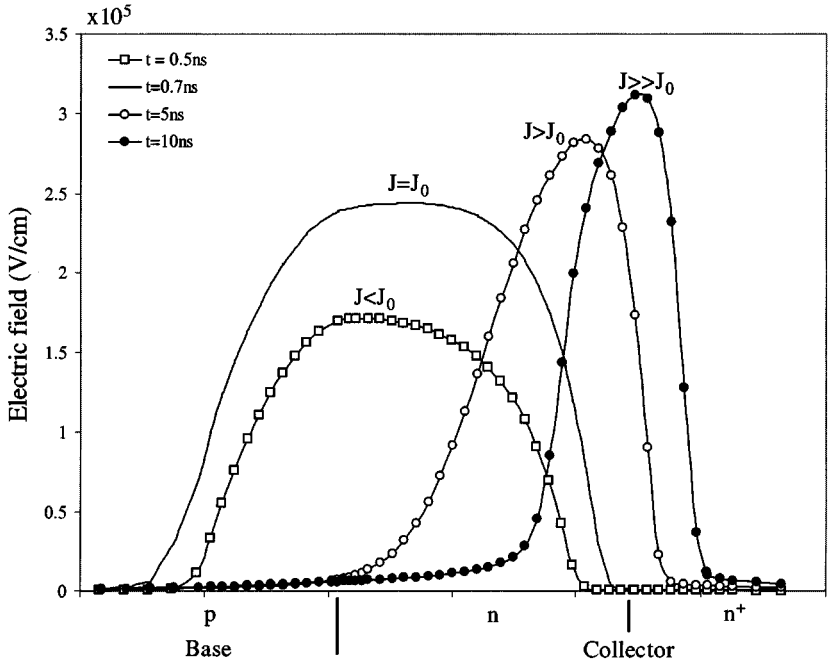


Fig. 3. Simulated electric field profiles of the VGBNPN under the emitter for various current densities under a 2-kV HBM stress.

to the N/N^+-buried layer boundary. As a result, the electric field is now sustained by a space charge mainly built up by free carriers [Fig. 5(b)]. The breakdown voltage of this equivalent "planar junction" is determined by an effective "doping" concentration $N_{\text{eff}} > N_D$ in the range of the local electron density [Fig. 5(b)]. As a consequence, the corresponding snapback holding voltage can be much less than the BV_{CEo} voltage value which is related to an avalanche current generated in the intrinsic base by the base–collector junction with a reference doping of N_D. At the N/N^+-buried layer boundary [Fig. 4(d)], the electric field becomes maximum and the impact ionization rate directly depends on the collector current that can be very large because of the resulting regenerative effect. This *electrically initiated mechanism* is the one involved in the second breakdown of epitaxial bipolar power devices [11], *failure resulting from the induced local heating*. However, the relatively short duration of the ESD stress ($\sim$150 ns) does not result in a significant heating and the previously described effect is very beneficial to the device since a lower snapback holding voltage leads to a lower power dissipation.

This theoretical explanation was validated by photoemission (EMMI) experiments. Both frontside and backside EMMI experiments were carried out using a C4880-10 HAMAMATSU digital CCD camera. To perform backside emission microscopy, we prepared the sample by thinning the die down to 200 μm using a CNC micromachining tool, the Chip Unzip from Hypervision [12].

Figs. 6 and 7 show a comparison between simulation and photoemission views. At the onset of snapback, the cylindrical base–collector junction goes into avalanche. The photoemission is localized at the corners of the base–collector junction [Fig. 6(b)] and R_{BC} indicated on the simulated cross section [Fig. 6(a)] is in the path of the avalanche current. This resistance, responsible for the high value of the VGBNPN trigger voltage, is extracted from TLP measurement and has a mean value around 2 kΩ. As soon as the bipolar transistor triggers on and current increases, the locus of the impact ionization moves from the spherical base-collector junction to underneath the right edge of the emitter [Fig. 7(a) and (b)]. It should be pointed out that a backside EMMI experiment was required to clearly see this photoemission which was masked by the emitter metallization in the front side experiment.

Failure analysis carried out using the focus ion beam (FIB) technique confirmed that failure actually occurs deep below the emitter, at a location where the 2-D simulation showed both high current density and high electric field [13].

IV. Compact Modeling of the VGBNPN

The vertical n-p-n transistor chosen as an ESD protection device is part of the library of the considered smart power technology, but its classical Gummel–Poon model does not include the high current regime of the ESD device. Therefore, our modeling approach consists of creating a macromodel using external circuit elements added to the standard model. The advantages of this strategy are its easy implementation within a SPICE-like simulator and the reduced characterization of the device, since only high-current avalanche-related parameters are needed. The electrical schematic of the VGBNPN macromodel is given in Fig. 8. The added external elements are an avalanche current source I_{av}, an extrinsic base resistance R_{BC}, an intrinsic base resistance R_{BASE} that is current modulated and the nonlinear capacitances of the bipolar device.

Prior to detailing the VGBNPN ESD model, let us briefly recall its trigger mechanism: when a positive discharge occurs on the collector, the hole current resulting from the avalanche breakdown of the base–collector junction flows through the internal base resistance and forward-biases the base–emitter junction. Then the n-p-n transistor turns on.

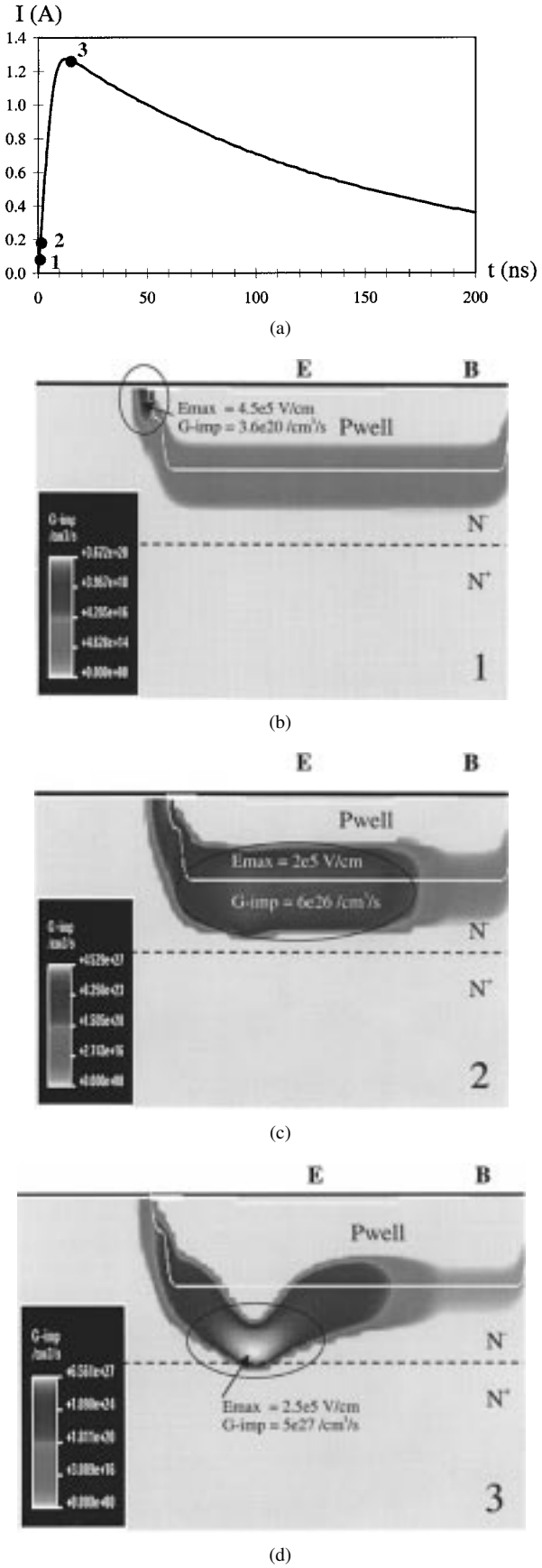


Fig. 4. Simulated cross sections of the VGBNPN showing impact generation rate at different times under a 2-kV HBM stress: (a) HBM waveform; (b) $t = 0.7$ ns at the onset of snapback; (c) $t = 1$ ns right after the snapback; and (d) $t = 11$ ns at peak current. Regions of highest impact generation are circled.

Avalanche current is modeled by an arbitrary controlled current source between base and collector electrodes, which expression depends on the collector current as follows [4]:

$$I_{\text{av}} = k_0 \cdot (M-1) \cdot I_C \tag{2}$$

where M is the avalanche multiplication coefficient and k_0 a fitting parameter.

The expression generally used for M is the Miller empirical formula [14], which has the drawback of inducing convergence problems when the voltage reaches the avalanche breakdown voltage. To overcome this drawback, two solutions are concurrently used. On the one hand, the avalanche current is expressed as a function of the total current I_{ESD} entering the collector electrode

$$I_{av} = \frac{k_0 \cdot (M-1)}{1 + k_0 \cdot (M-1)} \cdot I_{\text{ESD}}. \tag{3}$$

On the other hand, the chosen expression for M has continuous values over the whole range of voltages that eases the simulation convergence. Indeed, it has been demonstrated above that in the case of the VGBNPN, the avalanche current is mostly generated by a "planar junction" located at the N/N^+-buried layer boundary. This is a relatively simple theoretical case and we have chosen to extract M from the exact resolution of the ionization integral [15], [16] which can be expressed by means of the following equation:

$$1 - \frac{1}{M} = \frac{A_n}{A_p - A_n} \cdot \left[\exp\left\{ 2 \cdot (A_p - A_n) \cdot \left(\frac{q}{\varepsilon}\right)^3 \cdot N_{\text{eff}}^3 \cdot V^4 \right\} - 1 \right] \tag{4}$$

where A_n and A_p are constants involved in the expression of the ionization coefficients for electrons and holes [17], respectively, N_{eff} is the effective doping concentration of the collector, and V is the collector–base voltage.

N_{eff} is an effective doping concentration built up by the high density of free carriers. It is no longer dependent on the collector doping but on the collector current as soon as its density reaches the critical current density $J_o = qv_l N_D$. To avoid convergence problems, instead of using a current-dependent value, we choose to use a fixed value of N_{eff} that allows fitting the real BV_{CBo} breakdown voltage value of the structure [16], which is one of the critical parameters for ESD protection design. As long as the current is homogeneously distributed in the structure, under high-level injection, this simplification is somewhat justified since the local free carrier density varies slowly. Indeed, EMMI experiments showed that the emitter current spreads along the emitter finger with the increase of ESD current resulting in an almost constant local current density. Nevertheless, the introduction of another fitting coefficient k_0 is required to adjust the holding voltage V_h.

This avalanche current flows through the extrinsic base resistance, R_{BC}. In the model, this resistor is responsible for the V_{t1} high trigger voltage of the structure, which is critical for the ESD protection design margins definition. It is made current-dependent to take it into account only before the turn-on of

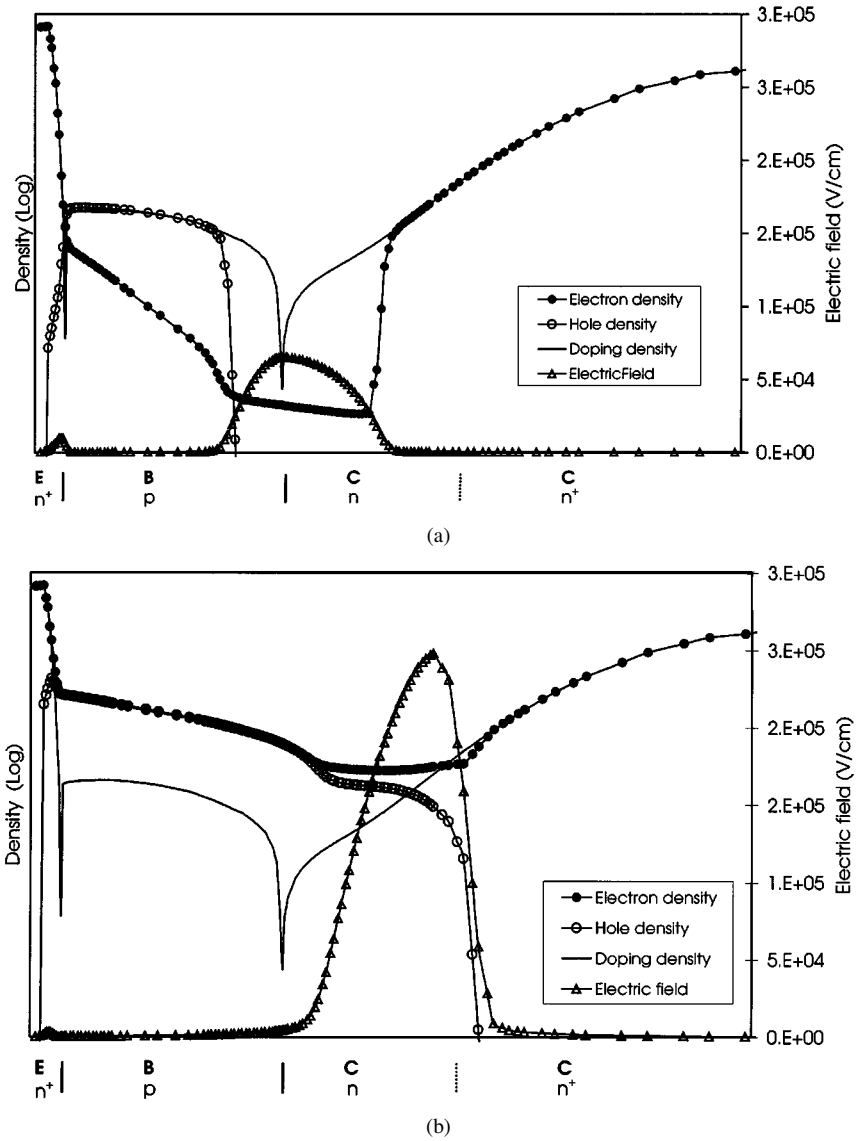


Fig. 5. Simulated data for net doping, free carrier density, and electric field in the VGBNPN under (a) low-level and (b) high-level injection.

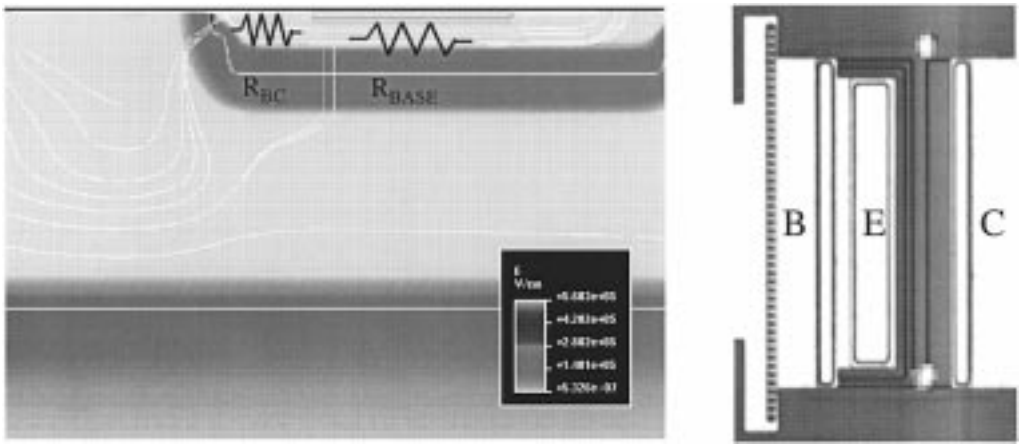
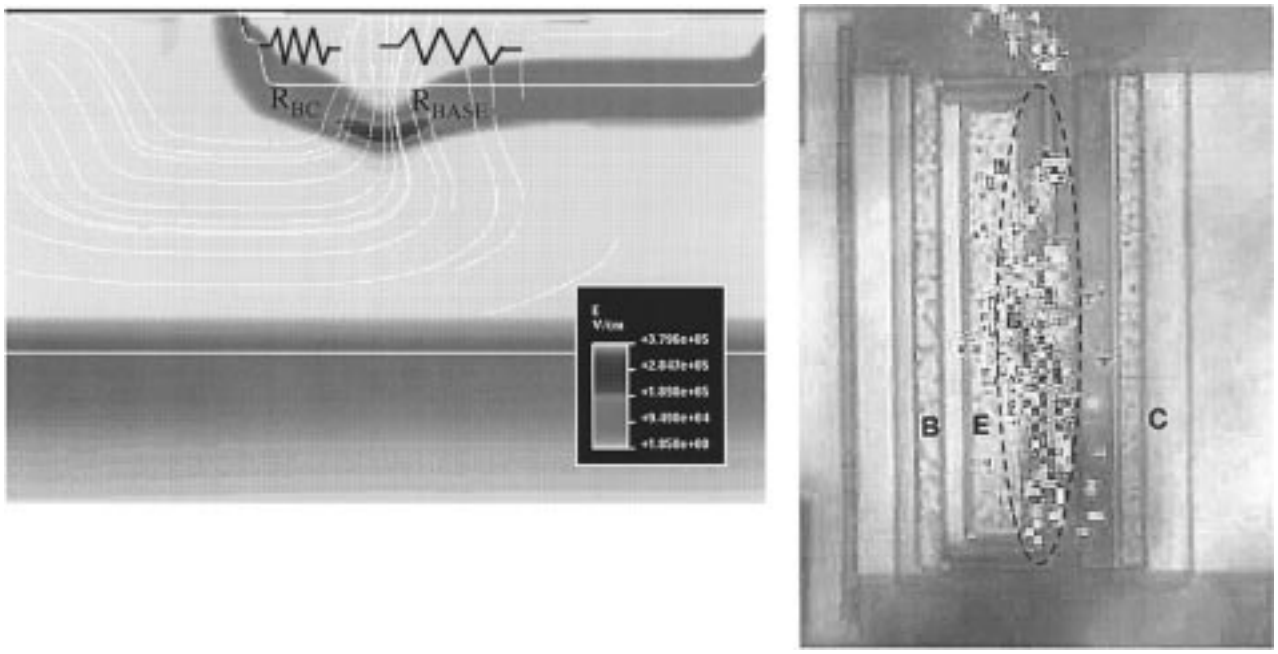


Fig. 6. (a) Electric field and current flowlines simulated results. (b) Frontside photoemission view of the VGBNPN under TLP testing at the onset of snapback.

the n-p-n bipolar transistor. No basic SPICE circuit element can model such variable resistance. Therefore, a current controlled voltage source has to be used.

Similarly, the avalanche current also flows through the intrinsic base resistance, R_{BASE}. It is then necessary to remove it from the n-p-n intrinsic model and add it externally between



(a) (b)

Fig. 7. (a) Electric field and current flowlines simulated results. (b) Backside photoemission view of the VGBNPN under TLP testing at high current density. Strong emission region is circled.

the base and emitter electrodes. To take into account the conductivity modulation effects, the base resistance is made variable using the formulation given by the standard Gummel–Poon model. Three parameters are required for its model:

- $R_{BASE\,\max}$, the maximum value, is calculated thanks to the pinched base sheet resistance value and the emitter size;
- $R_{BASE\,\min}$, the minimum value, is extracted from the SPICE parameters of the standard n-p-n;
- $R_{BASEtrig}$, the base resistance value at the trigger point (V_{t1}, I_{t1}), is extracted from TLP measurement ($R_{BASEtrig} = V_{BEtrig}/I_{t1}$, where $V_{BEtrig} \approx 0.5$ V).

Likewise, junction capacitances are removed from the n-p-n model and implemented as shown in Fig. 8.

Moreover, using a 2-D device simulation, we checked that the heating of the device under an ESD stress could be considered as adiabatic. Indeed, the only region going through a temperature increase is confined to a 10-μm-diameter region deep below the emitter, which is actually the location of the final failure. As a consequence, no electrothermal model is implemented in the ESD compact model since the aim of modeling is to simulate functional ESD protection structures.

Using this macromodel, simulation convergence problems during ESD stress simulations are definitively solved. In addition, a very good correlation is achieved between measured and simulated data for both dc (low current) and dynamic modes (Fig. 9).

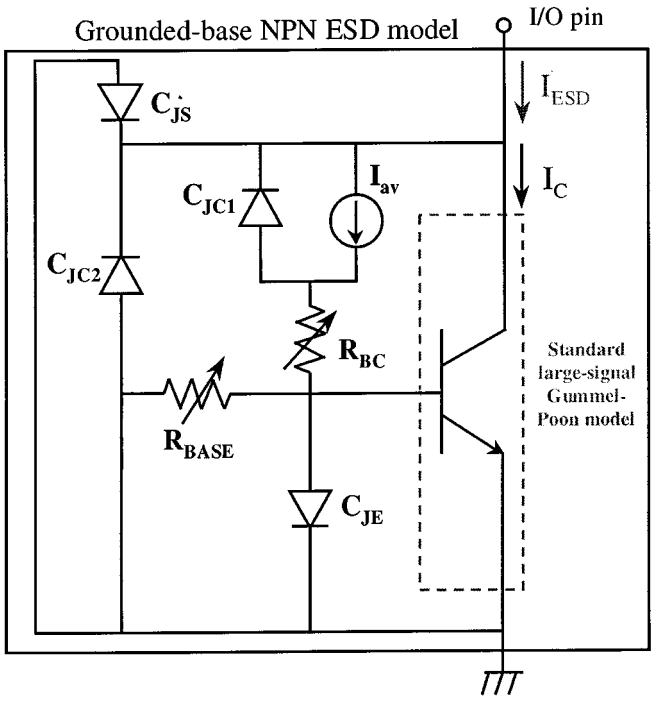


Fig. 8. Electrical schematic of the VGBNPN macromodel.

V. Modeling Validation

The aim of the ESD compact modeling is to provide circuit designers with a means of verifying their ESD protection strategy while assessing the impact of the ESD protection structures on the circuit performance. By way of example, we use the VGBNPN compact model to optimize the design of a two-stage ESD protection circuit (Fig. 10) for a CMOS inverter input where the VGBNPN is the primary device and a Zener diode, D_z, the secondary one. In this two-stage ESD protection, the secondary stage triggers on first and allows clamping of the voltage at the protected circuit input. When the ESD current increases, it induces a voltage drop over the series resistance R, which in turn triggers on the primary stage. Here the VGBNPN

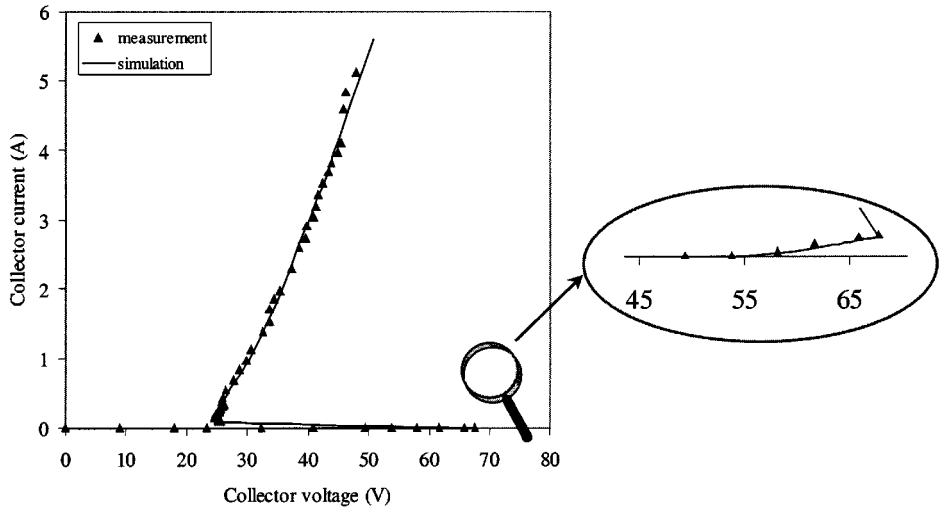


Fig. 9. Comparison between TLP measurement and TLP SPICE simulation. Enlarged view shows the good agreement at low current level.

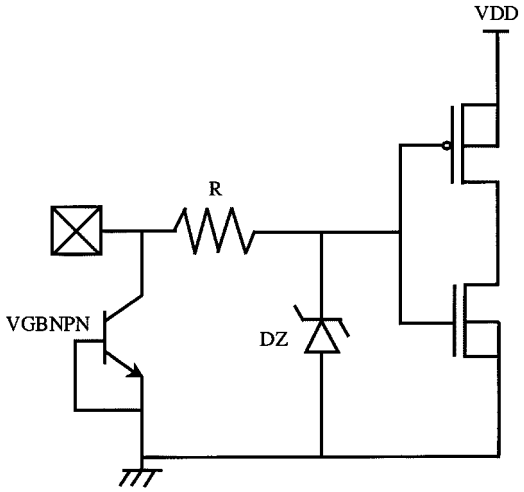


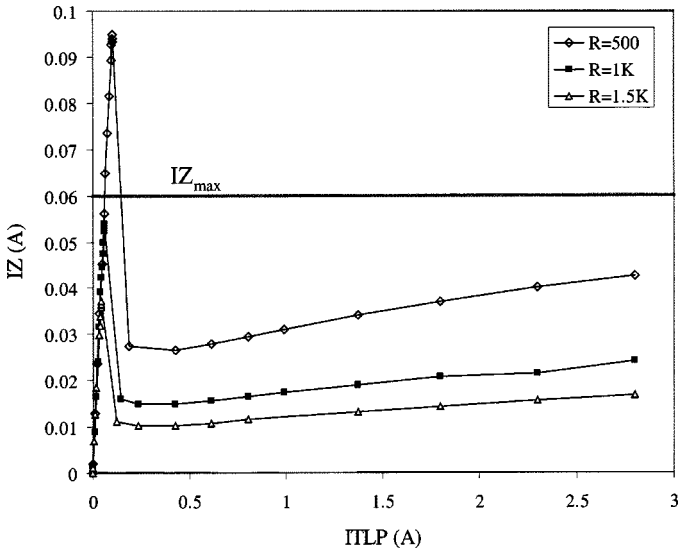
Fig. 10. Electrical schematic of the two-stage ESD protection circuit used to protect a CMOS inverter input.

is designed to absorb most of the ESD energy. Such an ESD protection scheme is very useful when the device that can provide the required ESD robustness features a trigger voltage higher than the breakdown voltage of the device to be protected. Optimization of this simple circuit requires proper sizing of the series resistance, R and the Zener diode taking into account the trigger voltages of both stages. The size of the Zener diode is defined from the results of the TLP characterization on this device and from a tradeoff between maximum Zener current and silicon area. The value of the series resistance is then adjusted to limit the voltage rise on the inverter input.

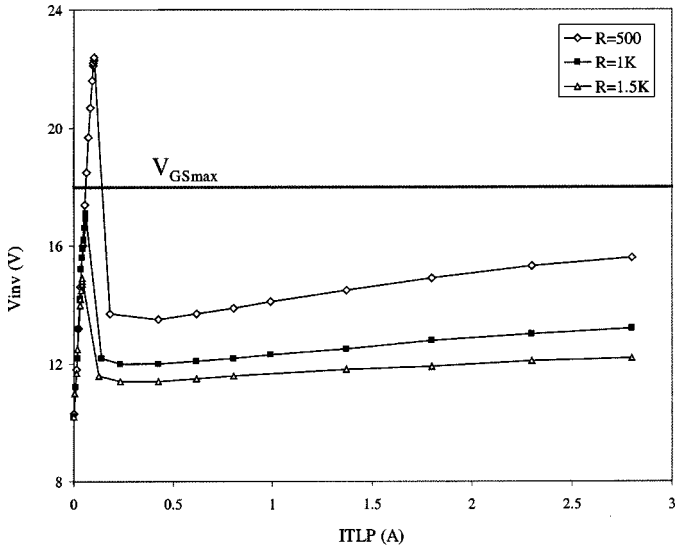
Fig. 11 plots both the Zener diode current, I_Z and the inverter input voltage, V_{inv} during TLP simulation. Clearly, for the chosen Zener diode size, a 1-kΩ minimum value for the series resistor is required to warrant a safe operation of the ESD protection within technological design margins $(V_{GS\max}, I_{z\max})$.

VI. Conclusion

Detailed analysis of the mechanisms involved under ESD stress in a vertical grounded-base n-p-n bipolar transistor is pro-



(a)



(b)

Fig. 11. TLP simulation of the ESD circuit of Fig. 9 protecting a CMOS inverter for three values of the series resistor: (a) Zener diode current (IZ) and (b) inverter input voltage (Vinv).

posed. Emphasis is placed on the impact ionization mechanism due to the high current density flowing in the structure which provides a good ESD robustness. Moreover, it accounts for particular features such as snapback holding voltage that is much lower than expected. This deep insight gained into the physics of ESD stress proved very helpful for proposing a new avalanche current model based on the resolution of the ionization integral for the planar junction. This new model offers good convergence as well as a good prediction of the ESD behavior.

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She has recently joined the European Technology Development Group as a permanent employee. Her research focuses on the study, optimization, and compact modeling of ESD protection structures for CMOS and BiCMOS technologies.

Christelle Delage was born in Perigueux, France, in 1972. She received the Engineering and Ph.D. degrees from the National Polytechnique Institute of Toulouse, France, in 1996 and 1999, respectively.

She worked on the design and simulation of ESD protection structures for bipolar and BiCMOS technologies. In 1999, she joined ON Semiconductor, Toulouse, as an analog IC designer. She is involved in new product development for wireless business.

Marise Bafleur received the Engineer degree in solid-state physics in 1979 from the Institut National des Sciences Appliquées of Toulouse, France, and the Ph.D. degree and the State Doctorate degree in 1982 and 1987, respectively, from Paul Sabatier University, Toulouse.

From 1979 to 1982, she worked on defect characterization of molecular beam epitaxy grown GaAs layers. In 1983, she joined the Centre National de la Recherche Scientifique (CNRS) at the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS), Toulouse. From 1983 to 1987, after one year spent at IBM-COMPEC, Bordeaux, France, working on the characterization of VLSI IC's using failure analysis techniques, she devoted her research activities to CMOS digital circuit design and modeling of their dynamic behavior. From 1987 to 1994, she oriented her activity toward smart power ICs design and technology. From 1991 to 1994, she was project leader in the PROMETHEUS/PROCHIP European program devoted to the introduction of smart power in the automotive environment in cooperation with Renault and Peugeot automotive manufacturers. Then she spent three years with Motorola, Phoenix, AZ, first as a low-power designer and then working on TCAD predictive engineering. Since the end of 1997, she has rejoined the LAAS Research Institute leading research activity in the field of electrostatic discharge (ESD) in CMOS and smart power technologies.

Nicolas Nolhier was born in Pau, France, in 1966. He received the Ph.D. degree in electronics from the National Institute of Applied Sciences (INSA), Toulouse, France, in 1992.

Since 1993, he has been a Lecturer with the University Paul Sabatier, Toulouse, and he has joined the Laboratoire d'Architecture et d'Analyse des Systèmes (LAAS-CNRS). First motivated by rapid thermal processing control and modeling, his interests moved in power devices design and simulations. In 1996, he initiated, in LAAS, the study of ESD protections using 2-D electrothermal simulations, and investigated in TLP experiments. He is also active in power MOSFET modeling for RF applications.

Jean-Marie Dorkel was born in Stiring-Wendel, France, on October 2, 1948. He received the Ph.D. degree in electronics in 1974 and the Docteur ès Sciences degree in 1982, both from the Paul Sabatier University, Toulouse, France.

He has worked on power rectifier behavior under surge-current conditions, on thermal and electrothermal modeling of power devices and circuits. He is presently a Professor at the National Institute of Applied Sciences of Toulouse and works with a research group on power devices and integration at the Laboratoire d'Analyze et d'Architecture des Systèmes du Centre National de La Recherche Scientifique, Toulouse.

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From 1981 to 1999, he was with Motorola working in the fields of device engineering, process development, automotive IC design. He is now with ON Semiconductor in wireless power management IC design.

Nicolas Mauran was born in Muret, France, in 1974. He received the degree of technician in physical measurements of the Institut Universitaire de Technologie of Toulouse, France, in 1995. He is currently pursuing the engineer degree through the Conservatoire National des Arts & Métiers of Toulouse.

He joined the Laboratoire d'Architecture et d'Analyse des Systèmes (LAAS-CNRS) in 1996, where he is responsible for the Semiconductor Characterization Center.

David Trémouilles was born in Villefranche de Rouergue, France, in 1976. He received the M.S. degree in electrical engineering from the Institut National des Sciences Appliquées of Toulouse, France, in 2000. He is currently pursuing the Ph.D. degree at the Laboratoire d'Analyze et d'Architecture des Systèmes in collaboration with ON Semiconductor.

His research activity focuses on the design optimization and simulation of ESD protection structures for BiCMOS technologies.

Philippe Perdu was born in 1952 at Amiens (80), France. He received the Engineer degree, in electronics from C.N.A.M of Toulouse in 1985 and the Ph.D. degree in electronics from Paul Sabatier University in Toulouse on April 1994.

At CNES, the French National Space Agency, he is in charge of a laboratory dedicated to integrated circuit analysis. He leads the expertise on VLSI circuits of diversified technologies for space applications where quality and reliability are key issues.