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Analysis and Control of Input-Parallel Output-Series Based Combined DC/DC Converter With Modified Connection in Output Filter Circuit

JIANG YOU[1], (Member, IEEE), LIANBIN CHENG[1], BIN FU[2], AND MENGLU DENG[1]
[1]College of Automation, Harbin Engineering University, Harbin 150001, China
[2]School of Light Industry, Harbin University of Commerce, Harbin 150001, China

Corresponding author: Bin Fu (fubinhcu@hotmail.com)

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ABSTRACT Input-parallel output-series (IPOS)-based combined converter is usually used in the situation with low input voltage and high output voltage to satisfy the requirements in switch voltage stress reduction and power expansion. In such a system, the voltage balance of filter capacitor in the output side or current sharing in the input side usually used to guarantee the control performance of the conversion system. In this paper, a phase-shifted full bridge (PSFB)-based IPOS converter with modified connection of output filter circuit used for the wide variation of input voltage is proposed, which is beneficial to reduce ripple current of filter inductor significantly. A control scheme using the same phase shifting for the two different modules of this IPOS converter is detailedly investigated with both steady state and small signal model-based analysis, it manifests that special voltage balance and current sharing control scheme are not necessary for IPOS system under the common phase shifting control method. And the small signal transfer functions of this topology used for dual loop control system design are also developed. The simulation and experiment results are presented to validate the analysis and control scheme.

INDEX TERMS Input-parallel output-series, combined converter, phase shifted full bridge, voltage balance.

I. INTRODUCTION

Combined DC/DC converters constituted through parallel and series connection are widely concerned in recent years, there are mainly four types of these converters, input-series output-parallel (ISOP) converter, input-series output-series (ISOS) converter, input-parallel output-series (IPOS) converter, and input-parallel output-parallel (IPOP) converter [1]. Each individual has its own characteristic and application area, a brief list is summarized in Table 1 for comparison. For these converters, the IPOS based combined converter is a favorable candidate in the fields of energy storage, renewable energy generation and high voltage pulse generator etc. due to its high gain and conversion efficiency compared to two-stage power conversion system [2]–[7]. Generally, in such a conversion system, the voltage value of power source is relatively low, while the output of the converter is interfaced to a high voltage DC bus, therefore, if there is only one DC/DC module is adopted, the input current of converter is large that will lead high current stress on the input side power switches, while the power switches in the output side have to tolerate high voltage stress. The IPOS converter usually consists of multiple DC/DC converter modules of lower rating, and the DC/DC converter modules can be either non-isolated [8]–[10] (e.g., using Boost and bidirectional converter) or isolated topologies [11]–[15] (e.g., using PSFB and dual active bridge). Since the large input current is shared by the input-parallel configuration, the conduction losses of power switches can be reduced which is conducive to improve power conversion efficiency [16]. Furthermore, by employing interleaved modulation method, the input current ripple can be reduced effectively [17].

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TABLE 1. Brief list of different combination mode.

	Main application situation	Key issues
ISOP	transfer high voltage to low voltage with power expansion	voltage balance in input side, and current sharing in output side
ISOS	high input/output voltage	voltage balance in output/input side
IPOS	transfer low voltage to high voltage with power expansion	voltage balance in output side
IPOP	power expansion	current sharing of output current

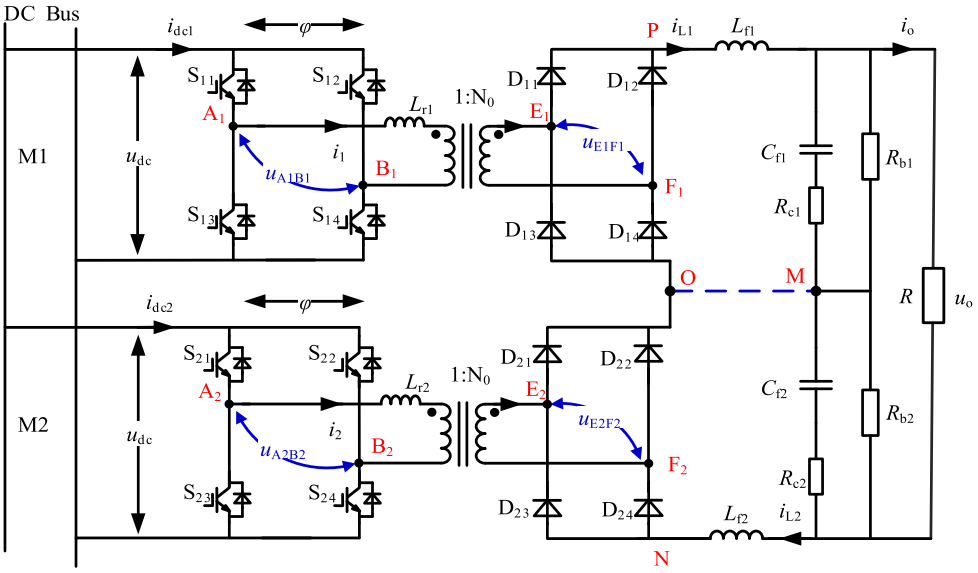

FIGURE 1. The topology of the IPOS combined converter.

In the IPOS converter control system, voltage balance in the output side can be guaranteed through active control method. For example, in [18], voltage balance is obtained by controlling the output voltage of each individual module's output voltage respectively. In [19], different modules share the same outer voltage control loop, the output of the voltage controller is performed as the reference signal for a particular input current control loop of each module, by this way, input current sharing and voltage balance can be achieved accordingly if the conversion efficiency of each module is very approximate. A novel voltage balance control method is proposed in [20], where the output voltage of each module is sampled, and the maximum output voltage value is used as the reference signal for all the modules to track. Though these mentioned methods are effective, extra voltage sensors and control loops are required, the complexity and cost of control system development will be increased accordingly. A new master–slave control scheme and distributed voltage sharing controller are proposed in [21] that can realize power sharing under different operating conditions. By allowing healthy module to replace the master module in failure status, fault-tolerant operation can be achieved by this control scheme.

On the other hand, almost in all the PSFB based IPOS converter system, each module has its own independent output LC filter for consideration of modularization (e.g., the point O and point M are connected together in Fig. 1), however, modularization is not always a very important requirement for all the application situations, a rational modification might bring other performance improvement.

In this paper, a PSFB based IPOS combined converter with wide change of input voltage is investigated. In order to reduce the inductor ripple current of output filter in the variation range of the input voltage, a modified connection of output filter circuit is proposed that is beneficial to significantly decrease the inductor ripple current of output filter. Therefore, the value of filter inductor can be reduced potentially, the weight and cost of the inductor can also be decreased accordingly. And a simplified control scheme without special current sharing and voltage balance strategies is adopted for this combined converter, the same phase shifting is used to control the two full bridges in the primary side of high frequency transformers (HFT). While the voltage balance of capacitors in the output filter can be guaranteed through reducing the parameter deviations of different modules, which is achievable in practices. Theoretical analysis and experiment results are provided to prove the effectiveness of the proposed methods.

The rest of this paper is organized as follows. In Section II, the topology, modulation scheme and relevant performance analysis of the proposed converter are presented. The small

signal model and control system design are given in section III. Simulation and experimental results that validate the effectiveness of the proposed methods are presented in Section IV. Finally, the conclusion is drawn in Section V.

II. TOPOLOGY, MODULATION AND ANALYSIS

A. INVESTIGATION ON RIPPLE CURRENT AND VOLTAGE

The topology of the input-parallel output series converter is shown in Fig. 1. In this figure, u_{dc} and u_o are input voltage and output voltage respectively. L_{f1} and L_{f2} are output filter inductors. C_{f1} and C_{f2} are output filter capacitors, and R_{c1} and R_{c2} are the equivalent series resistances (ESR) of C_{f1} and C_{f2} respectively. R_{b1} and R_{b2} are voltage balance resistor of C_{f1} and C_{f2}, R is used to represent load. Ideally, $R_{b1} = R_{b2} >> R$. L_{r1} and L_{r2} are resonant inductor in series with primary windings of the two HFTs. The turns ratio of the two HFTs are all 1: N_0. Compared with the conventional IPOS converter, no connection between point O and point M is the prominent characteristic of this topology.

The duty cycles of all the switches, S_{11}-S_{14} (in module 1, denoted by M1), and S_{21}-S_{24} (in module 2, denoted by M2) are 50%. In the proposed method, the phase shifting between the two legs of each module is φ, and the switching signals of M2 lag $T_s/4$, (T_s is the switching period) behind that of M1 as shown in Fig. 2, that means M1 and M2 are interleaved paralleled on the input side DC bus. As indicated in Fig. 2, the frequency of u_{E1F1} and u_{E2F2} is $2f_s$ ($f_s = 1/T_s$) by utilization of full bridge diode rectifier. Furthermore, the frequency of fluctuation in u_{PN} and ripple current of inductor is $4f_s$ due to 90° phase shifting ($T_s/4$ of time delay) of driving signals of M1 and M2.

In Fig. 2 (a), the phase shifting, φ of each module is less than 90°, that means the equivalent duty cycle, D of u_{E1F1} and u_{E2F2} is larger than 0.5, otherwise, if $\varphi > 90°$, then D is less than 0.5 as shown in Fig. 2 (b). In Fig. 2 (a), assuming $L_{f1} = L_{f2} = L_f$, the peak-to-peak value of inductor ripple current can be formulated as (1).

$$\Delta I_L = \begin{cases} \dfrac{U_o(1-D)(2D-1)T_s}{8DL_f}, & D \geq 0.5 \\ \dfrac{U_o(1-2D)T_s}{8L_f}, & D < 0.5 \end{cases} \tag{1}$$

In (1), U_{dc} and U_o are the steady state value of u_{dc} and u_o respectively.

For comparison, supposing the points O and M are connected, then the peak-to-peak of inductor ripple current can be expressed as (2).

$$\Delta I_L = \frac{(2N_0U_{dc} - U_o)DT_s}{4L_f} = \frac{U_o(1-D)T_s}{4L_f} \tag{2}$$

For (1) and (2), defining

$$I_{base} = \frac{U_oT_s}{4L_f} \tag{3}$$

the relationship between D and $\Delta I_L/I_{base}$ under different conditions are shown in Fig. 3 using the parameters listed in Table 2. As shown in this figure, the inductor ripple current can be reduced in the region of (0, 1) if the point O and point M are disconnected. Compared to the case with connection of the points O and M, the percentage of ripple current reduction (PRCR) is increased from 0.5 to 1 in the duty cycle region of (0, 0.5), and the percentage is decreased from 1 to 0.5 in the duty cycle region of (0.5, 1) respectively.

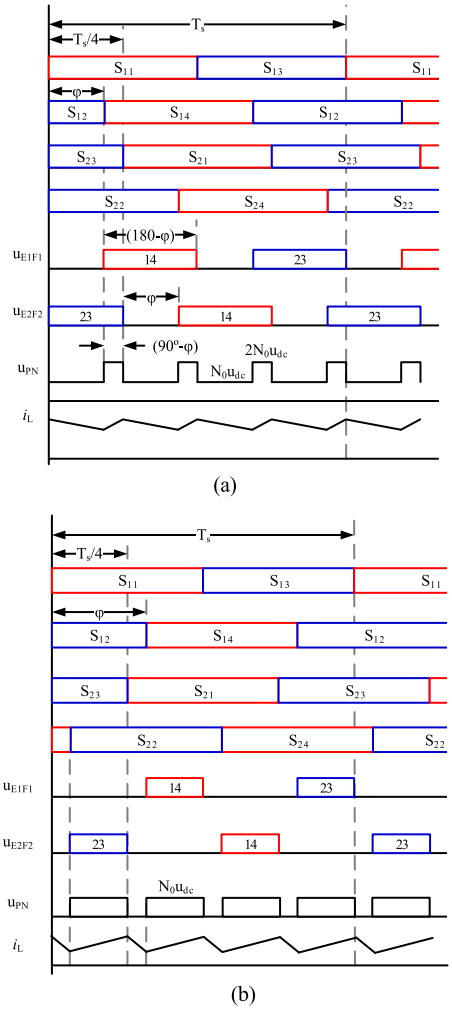

FIGURE 2. Switching signals and waveforms (a) $\varphi < 90°$ ($D > 0.5$) and (b) $\varphi > 90°$. ($D < 0.5$).

From Fig. 1, neglecting the influence of R_{c1}, R_{c2}, R_{b1} and R_{b2}, the inductor currents, i_{L1} and i_{L2} can be written as (4).

$$\begin{cases} i_{L1} = C_{f1}\dfrac{du_{o1}}{dt} + \dfrac{u_o}{R} \\ i_{L2} = C_{f2}\dfrac{du_{o2}}{dt} + \dfrac{u_o}{R} \end{cases} \tag{4}$$

Assuming $C_{f1} = C_{f2} = C_f$ and without connection of points O and M, (5) can be obtained by adding the two equations in (4) together ($i_{L1} = i_{L2} = i_L$).

$$C_f\frac{du_o}{dt} = 2(i_L - i_o) = \Delta i_o \tag{5}$$

TABLE 2. Simulation and experimental parameters.

Parameter	Nominal value	Experiment value
Input DC voltage (u_{dc})	350V-600V	350V-600V
Nominal output voltage (u_o)	540V	540V
Inductor (L_{f1}/L_{f2})	0.4mH	0.412mH/0.406mH
Filter capacitance (C_{f1}/C_{f2})	3300μF	3271μF/3284μF
Resonant inductor (L_{r1}/L_{r2})	20μH	20.37μH/20.33μH
Adjustable load resistor (R)	14.5Ω-500Ω	14.5Ω-500Ω
Switching frequency (f_s)	13kHz	13kHz
Peak value of carrier wave (V_m)	6460	6460
Voltage balance resistor (R_{b1}/R_{b2})	18kΩ	17.92kΩ/17.93kΩ
Turns ratio	1:1	1:1

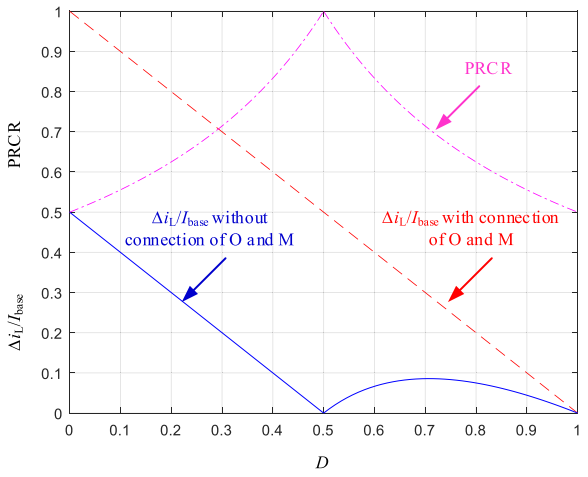

FIGURE 3. Comparison of $\Delta I_L/I_{base}$ versus D under different conditions.

It can be seen from (5) that the peak value of Δi_o is just two times the value of ΔI_L in (1), then the voltage ripple of the filter capacitor can be written as (6) according to the ampere-second balance principle (the average value of capacitor current in each $T_s/4$ is zero in this paper) of capacitor.

$$\Delta u_o = \begin{cases} \dfrac{U_o(1-D)(2D-1)T_s^2}{128DL_fC_f}, & D \geq 0.5 \\ \dfrac{U_o(1-2D)T_s^2}{128L_fC_f}, & D < 0.5 \end{cases} \tag{6}$$

On the other hand, if the points O and M are connected, the corresponding currents of inductor L_{f1} and L_{f2} are given in Fig. 4 (M1 and M2 are still interleaved paralleled on the input side DC bus). In this condition, though (4) is still held, the capacitor current is changed as (7).

$$C_f\frac{du_o}{dt} = (i_{L1} - i_o) + (i_{L2} - i_o) = \Delta i_o \tag{7}$$

That means Δi_o is the summation of the ripple currents of i_{L1} and i_{L2}. According to Fig. 4, the peak-to-peak value of Δi_o can be derived as (8), as shown at the bottom of the next page. Similarly, when the points O and M are connected, the voltage ripple of the filter capacitor can be calculated as (9) if the ampere-second balance principle is applied to the output filter capacitor of the IPOS based combined converter.

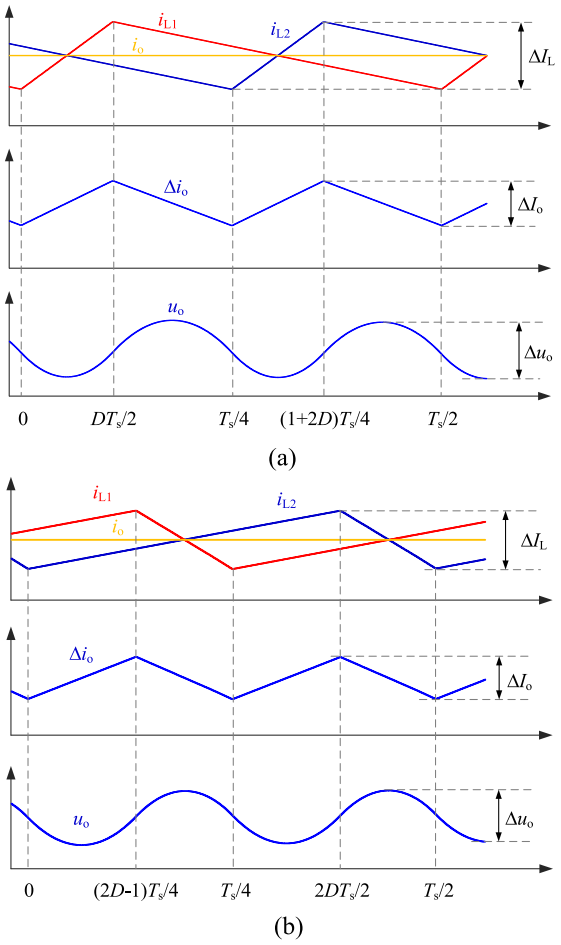

FIGURE 4. Inductor and capacitor currents with connection of point O and M. (a) D < 0.5 and (b) D > 0.5.

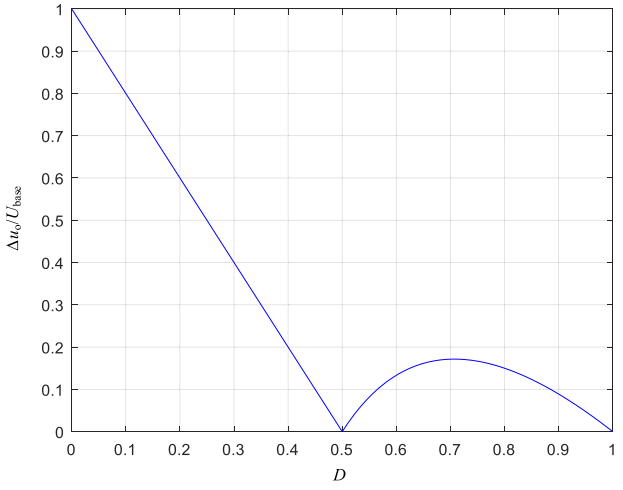

FIGURE 5. Comparison of $\Delta u_o/U_{base}$ versus D.

$$\Delta u_o = \begin{cases} \dfrac{U_o(2D-1)(1-D)T_s^2}{128DL_fC_f}, & D \geq 0.5 \\ \dfrac{U_o(1-D)(1-2D)T_s^2}{128(1-D)L_fC_f}, & D < 0.5 \end{cases} \tag{9}$$

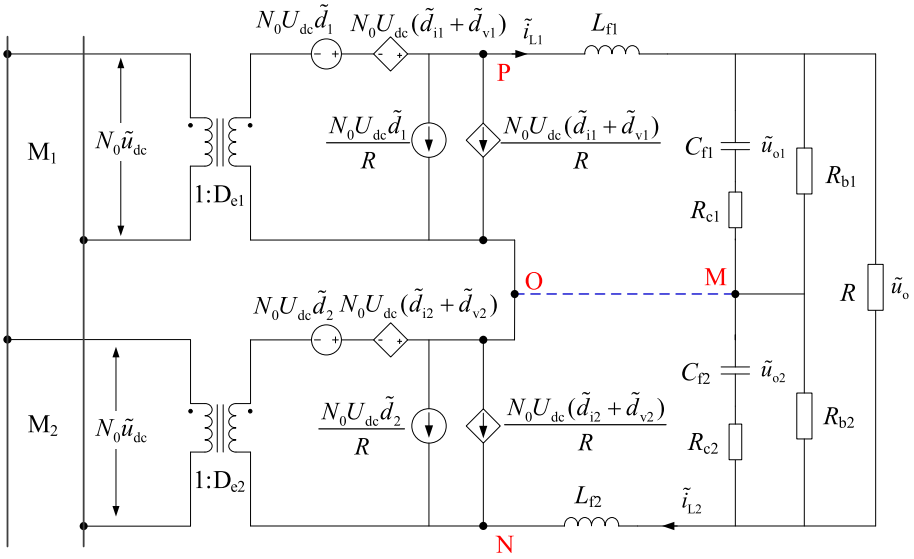

FIGURE 6. The equivalent small signal circuit model of the IPOS converter.

By defining

$$U_{base}=\frac{U_oT_s^2}{128L_fC_f} \tag{10}$$

the relationships between D and $\Delta u_o/U_{base}$ in (6) and (9) are the same, that means the output voltage ripples under this two different conditions are identical. The plot of D versus $\Delta u_o/U_{base}$ is shown in Fig. 5 using the parameters listed in Table 2. It can be seen in this figure that the voltage ripple is monotonously reduced in the region of (0, 0.5), and in the region of (0.5, 1) there is a maximum value of voltage ripple near $D=0.7$.

B. INVESTIGATION ON VOLTAGE BALANCE

By utilizing the small signal model of PSFB converter developed in [22], [23], the equivalent small signal circuit model of the proposed IPOS converter in Fig.1 can be derived in Fig. 6.

In this figure, D_{ej} $(j=1,2)$ is the steady-state value of the effective duty cycle of u_{EjFj}, and $\tilde{d}_j$ is the small signal disturbance of the equivalent duty cycle (corresponding to phase shifting φ) of u_{AjBj} in Fig. 1 respectively. $\tilde{d}_{ij}$ and $\tilde{d}_{vj}$ represent the small signal disturbances of duty cycle losses caused by the fluctuation of inductor current and input voltage respectively, the expressions of $\tilde{d}_{ij}$ and $\tilde{d}_{vj}$ are given in (11).

$$\begin{cases}\tilde{d}_{ij}=-\dfrac{4N_0L_{rj}f_s}{U_{dc}}\tilde{i}_L=-\dfrac{R_{dj}}{N_0U_{dc}}\tilde{i}_L\\ \tilde{d}_{vj}=\dfrac{R_{dj}I_L}{N_0U_{dc}^2}\tilde{u}_{dc}\end{cases}\quad(j=1,2) \tag{11}$$

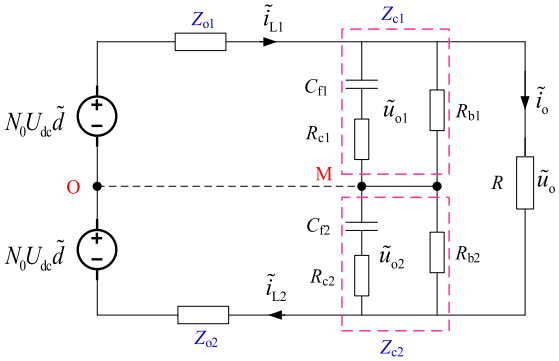

FIGURE 7. Simplified small signal circuit model of the proposed converter.

In (11), I_L and $\tilde{i}_L$ are the steady-state value and small signal disturbance of the inductor current respectively. Neglecting the influence of u_{dc}, Fig. 6 can be simplified to Fig. 7 ($\tilde{d}_1=\tilde{d}_2=\tilde{d}$ is assumed in this figure).

In Fig. 7, the expressions of Z_{o1} and Z_{o2}, Z_{c1} and Z_{c2} are given in (12) and (13) respectively.

$$\begin{cases}Z_{o1}=R_{d1}+L_{f1}s\\ Z_{o2}=R_{d2}+L_{f2}s\end{cases} \tag{12}$$

$$\begin{cases}Z_{c1}=\dfrac{R_{b1}+R_{c1}R_{b1}C_{f1}s}{(R_{b1}+R_{c1})C_{f1}s+1}\\ Z_{c2}=\dfrac{R_{b2}+R_{c2}R_{b2}C_{f2}s}{(R_{b2}+R_{c2})C_{f2}s+1}\end{cases} \tag{13}$$

$$\begin{cases}\Delta I_o=\Delta I_L-\dfrac{T_s/4-(2D-1)T_s/4}{DT_s/2}\Delta I_L=\dfrac{(2D-1)(2N_0U_{dc}-U_o)T_s}{4L_f}=\dfrac{U_o(2D-1)(1-D)T_s}{4DL_f}, & D>0.5\\ \Delta I_o=\dfrac{2\Delta I_L(T_s/4-DT_s/2)}{T_s/2-DT_s/2}\Delta I_L=\dfrac{(2N_0U_{dc}-U_o)(1-2D)DT_s}{4(1-D)L_f}=\dfrac{U_o(1-D)(1-2D)T_s}{4(1-D)L_f}, & D<0.5\end{cases} \tag{8}$$

For the proposed scheme, since there is no connection between point O and point M, the ratio in (14) can be used to evaluate the voltage deviation between $\tilde{u}_{o1}$ and $\tilde{u}_{o2}$.

$$G_1 = \frac{\tilde{u}_{o1} - \tilde{u}_{o2}}{\tilde{u}_o} = \frac{Z_{c1} - Z_{c2}}{Z_{c1} + Z_{c2}} \tag{14}$$

Furthermore, if point O and point M are connected in Fig. 7, then the voltage deviation between $\tilde{u}_{o1}$ and $\tilde{u}_{o2}$ can be evaluated by (15) according to circuit theory.

$$G_2 = \frac{\tilde{u}_{o1} - \tilde{u}_{o2}}{\tilde{u}_o} = \frac{Z_1 - Z_2}{Z_1 + Z_2} \tag{15}$$

where, the expressions of Z_1 and Z_1 are formulated in (16), as shown at the bottom of the next page.

From (13) and (14), it can be concluded that the voltage balance performance is affected by the output filter capacitors (C_{f1} and C_{f2}), ESR of capacitor (R_{c1} and R_{c2}) and voltage balance resistor (R_{b1} and R_{b2}) in the case without connection of point O and point M. While as shown in (15) and (16), if the point O and point M are connected together, the transformer resonant inductor and duty cycle loss (indicated by R_{d1} and R_{d2}) also have influence on the voltage deviation between u_{o1} and u_{o2}. Ideally, if there are no parameter deviations, (14) and (15) will always be zero, that indicates voltage balance can be completely realized both in dynamic and steady states. Using the parameter values listed in Table 2, deviations are assumed for different parameters to evaluate the voltage balance performance of the capacitor voltages, u_{o1} and u_{o2} in this section.

1) THE POINTS O AND M ARE UNCONNECTED

Assuming the disturbance in u_o can be represented by a unit step signal, the initial voltage deviation between u_{o1} and u_{o2} can be expressed as (17) according to the initial value theorem if point O and point M are unconnected.

$$\begin{aligned}(u_{o1} - u_{o2})|_{t=0+} &= \lim_{s\to\infty} s \cdot G_1 \cdot \frac{1}{s} \\ &= \frac{R_{b1}R_{b2}(R_{c1}-R_{c2})+R_{c1}R_{c2}(R_{b1}-R_{b2})}{R_{b1}R_{b2}(R_{c1}+R_{c2})+R_{c1}R_{c2}(R_{b1}+R_{b2})}\end{aligned} \tag{17}$$

And according to the final value theorem, the steady state value of the deviation between u_{o1} and u_{o2} in this case can be calculated as (18).

$$(u_{o1} - u_{o2})|_{t=\infty} = \lim_{s\to 0} s \cdot G_1 \cdot \frac{1}{s} = \frac{R_{b1} - R_{b2}}{R_{b1} + R_{b2}} \tag{18}$$

While if the voltage balance resistors, R_{b1} and R_{b2} are cancelled, the initial and steady state value of (u_{o1}-u_{o2}) can be obtained as (19) and (20) respectively.

$$(u_{o1} - u_{o2})|_{t=0+} = \lim_{s\to\infty} s \cdot G_1 \cdot \frac{1}{s} = \frac{R_{c1} - R_{c2}}{R_{c1} + R_{c2}} \tag{19}$$

$$(u_{o1} - u_{o2})|_{t=\infty} = \lim_{s\to 0} s \cdot G_1 \cdot \frac{1}{s} = \frac{C_2 - C_1}{C_2 + C_1} \tag{20}$$

It can be concluded from (18) and (20) that if there is a significant difference between C_1 and C_2, the resulted voltage deviation in steady state can be reduced by selecting

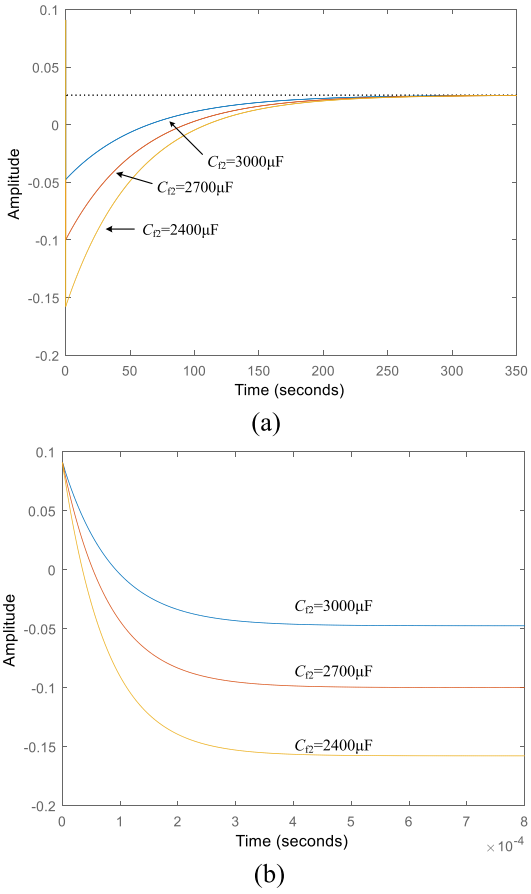

FIGURE 8. Step response without connection of points O and M (a) with R_{b1} and R_{b2} and (b) without R_{b1} and R_{b2}.

$R_{b1} = R_{b2}$ (high accuracy resistor is obtainable in practices). And since $R_{bj} >> R_{cj}$, (17) is very approximate to (19), the amplitude of voltage deviation in transient state process is determined by the identical of capacitor ESRs.

In Fig. 8, the values of R_{b1} and R_{b2} are 20kΩ and 19kΩ (5% difference from R_{b1}) respectively, and R_{c1} and R_{c2} are assumed 30mΩ and 25mΩ respectively. C_{f1} is fixed as 3300μF. Comparing Fig. 8 (a) with Fig. 8 (b), it can be seen that voltage deviation in the steady state can be reduced by introducing voltage balance resistors. The higher accuracy of the voltage balance resistors, the lower deviation between u_{o1} and u_{o2}. However, since the time constants defined by $R_{b1}C_{f1}$ and $R_{b2}C_{f2}$ are large (about 60s in Fig. 8 (a)), it will take a relatively long time before the voltage deviation can be damped to its steady state value.

2) THE POINT O AND POINT M ARE CONNECTED

If point O and point M are connected together with consideration of voltage balance resistors, (21) and (22) can be derived according to the initial value theorem and the final value theorem respectively (as shown at the bottom of the next page). If the voltage balance resistors are removed,

(21) and (22) can be rewritten as (23) and (24).

$$(u_{o1}-u_{o2})|_{t=0+}=\frac{R(L_{f1}R_{c2}-L_{f2}R_{c1})+2R_{c1}R_{c2}(L_{f1}-L_{f2})}{R(L_{f1}R_{c2}+L_{f2}R_{c1})} \tag{23}$$

$$(u_{o1}-u_{o2})|_{t=\infty}=\frac{(R_{d1}-R_{d2})}{R}=\frac{4N_0^2f_s(L_{r1}-L_{r2})}{R} \tag{24}$$

As shown in (22) and (24), the voltage deviation between u_{o1} and u_{o2} in steady state can be determined by the difference between R_{d1} and R_{d2}. Since the values of R_{b1} and R_{b2} are much higher than the values of R_{d1} and R_{d2}, the voltage balance resistors almost have no influence on reducing the voltage deviation in this case. In Fig. 9, the values of R_{b1} and R_{b2} are also 20kΩ and 19kΩ (5% difference from R_{b1}) respectively, and R_{d1} is fixed as 1.3Ω ($L_{r1}=25\mu$H), the values of R_{d2} are calculated as 1.56Ω, 1.82Ω and 2.08Ω with selecting L_{r2} as 30μH, 35μH and 40μH respectively in module 2. It can be seen that the corresponding steady state voltage deviations in Fig. 9 (a) and Fig. 9 (b) are almost the same with the three different values of L_{r2} which is consistent with the previous analysis.

III. SMALL SIGNAL MODEL AND CONTROL SYSTEM DESIGN

Ignoring the impact of R_bj (the value of R_bj is much larger than that of load resistor, R) in Fig. 6, (25) can be deduced, as shown at the bottom of the next page according to the Kirchhoff's voltage law. Assuming the corresponding values of different parameters are identical in the two PSFB modules, that is, $R_{c1}=R_{c2}=R_c$, $L_{r1}=L_{r2}=L_r$, $L_{f1}=L_{f2}=L_f$ and $D_{e1}=D_{e2}=D_e$, then (25) can be rewritten as (26), as shown at the bottom of the next page. Considering the influence of capacitor ESR, the small signal transfer function of $\tilde{i}_L$-to-$\tilde{u}_o$ can be derived in (27).

$$G_{ui}=\frac{\tilde{u}_o}{\tilde{i}_L}=\frac{2RR_cC_fs+2R}{(RC_f+2R_cC_f)s+2} \tag{27}$$

Substituting (27) into (26), and let $\tilde{u}_{dc}=0$, the transfer function of $\tilde{d}$-to-$\tilde{u}_o$ can be obtained as (28), as shown at the bottom of the next page. Similarly, by setting $\tilde{u}_{dc}=0$, the transfer function of $\tilde{d}$-to-$\tilde{i}_L$ in (29), as shown at the bottom of the next page, can be also derived by combining (26) with (27) to cancel $\tilde{u}_o$.

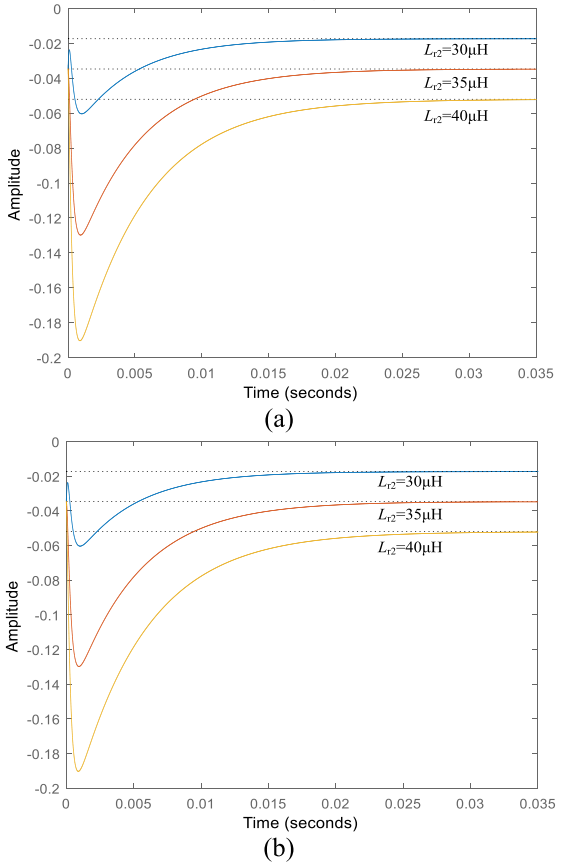

FIGURE 9. Step response with connection of points O and M (a) with R_{b1} and R_{b2} and (b) without R_{b1} and R_{b2}.

The dual loop control scheme developed to control the proposed IPOS converter is shown in Fig. 10. In this figure, two compensation controllers should be designed for the two control loops, the voltage controller, H_v and current controller, H_c are given in (30).

$$\begin{cases} H_v(s)=1.16+\dfrac{23.3}{s} \\ H_c(s)=\dfrac{9.2\times10^6s^2+7.36\times10^{10}s+1.104\times10^{14}}{s^3+1.4\times10^5s+4.9\times10^9s} \end{cases} \tag{30}$$

In order to investigate the stable margin of the design results despite the changes of input voltage, u_{dc} and the

$$\begin{cases} Z_1=\dfrac{(RZ_{c2}+RZ_{o2}-Z_{c2}Z_{o1}+Z_{c2}Z_{o2})Z_{c1}}{(RZ_{c2}+RZ_{o2}+Z_{c2}Z_{o1}+Z_{c2}Z_{o2}+Z_{o1}Z_{o2})Z_{c1}+RZ_{c2}Z_{o1}+RZ_{o1}Z_{o2}+Z_{c2}Z_{o1}Z_{o2}} \\ Z_2=\dfrac{(RZ_{c1}+RZ_{o1}-Z_{c1}Z_{o2}+Z_{c1}Z_{o1})Z_{c2}}{(RZ_{c2}+RZ_{o2}+Z_{c2}Z_{o1}+Z_{c2}Z_{o2}+Z_{o1}Z_{o2})Z_{c1}+RZ_{c2}Z_{o1}+RZ_{o1}Z_{o2}+Z_{c2}Z_{o1}Z_{o2}} \end{cases} \tag{16}$$

$$(u_{o1}-u_{o2})|_{t=0+}=\frac{RR_{b1}R_{b2}(L_{f1}R_{c2}-L_{f2}R_{c1})+RR_{c1}R_{c2}(L_{f1}R_{b2}-L_{f2}R_{b1})+2R_{b1}R_{b2}R_{c1}R_{c2}(L_{f1}-L_{f2})}{RR_{b1}R_{b2}(L_{f1}R_{c2}+L_{f2}R_{c1})+RR_{c1}R_{c2}(L_{f1}R_{b2}+L_{f2}R_{b1})} \tag{21}$$

$$(u_{o1}-u_{o2})|_{t=\infty}=\frac{R(R_{b2}R_{d1}-R_{b1}R_{d2})+2R_{b1}R_{b2}(R_{d1}-R_{d2})}{(2R_{b1}R_{b2}+R_{b1}R_{d2}+R_{b2}R_{d1})R} \tag{22}$$

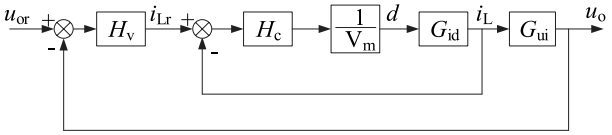

FIGURE 10. Dual loop control of the IPOS based combined converter.

load resistor, R, the Bode plots of the corrected current and voltage control loops using the controllers, H_v and H_c in (30) are shown in Fig. 11. As shown in this figure, the cutoff frequencies of the control systems are varied with the changes of u_{dc} and R. However, the corrected current and voltage control loops are still stable with the designed controller. In Fig. 11 (a) and (b), the Bode curves denoted by arrows represent the boundaries of the designs.

IV. SIMULATION AND EXPERIMENT VALIDATION

To verify the theoretical analysis and control scheme of the IPOS converter, a simulation model of the proposed system was developed in MATLAB Simulink environment. The simulation model parameters are listed in Table 2.

The simulation results under different conditions are shown in Fig. 12 and Fig. 13. In Fig. 12, the input voltage $u_{dc} = 600$V, there is 90° phase shifting between u_{A1B1} and u_{A2B2}, the load power is about 10kW ($R = 29\Omega$) and the equivalent duty cycle in primary side is about 0.482. As shown in Fig. 12 (a), u_{PN} changes from 0 to u_{dc}, the inductor ripple current is about 1A without connection of points O and M. While in Fig. 12 (b) under the same 10kW load, though u_{PO} and u_{ON} are all changed from 0 to u_{dc}, the ripple current of inductor is increased to about 13.5A if points O and M are connected. In Fig. 13, the input voltage u_{dc} is reduced to 350V, then u_{PN} changes from u_{dc} to $2u_{dc}$, the phase shifting between u_{A1B1} and u_{A2B2} is still 90°, and the load power is about 20kW ($R = 14.5\Omega$). In this case, the equivalent duty cycle in primary side is enhanced to about 0.91 to keep the output voltage at 540V constantly, the inductor ripple current in Fig. 13 (a) is about 2A without connection of points O and M. And in Fig. 13 (b), due to the significant decreases of u_{PO} and u_{ON}, the inductor ripple current is about 5A when the two points are connected.

The simulation results about dynamic performance test of closed-loop control system are shown in Fig. 14 with

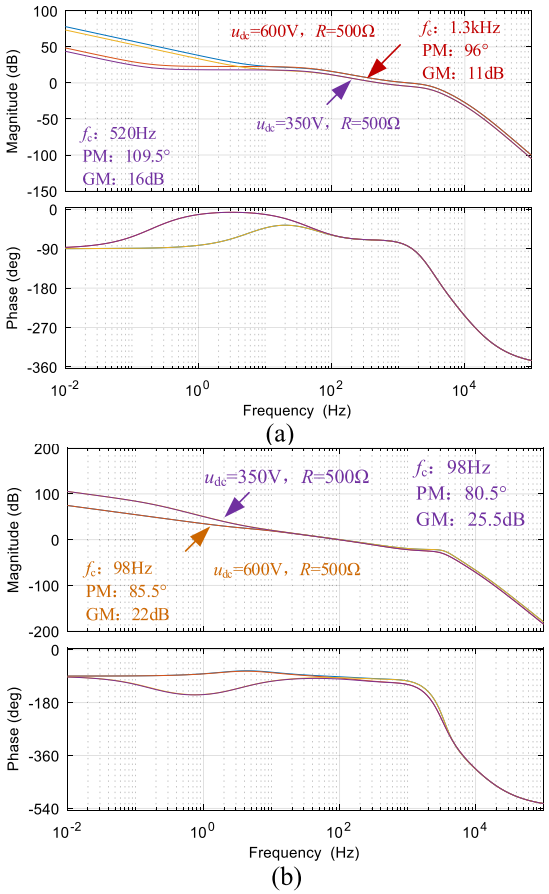

FIGURE 11. The Bode plots of the closed loop control system (a) current loop and (b) voltage loop.

$u_{dc} = 350$V, $R_{c1} = 50$mΩ, $R_{c2} = 30$mΩ, $L_{r1} = 30\mu$H, $L_{r2} = 20\mu$H, $C_{f1} = 3300\mu$F and $C_{f2} = 3100\mu$F are assumed, the ratio of $(C_{f1} - C_{f2})/C_{f1} + C_{f2})$ is 0.03125. In Fig. 14 (a) the points O and M are not connected, the initial load is about 580W. A sudden load (about 19.4kW) is added to the converter at 0.2s, a voltage drop about 26V is produced in u_o, and the voltage deviation between u_{o1} and u_{o2} is about 17V (540V × 0.03125 ≈ 17V) before and after the load change. According to Fig. 8 (a), it will take much longer time to decrease this voltage deviation. In Fig. 14 (b), the points O and M are connected, the same load change is adopted

$$N_0 D_{e1}\tilde{u}_{dc} + N_0 U_{dc}(\tilde{d}_{i1} + \tilde{d}_{v1} + \tilde{d}) + N_0 D_{e2}\tilde{u}_{dc} + N_0 U_{dc}(\tilde{d}_{i2} + \tilde{d}_{v2} + \tilde{d}) = L_{f1}\frac{d\tilde{i}_L}{dt} + L_{f2}\frac{d\tilde{i}_L}{dt} + \tilde{u}_{o1} + \tilde{u}_{o2} \tag{25}$$

$$(2D_e N_0 + \frac{16N_0^2 L_r D_e}{RT_s})\tilde{u}_{dc} + 2N_0 U_{dc}\tilde{d} = (2L_f s + \frac{8N_0^2 L_r}{T_s})\tilde{i}_L + \tilde{u}_o \tag{26}$$

$$G_{ud} = \frac{\tilde{u}_o}{\tilde{d}} = \frac{2N_0 U_{dc}(R_c C_f s + 1)}{(1 + \frac{2R_c}{R})L_f C_f s^2 + (\frac{2L_f}{R} + R_d C_f + R_c C_f + \frac{2R_d R_c}{R} C_f)s + \frac{2R_d}{R} + 1} \tag{28}$$

$$G_{id} = \frac{\tilde{i}_L}{\tilde{d}} = \frac{N_0 U_{dc}(1 + 2R_c/R)C_f s + 2N_0 U_{dc}/R}{(1 + \frac{2R_c}{R})L_f C_f s^2 + (\frac{2L_f}{R} + R_d C_f + R_c C_f + \frac{2R_d R_c}{R} C_f)s + \frac{2R_d}{R} + 1} \tag{29}$$

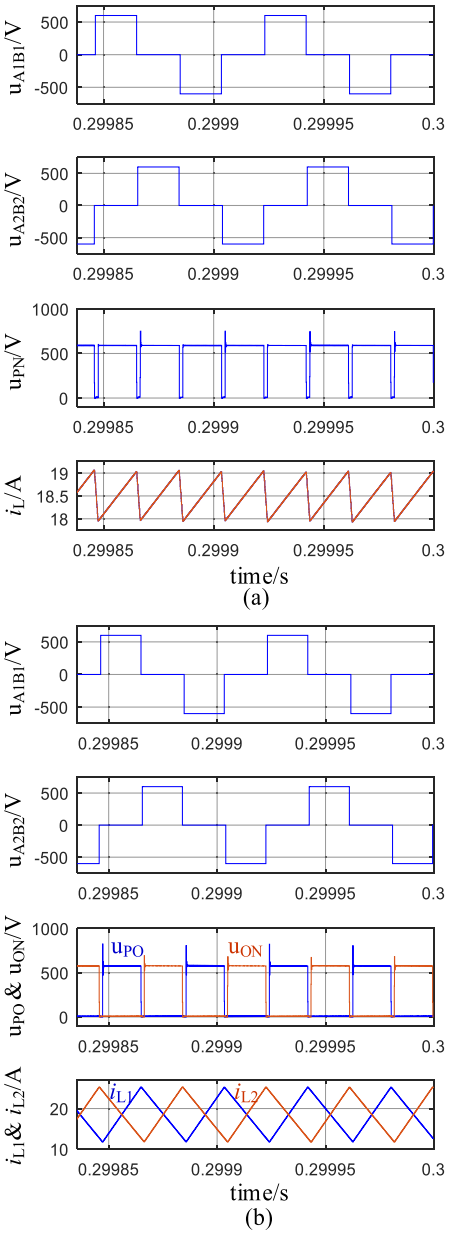

FIGURE 12. Simulation waveforms under $u_{dc} = 600V$, $R = 29\ \Omega$ and $D \approx 0.482$ (a) without connection of point O and point M and (b) with connection of point O and point M.

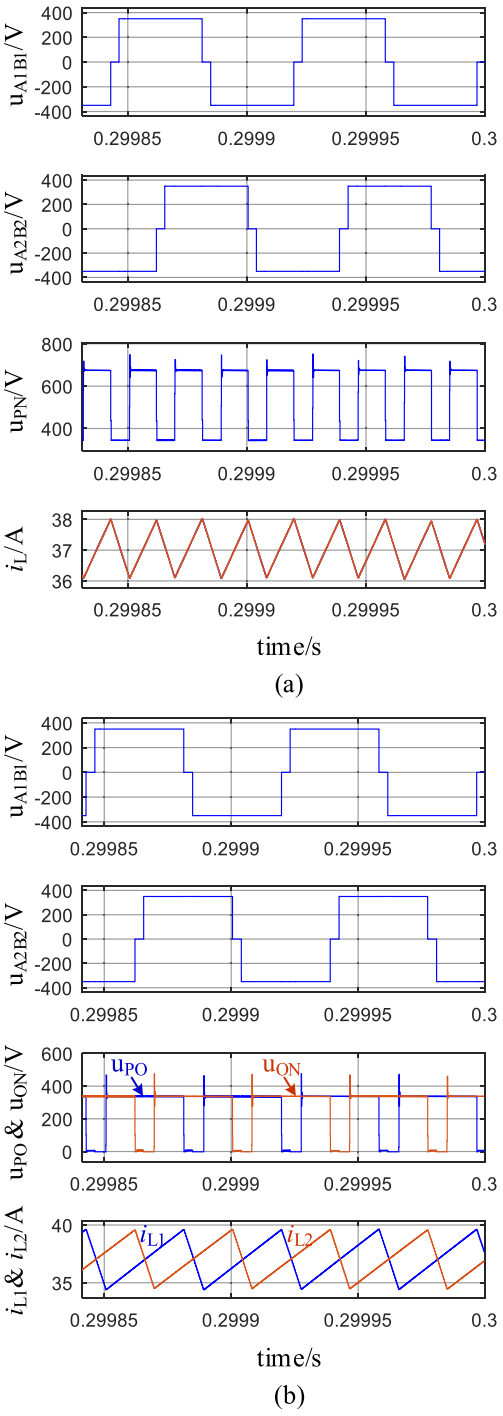

FIGURE 13. Simulation waveforms under $u_{dc} = 350V$, $R = 14.5\ \Omega$ and $D \approx 0.91$ (a) without connection of point O and point M and (b) with connection of point O and point M.

at 0.2s, in this case, a voltage drop about 34V is caused in u_o. Though the initial voltage deviation between u_{o1} and u_{o2} is about 4.5V, it is changed to about 15.5V (it can be roughly evaluated by (24), the inductor average current is about 37A in this case) after the load is added.

To verify the effectiveness of the proposed method, a hardware test circuit is developed. A 32-bit ARM microprocessor with FPU (floating point unit) and 168MHz clock frequency is used to implement the proposed control strategy. Four Infineon IGBT modules (FS150R12KT4) form the topology of the combined converter, and four 2SD106AI modules are used as driver circuits for the IGBTs. The voltage sensors, LV25-PSP2, and current sensors LT108-S7 are used to measure the output voltage and inductor current of the IPOS converter respectively. The nominal values of experimental parameter are the same as that list in Table 2. The corresponding hardware experiment circuit is shown in Fig. 15.

The experiment results are shown in Fig. 16 to Fig. 20. In Fig. 16 (a), the points O and M are connected, in this

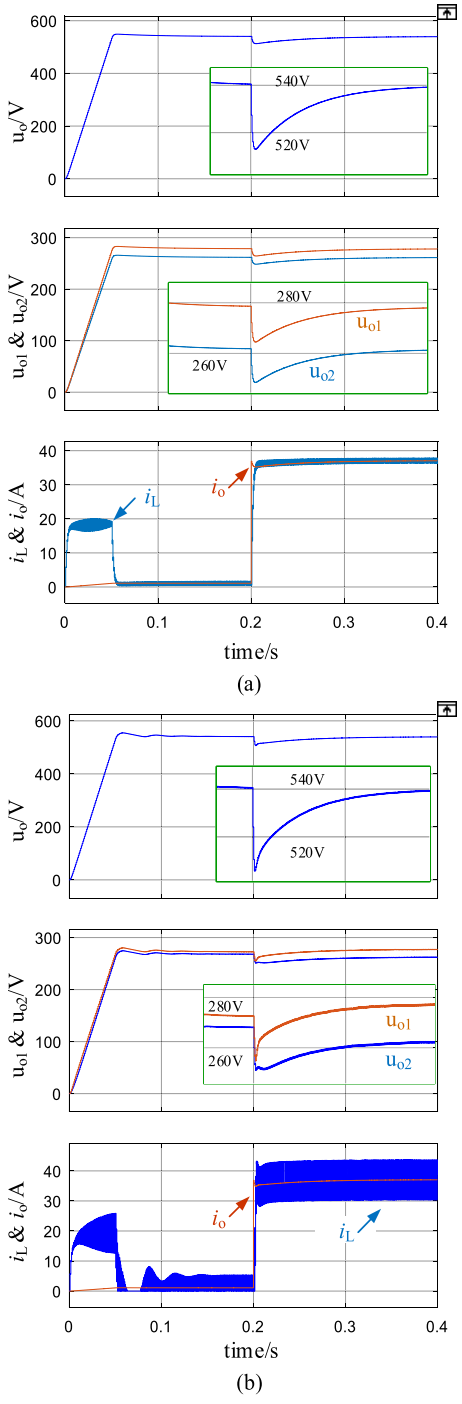

FIGURE 14. Simulation waveforms under sudden load change (a) without connection of point O and point M and (b) with connection of point O and point M.

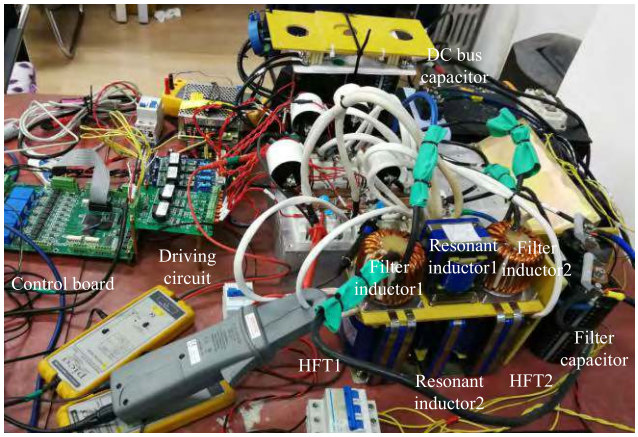

FIGURE 15. Hardware experiment circuit of the three-port converter.

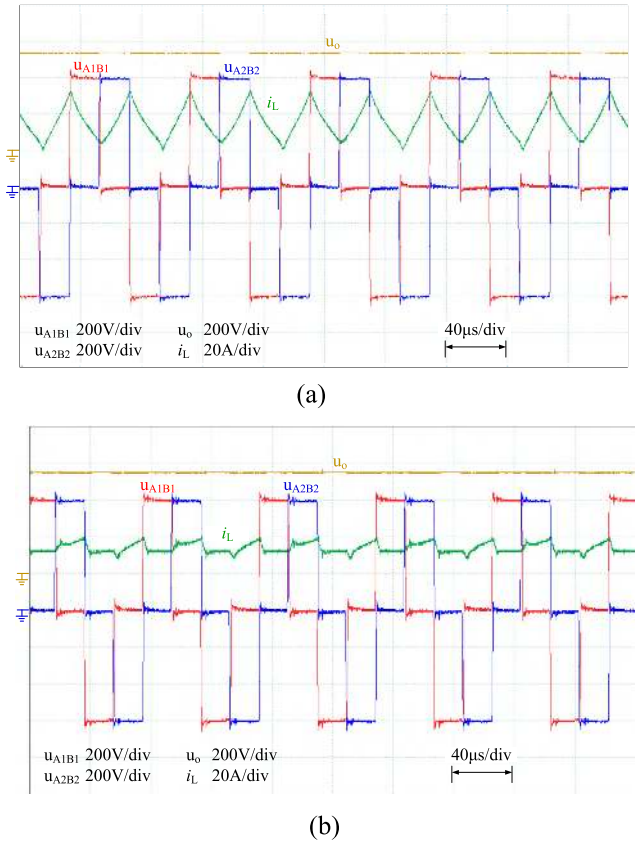

FIGURE 16. Experiment results under u_{dc} = 600V (a) with connection of point O and point M and (b) without connection of point O and point M.

case, the input voltage is 600V, the output voltage is 540V, the load power is about 21 kW (i_o is about 39A). The peak-to-peak value of inductor ripple current is about 31.7A. While if the point O and point M are not connected, the peak-to-peak value of ripple current is decreased to about 11.1A in Fig. 16 (b).

Under the same load condition, Fig. 17 shows the experiment results with u_{dc} = 500V. In Fig. 17 (a), the point O and point M are connected, the peak-to-peak value of inductor ripple current is about 28.1A in this case. When the two points are disconnected in Fig. 17 (b), the peak-to-peak value of ripple current is decreased to about 9.9A. Moreover, when the DC bus voltage is further decreased to 350V in Fig. 18, the peak-to-peak values of the inductor ripple current are about 16.6A in Fig. 18 (a) with connection of point O and point M, and 9.6A in Fig. 18 (b) without connection of point O and point M, respectively. It manifests that the inductor ripple current can be significantly attenuated by

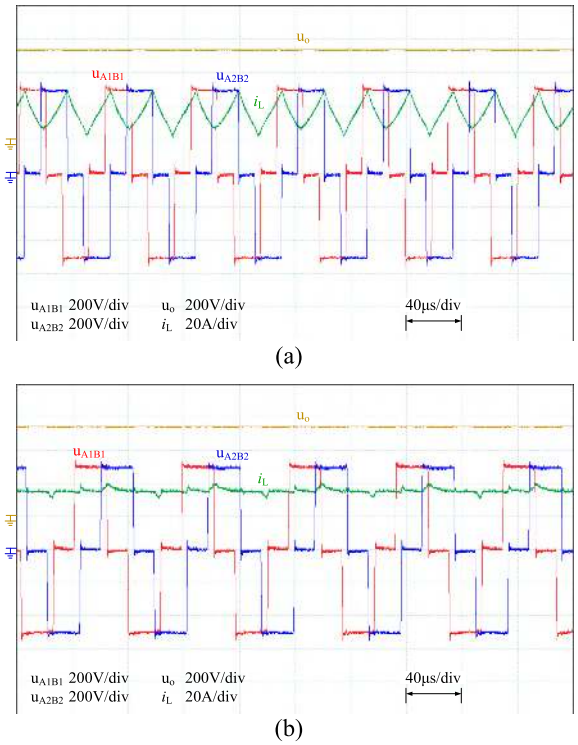

FIGURE 17. Experiment results under $u_{dc} = 500V$ (a) with connection of point O and point M and (b) without connection of point O and point M.

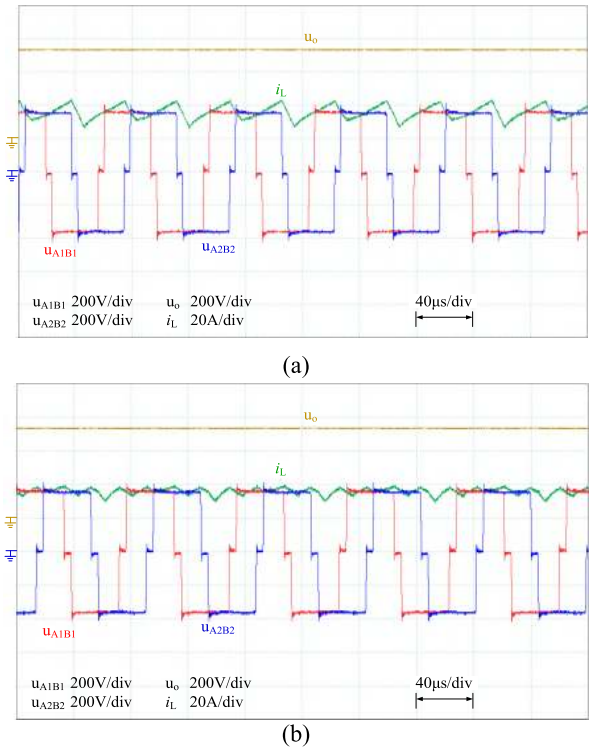

FIGURE 18. Experiment results under $u_{dc} = 350V$ (a) with connection of point O and point M (b) without connection of point O and point M.

disconnecting the point O and point M. The experiment results presented in Fig. 16 to Fig. 18 validate the theoretical analysis in previous sections.

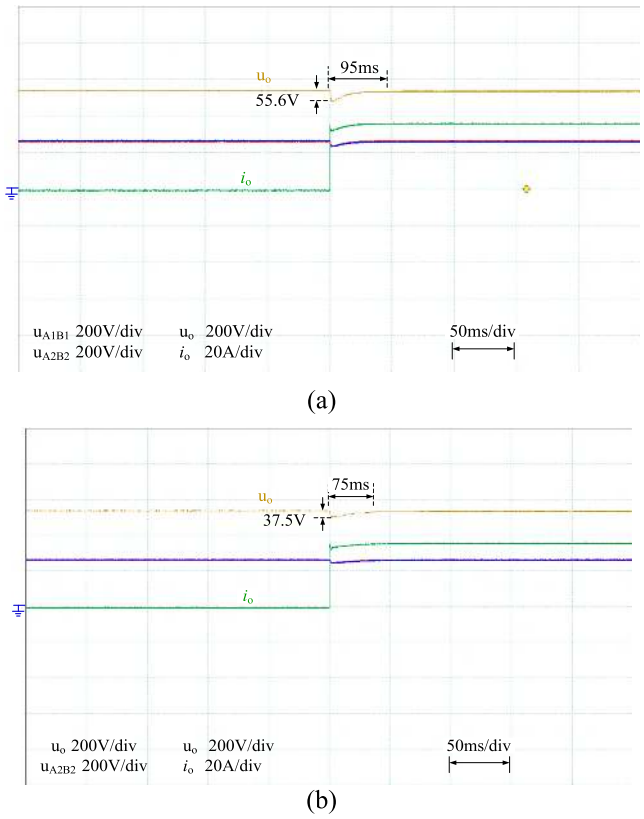

FIGURE 19. Experiment waveforms under 21kW sudden load change and $u_{dc} = 350V$ (a) with connection of point O and point M and (b) without connection of point O and point M.

TABLE 3. Comparison of the inductor ripple current.

Δi_L(A) / u_{dc} (V)	With connection of O and M	Without connection of O and M	PR
600	31.7	11.1	65.0%
500	28.1	9.9	64.8%
350	16.6	9.6	42.2%

The values of the peak-to-peak inductor ripple current with different input voltage, u_{dc} are listed in Table 3 for brief comparison. The symbol PR in the last column of Table 3 means percentage reduction of peak-to-peak inductor ripple current.

Fig. 19 shows the experiment results for dynamic test. In Fig .19 (a), the point O and point M are connected, the input voltage is 350V, the power converter has no load in its initial state, the voltage deviation between u_{o1} and u_{o2} is very small in steady state before load is added. When a 21kW load power is imposed to the power converter suddenly, a voltage undershoot about 55.6V is produced in u_o, and the transient recovery time is about 95ms. In this dynamic process, since the parameter values of the components used in these two modules are very similar (off-the-shelf components and dedicated components are used in the hardware circuit) the dynamic voltage deviation between u_{o1} and u_{o2} is kept very

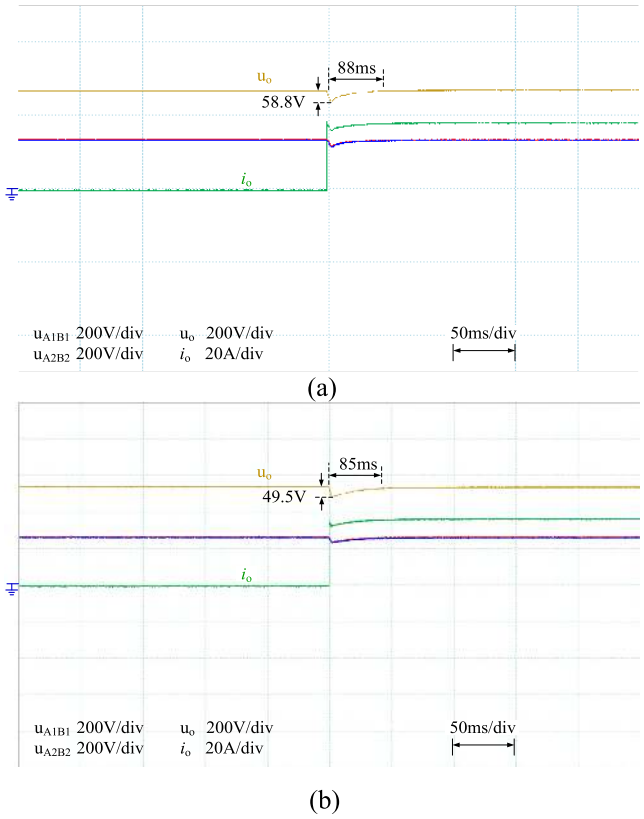

FIGURE 20. Experiment waveforms under 21kW sudden load change and $u_{dc} = 500V$ (a) with connection of point O and point M and (b) without connection of point O and point M.

small too, which is completely acceptable in practices (in the experiment hardware circuit, two electrolytic capacitors are in series, the rated voltage of each capacitor is 450V, therefore, there is sufficient voltage margin to tolerate possible voltage deviation). In Fig. 19 (b), the point O and point M are disconnected, it can be found in this figure that the amplitude of voltage undershoot is about 37.5V when the same load change condition used in Fig. 19 (a) is applied, and the transient recovery time is reduced to about 75 ms in this case.

In Fig. 20, the input voltage, u_{dc} is increased to 500V. As shown in Fig. 19, the same load change condition is also adopted in this test, it can be seen that the voltage deviation between u_{o1} and u_{o2} is still small enough in the steady state and transient state process. The voltage undershoots are about 58.8V and 49.5V with and without connection of point O and point M respectively, and the corresponding transient recovery time are about 88ms and 85ms respectively.

It can be concluded from Fig. 19 and Fig. 20 that the voltage deviation between u_{o1} and u_{o2} in steady state and transient state process can be fully acceptable in practical application using the proposed common phase shifting control scheme, the voltage deviation can be attenuated by dedicated parameters design (or selection) of circuit components (such as HFT, capacitor and inductor etc.) which are available at the current state of the art.

V. CONCLUSION

An input-parallel output-series based combined power converter with modified output filter circuit is proposed in this paper, it has prominent characteristic in decreasing the ripple current of filter inductor which is beneficial to obtain a reduction in the weight and cost of the power converter. A control scheme using the common phase shifting for both of the modules in the input-parallel output-series power converter is developed, the voltage balance performance and comparison studies are presented through small signal based analysis. Though voltage deviation might be produced between the terminal voltages of the output electrolytic capacitors due to parameter deviations of different components, the amplitude of the voltage deviation can be completely acceptable and the capacitor voltage can be constrained in its rated voltage in practical application. Small signal models for dual loop control system design are also deduced for the modified topology. The effectiveness of the developed methods is evaluated through simulation and experimental tests.

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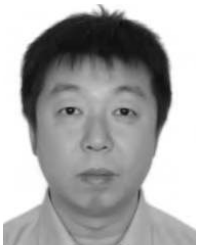
JIANG YOU (M'18) received the Ph.D. degree in control theory and engineering from Harbin Engineering University, China, in 2007. He joined Harbin Engineering University, in 2006, where he is currently an Associate Professor with the Electrical Engineering Department. His research interests include power electronic converters and renewable energy generation.

LIANBIN CHENG was born in Linyi, Shandong, China, in 1993. He received the B.Sc. degree from Harbin Engineering University, in 2016, where he is currently pursuing the M.S. degree with the College of Automation. His research interest includes power converter and control.



BIN FU received the Ph.D. degree in control theory and engineering from Harbin Engineering University, China, in 2006. He joined the College of Automation, Harbin Engineering University, in 2006. He is currently an Associate Professor with the Light Industry Institute, Harbin University of Commerce, China. His research interests include electromechanical control and electronic technique.

MENGLU DENG received the B.S. degree from Harbin Engineering University, Heilongjiang, China, where he is currently pursuing the M.S. degree. His research interests include power converter and AC motor control.