Analysis and Design Considerations of a Load and Line Independent Zero Voltage Switching Full Bridge DC/DC Converter Topology

Praveen K. Jain, *Fellow, IEEE*, Wen Kang, Harry Soin, and Youhao Xi, *Member, IEEE*

***Abstract*—The analysis and design of a zero voltage switching (ZVS) full bridge dc/dc converter topology is presented in this paper. The converter topology presented here employs an asymmetrical auxiliary circuit consisting of a few passive components. With this auxiliary circuit, the full bridge converter can achieve ZVS independent of line and load conditions. The operating principle of the circuit is demonstrated, and the steady state analysis is performed. Based on the analysis, a criterion for optimal design is given. Experiment and simulation on a 350–400 V to 55 V, 500 W prototype converter operated at 100 kHz verify the design and show an overall efficiency of greater than 97% at full load.**

***Index Terms*—DC–DC converter, full bridge converter, soft switching, zero voltage switching.**

I. Introduction

FULL-BRIDGE dc/dc converters are extensively applied in medium to high power dc/dc power conversion. High efficiency, high power density, high reliability and low EMI are some of the most desirable features for these converters, particularly for computer and telecommunication applications.

For power levels up to 3 kW, the full-bridge converters now employ MOSFET switches and use Phase-Shift Modulation (PSM) to regulate the output voltage. In most of these converters, zero voltage switching (ZVS) is achieved by placing a snubber capacitor across each of the switches and either by inserting an inductor in series with the transformer or by inserting an inductor in parallel to the power transformer [1]–[7]. In a practical full-bridge configuration, the snubber capacitor may be the internal drain-to-source capacitor of the MOSFET, the series inductor may be the leakage inductor and the parallel inductor may be the magnetizing inductor of the power transformer. This makes the power circuit of these converters very simple. However, the full-bridge converter with the series inductor loses its ZVS capability at no-load (or light-load), and the converter with the parallel inductor loses its ZVS under short-circuit. The loss of ZVS under these two extreme conditions results in:

1) increased size of heat sink due to switching losses;
2) higher EMI due to high di/dt of the snubber discharging current;
3) reduced reliability due to reverse recovery current of the body diodes.

Moreover, the converter with series inductor reduces the effective duty ratio because of the voltage drop across the series inductor, resulting in higher primary current and larger output inductor.

An alternative full-bridge converter topology to overcome the aforementioned drawbacks has been developed for high power IGBT Full-bridge circuits [6]–[10]. An auxiliary circuit controlled by bidirectional switches is employed at each leg of the full bridge to achieve ZVS of the main switches. For lower power level applications, this topology is rather complicated in both power and control circuitry.

Auxiliary commutated ZVS full bridge converter topologies suitable for low power applications ($\leq$3 kW) have been reported [11]–[13]. In these converter topologies an auxiliary circuit comprising of an inductor at each leg of the bridge is employed. The proposed topologies provide ZVS of all the switches under all operating conditions including open and short circuits making them very attractive for telecommunication applications where two extreme load conditions are often present (e.g., rectifiers for central power plants). Although, these converter topologies have been described in details, in-depth circuit analysis and performance characteristics are not given for the detailed design of the converters.

In this paper, steady-state analysis of such a converter topology is performed to provide design guidelines. Trade-off in selecting the auxiliary circuit components is given to optimize the performance of the overall converter. Detailed simulation of the converter is presented to verify the analysis and to demonstrate the key features. A prototype of 500 W, 300–400 V dc to 55 V dc converter operating at 100 kHz is built and the experimental results show an overall efficiency of greater than 97% at full load and over the entire input voltage range.

II. Description of Circuit

Fig. 1 shows the proposed ZVS full bridge converter topology. It consists of two functional sub-circuits. One subcircuit is the conventional PSM full bridge converter, which is referred to as the power circuit hereafter. The other is an auxiliary network shown in the shaded area in Fig. 1.

The power circuit employs the following devices: (i) S_1, S_2, S_3, and S_4, four MOSFET switches, (ii) T_r, the power transformer with a turns ratio of k, (iii) D_1 and D_2, two rectifier diodes, (iv) L_o & L_o, the output filter, and (v) R_o, the load.

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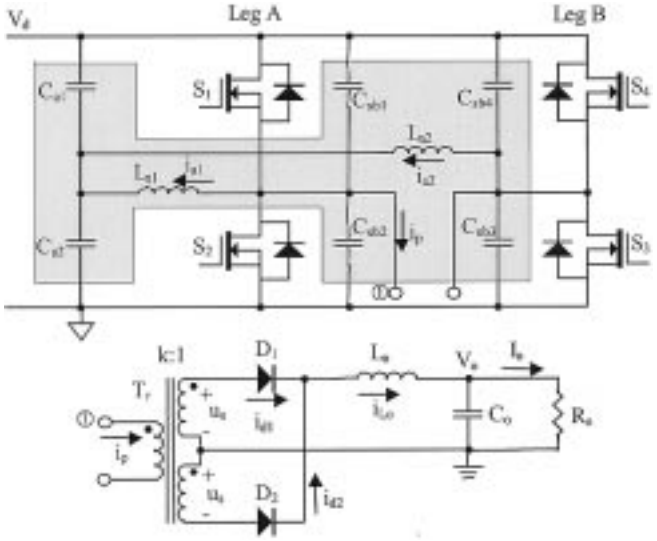

Fig. 1. The proposed ZVS full bridge converter.

The auxiliary circuit is comprised by eight passive devices, i.e., (i) C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}, four drain-to-source snubber capacitors, each connected across one switch, (ii) C_{a1} and C_{a2}, a capacitor voltage divider, and (iii) L_{a1} and L_{a2}, two auxiliary inductors.

PSM is used as the control technique for output regulation in the proposed converter topology. In terms of power transfer from the input to load, the power circuit operates in exactly the same way as does a conventional phase-shift full bridge converter, and the auxiliary circuit hardly interferes with this power transfer. However, the auxiliary circuit does have significant influences on the switching transients of the switches: it removes the switching losses from all the switches, at both turn-on and turn-off.

III. Steady State Analysis

Since conventional PSM full bridge converters have been extensively discussed in the literature, its operation will not be addressed in detail in this paper. Only the operation of the auxiliary circuit is analyzed below. To perform the steady state analysis, the following assumptions are made.

i) The steady state conditions have been established and the converter is operating in the continuous conduction mode (CCM), and producing the nominal output voltage V_o and delivering the power P_o to a constant output load. The input dc voltage V_d is ripple free.

ii) The gating of switches on Leg A, namely S_1 and S_2, is leading the gating of switches on Leg B, or S_3 and S_4, by a phase shifted angle θ (expressed as a fraction of a switching period), and θ is determined by the control circuit to regulate the output voltage.

iii) The switching frequency is f_s.

iv) All components and devices have ideal properties and characteristics.

v) There is a very short dead time, t_d, between the ON states of the two switches on each leg of the bridge.

vi) C_{sb1} and C_{sb2} have equal capacitance values, and so do C_{sb3} and C_{sb4}.

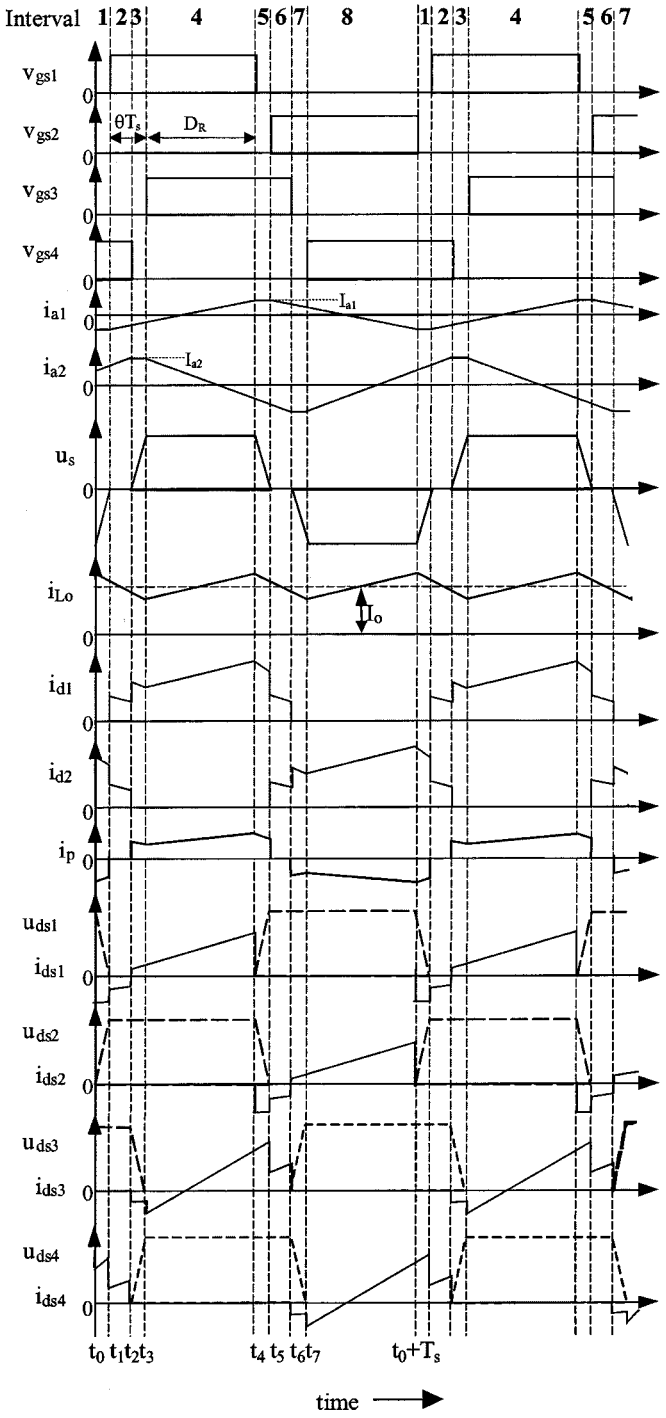

Fig. 2. Key waveforms of the proposed converter topology. The dead time and switching transient are exaggerated.

vii) C_{a1} and C_{a2} have equal capacitance value, and they are large enough to establish a constant and ripple free voltage during the steady state operation.

With these assumptions, the operating principle is illustrated with key waveforms in Fig. 2. Each switching cycle can be divided into eight intervals. For convenience, the following constants are defined.

For the power circuit, the steady state current flowing through the output inductor has the saw-tooth waveform biased by the output dc current I_o. Currents I_{Lopeak} and I_{Lovalley} are the peak

and valley values of this saw-tooth shaped current, respectively, which are given below

$$I_{\text{Lopeak}} = \frac{(V_d - kV_o)V_o}{4f_s V_d L_o} + I_o \tag{1}$$

$$I_{\text{Lovalley}} = -\frac{(V_d - kV_o)V_o}{4f_s V_d L_o} + I_o. \tag{2}$$

For the auxiliary circuit, as the two switches on each leg are switched alternately and symmetrically with little dead time in between, the auxiliary inductors L_{a1} and L_{a2} each see alternating positive and negative voltage for equal intervals. Then the steady state currents through L_{a1} and L_{a2} have a triangle waveform. The peak values of current I_{a1} and I_{a2} through L_{a1} and L_{a2} respectively are given as follows

$$I_{a1} = \frac{V_d}{4L_{a1}}\left(\frac{T_s}{2} - t_d\right) \tag{3}$$

$$I_{a2} = \frac{V_d}{4L_{a2}}\left(\frac{T_s}{2} - t_d\right). \tag{4}$$

A. Interval 1 ($t_0 \le t < t_1$)

In the last interval of the previous cycle, both S_2 and S_4 were ON while both S_1 and S_3 OFF. The primary winding of T_r saw a constant voltage, $-V_d$, and D_{o1} was reverse biased and D_{o2} forward biased. Thus the output inductor current was reflected to the primary side via D_{o2} and T_r. The drain current of S_2 was the sum of the reflected load current and the auxiliary inductor current I_{a1}, and it reached its peak value at the end of last cycle.

At the beginning of this interval, S_2 is turned off, and no other switching action takes place during this interval. The duration of this interval is the dead time t_d.

As S_2 is OFF, the said peak current starts to charge C_{sb2}, and at the same time it discharges C_{sb1}. The drain-to-source voltages of both switches on Leg A are thus governed, respectively, by the following:

$$u_{ds1}(t) = V_d - \frac{I_{a1} + \frac{I_{\text{Lopeak}}}{k}}{2C_{sb1}}(t - t_0) \tag{5}$$

$$u_{ds2}(t) = \frac{I_{a1} + \frac{I_{\text{Lopeak}}}{k}}{2C_{sb2}}(t - t_0). \tag{6}$$

Owing to C_{sb2}, u_{ds2} can only rise slowly, providing the ZVS condition for S_2 to turn off. Meanwhile, C_{sb1} is discharged within this interval. As soon as C_{sb1} is completely discharged, the body diode of S_1 latches in, giving a path for the auxiliary inductor current to flow. This clamps u_{ds1} at zero in the rest of this interval, providing the ZVS condition for S_1 to turn on.

Because S_4 is still ON, the primary winding of T_r will see a zero voltage after u_{ds1} is clamped at zero. Then, both D_{o1} and D_{o2}share the output inductor current in the freewheeling mode, and this stops the primary current i_p. Now, the primary circuit only sees i_{a1} and i_{a2}. Specifically, the current that flows through S_4 only consists of i_{a2} and that is determined by

$$i_{a2}(t) = \frac{V_d}{2L_{a2}}\left(t - t_0 - \frac{\theta}{f_s}\right) + I_{a2}. \tag{7}$$

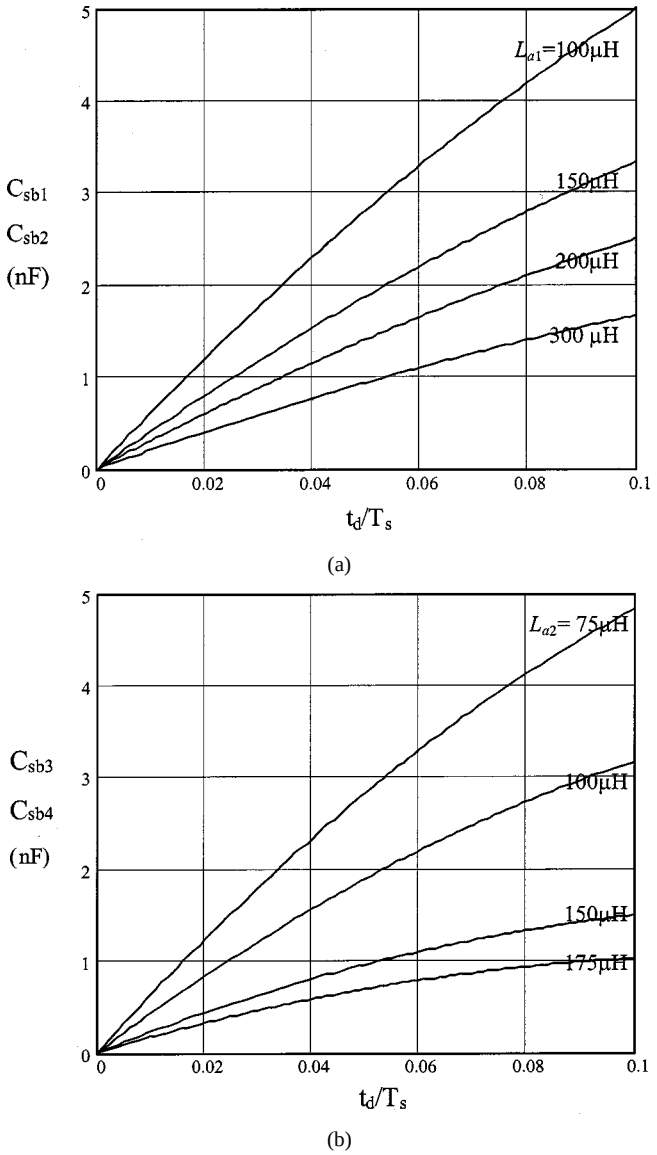

Fig. 3. Example design curves for selecting the auxiliary inductors and the permitted maximum snubber capacitors: (a) C_{sb1} and C_{sb2} vs. t_d and L_{a1} and (b) C_{sb3} and C_{sb4} versus t_d and L_{a2}. $f_s = 100$ kHz, $V_d = 350$–400 V, $V_o = 55$ V, $k = 5.5{:}1$, $L_o = 20$ μH, and full load at 500 W.

B. Interval 2 ($t_1 \le t < t_2$)

At the beginning of this interval, S_1 is turned on under ZVS condition. No other switching action takes place during this interval. The duration of this interval is determined by the phase shift angle that is required to regulate the output voltage.

Now L_{a1} sees a constant positive voltage established by C_{a1}, i_{a1} starts to increase linearly from its negative peak, as governed by

$$i_{a1}(t) = \frac{V_d}{2L_{a1}}(t - t_1) - I_{a1}. \tag{8}$$

Because both S_1 and S_4 are ON, the primary winding of T_r still sees zero voltage. Thus, both output rectifier diodes are forward biased to freewheel the output inductor current, and no current flows through the primary winding. The current i_{a2} flowing through S_4 is still determined by (7).

C. Interval 3 ($t_2 \le t < t_3$)

At the beginning of this interval, S_4 is turned off in ZVS. No other switching action takes place during this interval. The duration of this interval is the dead time t_d.

When S_4 is off, i_{a2} reaches its positive peak value I_{a2}. Similar to Interval 1, this current starts to charge C_{sb4} and discharge C_{sb3}. Thus u_{sb4} starts to rise from zero while u_{sb3} starts to decrease from V_d.

As soon as u_{sb3} decreases T_r starts to see a positive voltage because S_1 is already ON. Thus D_{o1} is forward biased and D_{o2} is reverse biased. The total output inductor current, that is at its valley value now, starts to flow through D_{o1}, forcing a primary current to flow. Therefore the current flowing out of Leg B is i_{a2} minus the reflected output inductor current.

As this interval is very short, i_{a2} is almost constant at its peak value I_{a2}. So is the output inductor current at its valley value. Similar to Interval 1, it is found that

$$u_{ds3}(t) = V_d - \frac{I_{a2} - \frac{I_{\text{Lovalley}}}{k}}{2C_{sb3}}(t - t_2) \tag{9}$$

$$u_{ds4}(t) = \frac{I_{a2} - \frac{I_{\text{Lovalley}}}{k}}{2C_{sb4}}(t - t_2). \tag{10}$$

It is seen that, owing to C_{sb4}, u_{sb4} can only rise slowly, providing the ZVS condition for S_4 to turn off. The gradual discharging of C_{sb3} brings down u_{sb3} to zero within this interval, providing the ZVS condition for S_3 to turn on.

During this interval, the Leg B current is equal to i_{a2} minus the reflected load current i_p. This relieves the current stress of S_4 at turn-off, but it also reduces the effective current to discharge the snubber capacitor of S_3. In order to achieve a ZVS turn-on of S_3, C_{sb3} must be completely discharged within the dead time t_d. This requires I_{a2} to be greater than the reflected load current i_p. Otherwise, C_{sb3} would not be completely discharged due to the insufficient magnitude of the effective discharging current, and S_3 would lose ZVS. This shows the opposite effects of the load current on two legs during the switching transients.

D. Interval 4 ($t_3 \le t < t_4$)

At the beginning of this interval, S_3 is turned on under ZVS condition. No other switching action takes place during this interval. The duration of this interval is determined by effective duty ratio required to regulate the output voltage.

As S_3 is ON, L_{a2} sees a constant negative voltage established by C_{a2}. Current i_{a2} starts to decrease linearly, as given by

$$i_{a2}(t) = -\frac{V_d}{2L_{a2}}(t - t_3) + I_{a2}. \tag{11}$$

During this interval, the drain currents of S_1 and S_3 are determined, respectively, by

$$i_{ds1}(t) = \frac{V_d}{2L_{a1}}(t - t_1) - I_{a1} + \frac{1}{k}\left[\frac{V_d - kV_o}{kL_o}(t - t_2) + I_o - \frac{(V_d - kV_o)V_o}{4f_sL_oV_d}\right] \tag{12}$$

$$i_{ds3}(t) = \frac{V_d}{2L_{a2}}(t - t_3) - I_{a2} + \frac{1}{k}\left[\frac{V_d - kV_o}{kL_o}(t - t_2) + I_o - \frac{(V_d - kV_o)V_o}{4f_sL_oV_d}\right]. \tag{13}$$

E. Intervals 5 Through 8

The analysis of the circuit in the last four intervals of this switching cycle is similar to the first four intervals, except for the opposite switching activities on the switches.

After Interval 8, another switching cycle begins and the converter repeats the process from Intervals 1 through 8.

IV. Derivation of Asymmetrical Auxiliary Circuit

It is understood that the auxiliary inductors are required in the proposed topology to achieve ZVS at turn-on by providing the necessary current to discharge the snubber capacitors. However, the auxiliary circuit currents flow through the switches and this results in additional conduction losses. Reducing this type of conduction losses will optimize the overall performance of the proposed topology. This can be achieved by using an asymmetrical auxiliary circuit arrangement.

To successfully discharge the snubber capacitors of the switches of Leg A within the dead time period t_d, the required discharging current shall satisfy

$$I_{A\_\text{discharge}} \ge \frac{C_{sb1,2}V_d}{t_d}. \tag{14}$$

Similarly for Leg B it shall satisfy

$$I_{B\_\text{discharge}} \ge \frac{C_{sb3,4}V_d}{t_d}. \tag{15}$$

On the other hand, the magnitude of the discharging current for snubber capacitors on Leg A is given by

$$I_{A\_\text{discharge}} = \frac{V_d}{8L_{a1}}\left(\frac{1}{2f_s} - t_d\right) + \frac{1}{2k}\left[\frac{(V_d - kV_o)V_o}{4f_sV_dL_o} + I_o\right] \tag{16}$$

and for the switches on Leg B, it is given by

$$I_{B\_\text{discharge}} = \frac{V_d}{8L_{a2}}\left(\frac{1}{2f_s} - t_d\right) - \frac{1}{2k}\left[I_o - \frac{(V_d - kV_o)V_o}{4f_sV_dL_o}\right]. \tag{17}$$

Equations (16) and (17) indicate that the load current assists the auxiliary current i_{a1} in the process to discharge the snubber capacitors of Leg A, while it counteracts the auxiliary current i_{a2} in the discharging of the snubber capacitors on Leg B.

In practice, all the snubber capacitors can be selected the same as it reduces the number of parts in the inventory and therefore the purchasing costs. Then, as seen from (14) and (15), all the snubber capacitors require the same magnitude of current to discharge and charge them completely for successful ZVS at turn-on and turn-off respectively. Therefore, from (16) and (17), the value of L_{a1} can be selected higher than the value of L_{a2} in order to reduce the conduction losses. This leads to the asymmetry of the auxiliary circuit.

If increasing L_{a1} is not preferable in some design because a larger L_{a1} increases the overall size and weight of the converter, L_{a1} and L_{a2} can be selected the same. Then at turn-off, the switches on Leg A see higher current stress than those on Leg B. Thus, to achieve successful ZVS turn-off, the switches on Leg A require larger snubber capacitors than those of Leg B do. This supports the arguments of adopting an asymmetrical auxiliary circuit from another point of view.

TABLE I
PRINCIPAL PARAMETERS OF THE EXAMPLE CIRCUIT

parameter	value	parameter	value/device
V_{dmin}/V_{dmax}	350 V/400 V	C_{a1}, C_{a2}	1 μF, each
V_o/I_o	55 V /10 A	C_{sb1}, C_{sb2} C_{sb3} and C_{sb4}	1 nF, each
k	5.5:1	L_{a1}/L_{a2}	200 μH/100 μH
L_o/C_o	20 μH/5000 μF	S_1, S_2, S_3, S_4	IRFP460
t_d	400 ns	D_{o1}, D_{o2}	MUR3020

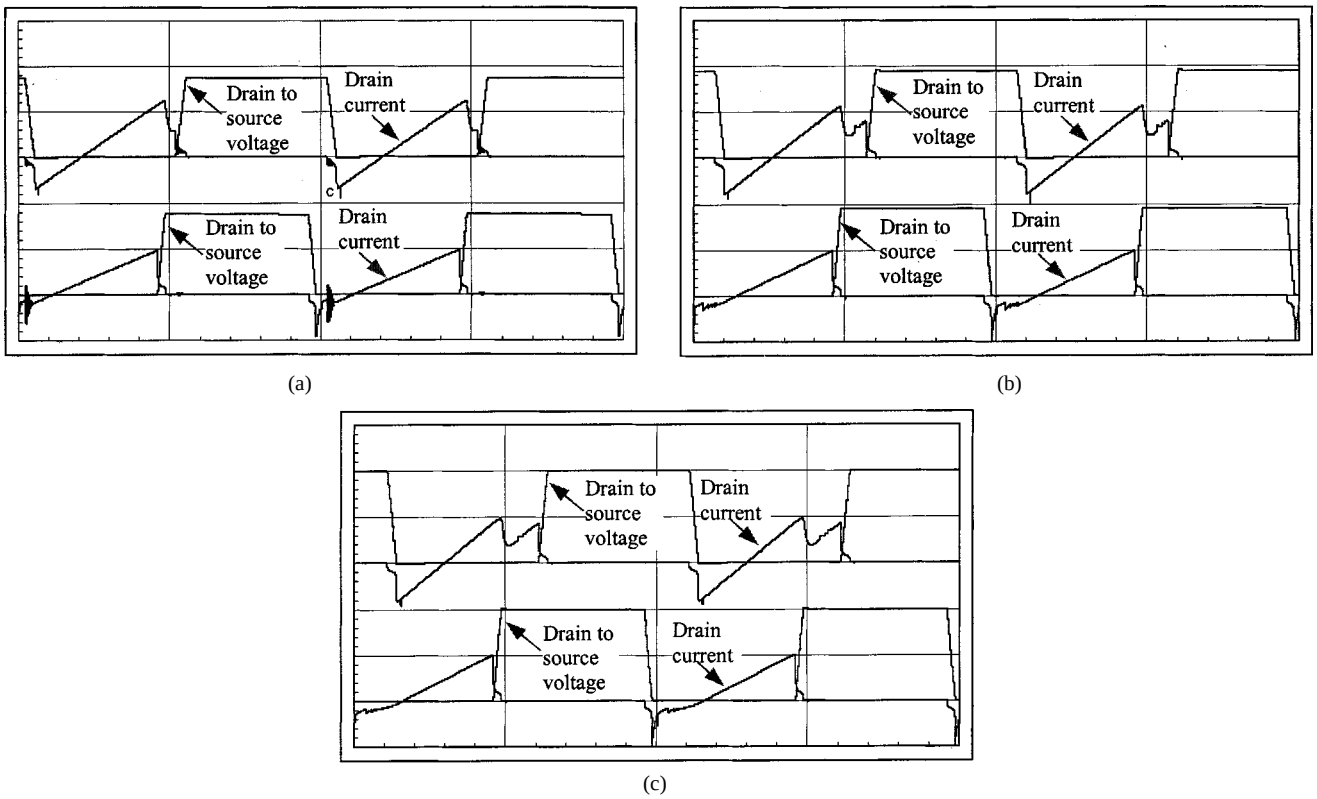

Fig. 4. Simulation results of the current and voltage waveforms of switches on both legs of the bridge at full load condition. $P_o = 500$ W: (a) at low line, $V_d = 350$ V, (b) at medium line, $V_d = 380$ V, and (c) at high line, $V_d = 400$ V. Top traces are the waveforms of the switch on Leg B. Bottom traces are the waveforms of the switch on Leg A Scale: voltage-200 V/div., current-5 A/div. time-5 μs/div.

V. DESIGN PROCESS

The power circuit will not be discussed as it has been extensively addressed in the literature, therefore, only the design of auxiliary circuit will be presented here. The following parameters are assumed known:

i) the design of the power circuit, namely L_{omax}, C_o, k, etc.;
ii) I_o, full load current;
iii) $V_{d\max}$ and $V_{d\min}$, input dc voltage range;
iv) V_o, nominal output voltage;
v) f_s, switching frequency;
vi) $D_{\max}$, maximum duty ratio;
vii) t_d, switching dead time.

A. Selection of L_{a1}, L_{a2}, C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}

To achieve ZVS turn-on, the snubber capacitors shall be completely discharged within the dead time period t_d, under all operating conditions. Because the auxiliary inductors determine the values of the discharging currents, and the required discharging currents are determined by snubber capacitors, the selection of the auxiliary inductors and the snubber capacitors are correlated.

As seen from (16) and (17), to guarantee the complete discharge of the snubber capacitors for Leg A under all line and load conditions, the following equation shall be satisfied

$$C_{sb1} = C_{sb2} \le \frac{t_d}{8L_{a1}}\left(\frac{1}{2f_s} - t_d\right). \tag{18}$$

As mentioned previously, the load current assists the auxiliary current to discharge snubber capacitors on Leg A. When (18) is satisfied, the Leg A snubbers can be completely discharged even under no load condition, not to mention under full load. It is also seen that ZVS on Leg A is inherently independent of the input voltage.

For Leg B, the following equation must be satisfied

$$C_{sb3} = C_{sb4} \le \frac{t_d}{8L_{a2}}\left(\frac{1}{2f_s} - t_d\right) - \frac{t_d}{2kV_{d\min}}\left(I_{omax} - \frac{V_{d\min} - kV_o}{4V_{d\min}f_sL_o}V_o\right). \tag{19}$$

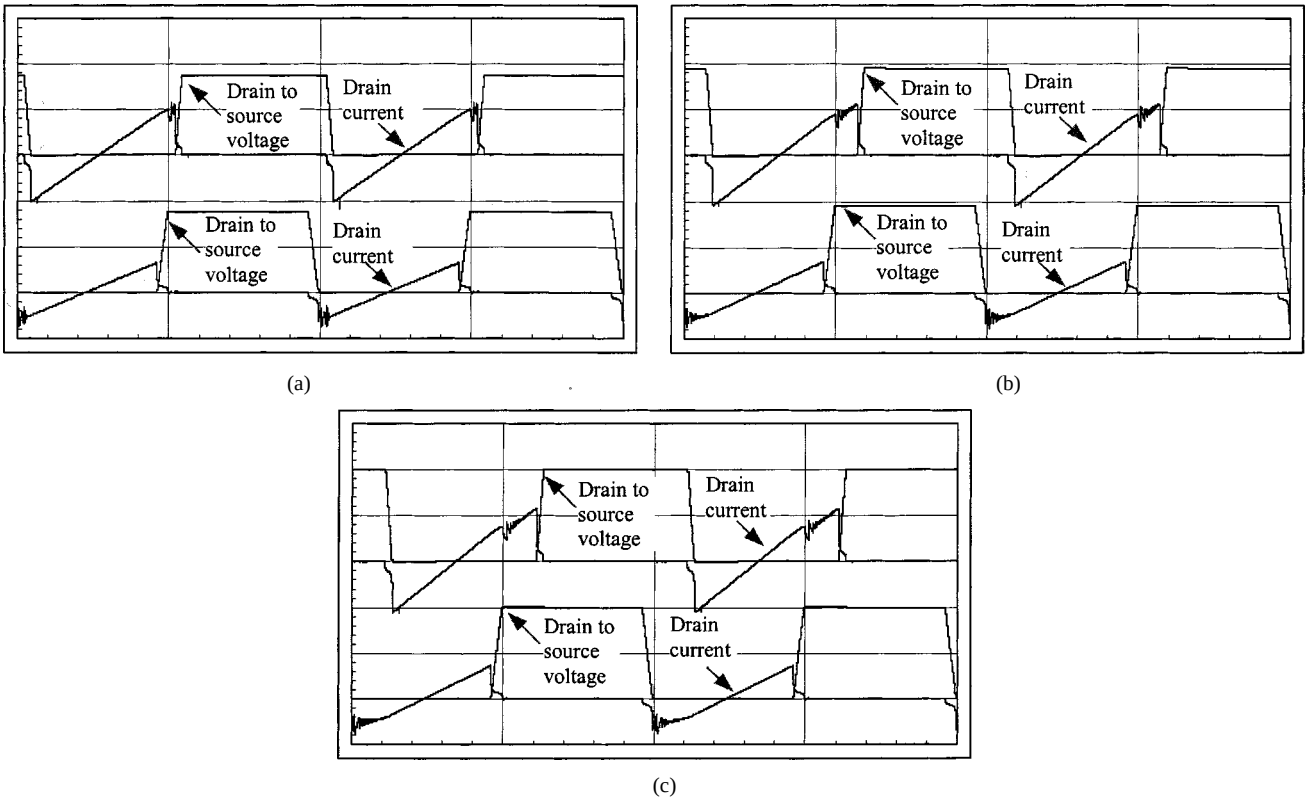

Fig. 5. Simulation results of the current and voltage waveforms of switches on both legs of the bridge at light load condition. $P_o = 50$ W (10% of the full load). (a) At low line, $V_d = 350$ V. (b) At medium line, $V_d = 380$ V. (c) At high line, $V_d = 400$ V. Top traces are the waveforms of the switch on Leg B. Bottom traces are the waveforms of the switch on Leg A Scale: voltage-200 V/div., current-5 A/div. time-5 μs/div.

It is seen that the load current counteracts the auxiliary current to discharge the snubbers on Leg B. As (19) is satisfied at the minimum input voltage and full load which is the worst case, the snubber will be discharged under all other operating conditions. In this way ZVS for Leg B will also become independent of line and load conditions.

Fig. 3. shows an example of the selection curves of the snubber capacitors as functions of t_d and the auxiliary inductors. It is seen that for a dead time of 400 ns when all the snubbers are selected to be 1 nF, the auxiliary inductor for Leg A or the leading leg, shall be about 200 μH, while that for the lagging leg (Leg B) shall be 100 μH.

B. Selection of C_{a1}, C_{a2}, the Capacitor Type Voltage Divider

The two capacitors are employed to establish and hold almost dc voltages with little ripples for the proper operation of the auxiliary circuit. Assume the permitted ripple voltage on these two capacitors is about 2% of the input line voltage, then their approximate values are given by

$$\frac{2}{100}\cdot\frac{C_{a1}+C_{a2}}{2}V_d \geq \frac{1}{2}\left|I_{a2}-I_{a1}\right|\frac{T_s}{2}. \qquad (20)$$

Substituting (2-7) and (2-8) into (20), and considering $C_{a1} = C_{a2}$, then (20) yields:

$$C_{a1} = C_{a2} \geq \frac{100}{2}\cdot\frac{|L_{a1}-L_{a2}|}{32f_s^2 L_{a1}L_{a2}}. \qquad (21)$$

In the example, these two capacitors shall be greater than 0.8 μF, therefore, 1 μF capacitors are selected.

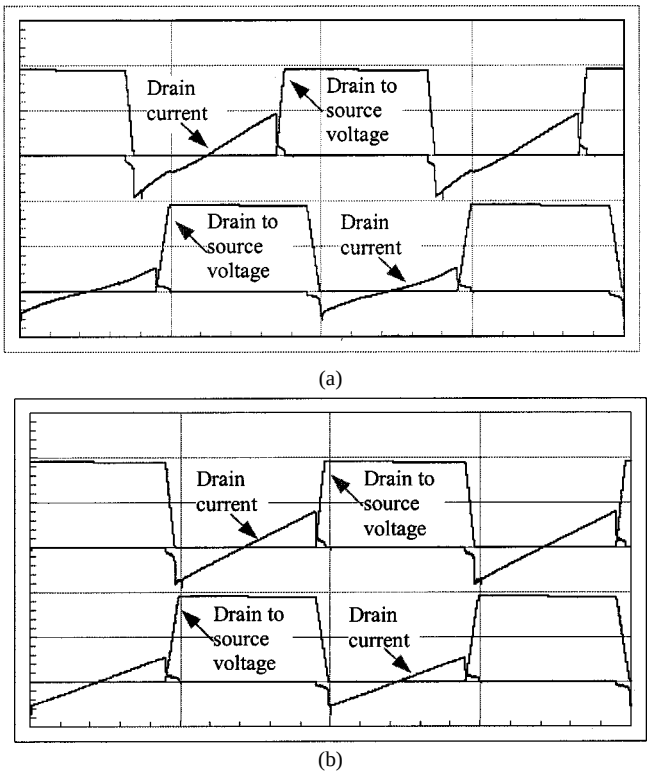

Fig. 6. Simulation results of the current and voltage waveforms of switches on both legs under extreme operating conditions. (a) Under open circuit condition, $V_d = 380$ V, $P_o = 0$ W. (b) under short circuit condition, $V_d = 380$ V. Top traces are the waveforms of the switch on Leg B. Bottom traces are the waveforms of the switch on Leg A Scale: voltage-200 V/div., current-5 A/div. time-5 μs/div.

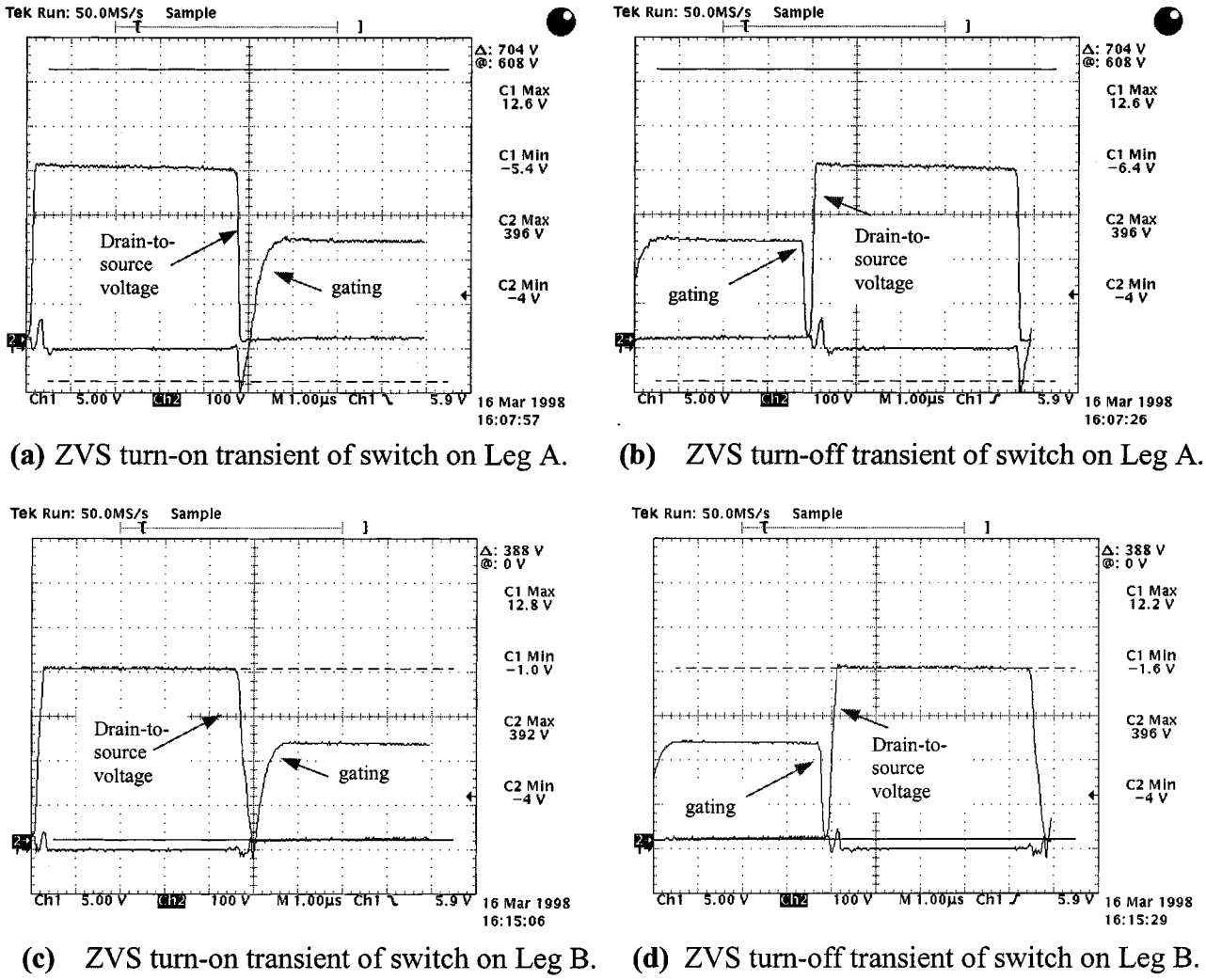

Fig. 7. Experimental results under full load condition. $f_s = 128$ kHz, $V_o = 55$ V, $P_o = 500$ W, $V_d = 390$ V.

C. A Design Example

According to the design criteria given above, the prototype circuit is designed. The principal parameters and selected devices are listed in Table I.

VI. Simulation Results

Simulation of the proposed converter topology is performed by using Pspice software. The principal parameters of Table I are used in the simulation. It should be pointed out that the drain-to-source voltage and current of the two switches of one leg have exactly the same waveforms, although they are out of phase. Therefore, only the waveforms of S_1 and S_3 are displayed below.

Fig. 4 shows the voltage and current waveforms of the switches at full load but different input voltages. It is seen that ZVS on each switch is achieved at both turn-on and turn-off under all these conditions.

A switching spike on the drain current waveform of the switch on Leg A is observed in Fig. 4(a). It is because, the switching of the switches on Leg B moves the voltage across the primary winding of T_r out of the clamping mode. This will reverse bias one of the two freewheeling output rectifier diodes. Consequently, the reverse recovery of the diode give rise to the spike, and this spike is reflected back into the primary side and appears in the drain current of the switches. In a practical circuit, a snubber might be added to each of the two rectifier diodes to reduce and/or eliminate the spike. Alternatively, Schottky diodes can be used for low output applications.

Fig. 5 shows the voltage and current waveforms of the switches under 10% of the rated load and different input voltage. It is seen that ZVS is also achieved on each switch at both turn-on and turn-off under all these conditions.

Fig. 6 shows the voltage and current waveforms of the switches under extreme operating conditions, i.e., open circuit and short circuit. It can be concluded that ZVS is still achieved under these extreme conditions.

In summary, as seen from Figs. 4–6, ZVS at turn-on and turn-off on each switch is achieved independent of line and load conditions.

VII. Experimental Results

A prototype of 500 W, 300–400 V dc to 55 V dc converter operating at 100 kHz was built to verify the performance of the proposed topology. The principal parameters of this prototype are given in Table I.

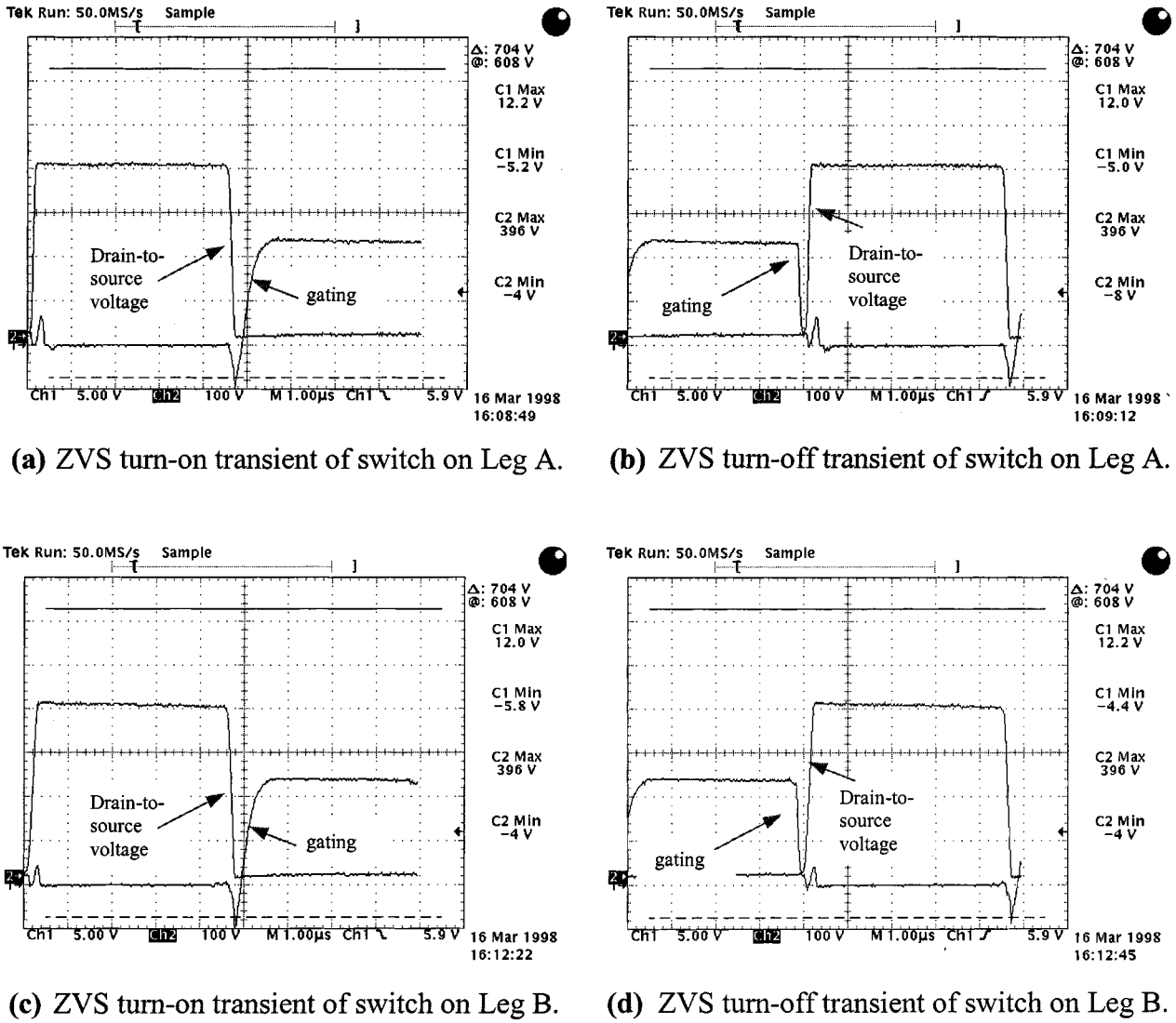

Fig. 8. Experimental results under light load condition. $f_s = 128$ kHz, $V_o = 55$ V, $P_o = 50$ W, $V_d = 390$ V (to be continued).

In the prototype circuit, an ETD44 core is used for the power transformer, and an air gapped RM42819 core is used for each of the two auxiliary inductors. The size ratio of each auxiliary inductor to the power transformer is about 1/4 in this 500 W prototype, and this makes the proposed topology seemingly less advantageous. However, for higher power level up to 3 kW, the power transformer significantly increases the size but the auxiliary inductor can almost use the same core with a larger air gap. It is because lower inductance is required such that higher auxiliary current can be produced to achieve ZVS in a higher power level. Therefore, for higher power level applications the size ratio will become much lower. On the other hand, because ZVS is now achieved independent of line and load conditions, the power switches require much smaller heat sinks and this leaves room for the auxiliary inductors such that the overall size of the converter may not increase.

Fig. 7 shows the gating signal and the drain-to-source voltage of switches on both legs of the bridge, under full load and variable input conditions. The waveforms of only one switch from each leg are shown. The other switch has the same waveform with a 180° phase shift. The drain current is not shown here for the reason that measuring the current requires a long loop of wire to be inserted into the circuit and it will interfere with the normal operation. It can be concluded from Fig. 7 that each switch has ZVS at both turn-on and turn-off under all those conditions, because the gating signal comes after the drain to source voltage completely drops to zero, and it is withdrawn completely before the latter rises from zero.

Fig. 8 shows the gating signal and the drain to source voltage of switches on both legs of the bridge under 10% of the rated load and different input voltage. Similarly, it can be concluded that ZVS is achieved on each switch under all those conditions.

Fig. 9 shows the overall efficiency as a function of output power. It is seen that, the efficiency is almost constant $(>97\%)$ over the output load range from 50% to 100%. The efficiency, however, deceases gradually below this load range due to the load independent conduction losses caused by the auxiliary circuit.

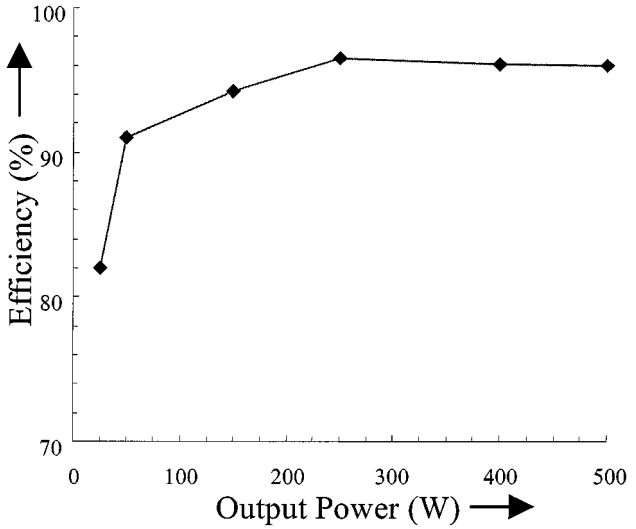

Fig. 9. Overall efficiency as a function of output power. Operating conditions $f_s = 128$ kHz, $V_o = 55$ V, and $V_d = 390$ V.

VIII. Conclusions

The ZVS full bridge dc/dc converter topology presented in this paper is simple both in the power circuit and control. The auxiliary circuit only employs passive components, and the proposed converter topology can achieve ZVS under all line and load conditions. Asymmetry in the auxiliary circuit optimizes the overall performance. It has an overall efficiency higher than 97% at full load and over the entire input voltage range. The proposed converter topology is very attractive for the power levels up to 3 kW applications.

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