Analysis and design of a 60GHz wideband voltage-voltage transformer feedback LNA

Analysis and Design of a 60 GHz Wideband Voltage-Voltage Transformer Feedback LNA

Pooyan Sakian, Erwin Janssen, Arthur H. M. van Roermund, *Senior Member, IEEE*, and Reza Mahmoudi

***Abstract*—To cope with the problem of instability and imperfect reverse isolation, a millimeter-wave voltage-voltage transformer feedback low noise amplifier has been analyzed, designed, and measured in CMOS 65 nm technology. Analytical formulae are derived for describing the stability, gain, and noise in this circuit topology. An analogy with the classic concept of Masons's invariant is used to illustrate how the transformer feedback provides the required reverse isolation in the LNA. Based on the developed theoretical analysis, the circuit is implemented as a fully integrated 60 GHz two-stage differential low noise amplifier in 65 nm CMOS technology. A flat gain of 10 dB is achieved over the entire 6 GHz bandwidth. The measured noise figure is 3.8 dB.**

***Index Terms*—Low-noise amplifier, millimeter wave, receiver, transformer, wideband.**

I. Introduction

THE 7 GHz unlicensed bandwidth around 60 GHz provides new possibilities for realization of short-range high-data-rate communication links. Modern CMOS technology is a promising candidate for implementing the required hardware due to its potential of integration of digital baseband with the RF front end.

As the first stage of the receiver frontend after the signal source or the antenna, the LNA is responsible for amplification of the signal from the antenna with minimum added noise and distortion. Therefore, noise figure, gain, and linearity are among the main design concerns. Many of the conventional topologies of the LNA, such as those based on the common-source topology, suffer from stability problems, particularly at high frequencies as a result of the pronounced impact of the Miller capacitance. Various solutions have been proposed and implemented for addressing the stability problems, which mainly focus on providing reverse isolation between the input and the output. Voltage-voltage transformer feedback (VVTF) technique is one of these methods and has been successfully used at lower frequencies [8]. The applicability of this technique to mm-wave regime has been verified in [7]. This paper deals with the analysis and implementation of a voltage-voltage transformer feedback technique, as a method of providing reverse isolation and stability in the LNA. The analysis for stability is performed using an analogy with Mason's invariant concept [9]. Besides, an insightful noise analysis is done on this LNA topology. Furthermore, extensive measurements have been performed on the VVTF LNA fabricated in [7].

In Section II, different LNA topologies are briefly reviewed and the voltage-voltage transformer feedback LNA topology is introduced. In Section III, a stability analysis is performed based on the concept of Mason's invariant. In Section IV, a noise analysis is performed on an LNA circuit with voltage-voltage transformer feedback. In Section V, the design and layout of the LNA and its transformers are discussed. In Section VI, the experimental results are presented.

II. Topology Selection

Apart from the responsibility for amplification of the signal with minimum added noise, the LNA must be stable to prevent self-oscillation. There are various LNA circuit topologies. One of the most commonly used LNA topologies is the inductively-degenerated common-source LNA, shown in Fig. 1 [1]. The inductors L_S and L_G provide the required input matching. The inductor L_S produces the real part of the input impedance and L_G nullifies the imaginary part. One of the main advanatages of this topology is the implementation of the real part of the input impedance without having to use a lossy resistor in the signal path. The input-referred noise voltage of the LNA and its input impedance are described by (1) and (2), respectively, shown at the bottom of the next page, where k is the Boltzmann constant, T is the temperature, γ is the channel noise coefficient, $\mathrm{g_{d0}}$ is the channel conductance when the drain-source voltage is zero, R_S is the source resistance, $\mathrm{g_m}$ is the transconductance of the transistor, c_{gs} is the gate-source capacitance, and ω is the angular frequency. In a good design, L_S is adjusted in such a way that the real part of z_{in} is matched with R_S, and L_G is selected in a way that the imaginary part of z_{in} is nullified. The multiple influential design parameters provide a desirable decoupling between different performance requirements. For instance, the real part of the input impedance can be adjusted independently while achieving the required noise performance.

In order to investigate the stability, a simplifying assumption that is made in the above calculations must be discarded; the gate-drain capacitance, c_{gd}, must be taken into consideration. This capacitance constitutes a reverse path between the input and output which endangers the stability. Several solutions have been proposed to overcome this problem. Using cascode architecture is one way to implement isolation between the output and input [2]. However at high frequencies the additional parasitics due to the cascode device deteriorate the performance. This has motivated the designers to adopt more complicated cascode architectures using additional inductors [3]. Using a common-gate topology is another way to provide the required isolation. However the common-gate LNAs suffer

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The authors are with Eindhoven University of Technology, Eindhoven 5612 AZ, The Netherlands (e-mail: p.sakian.dezfuli@tue.nl).

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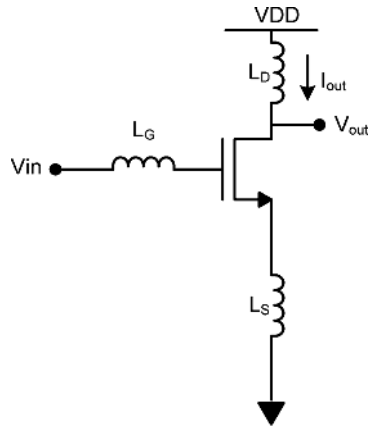

Fig. 1. An inductively degenerated common-source LNA.

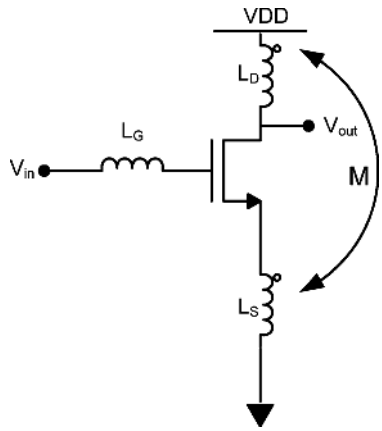

Fig. 2. Voltage-voltage transformer feedback LNA.

from a tradeoff between the input matching and the noise figure [4]–[6]. In this work the isolation is implemented by equipping L_D and L_S with mutual magnetic coupling [7], [8]. The resulting topology is called voltage-voltage transformer feedback LNA and is shown in Fig. 2.

Another potential benefit of using this topology, as compared to other solutions which entail stacking transistors on top of each other, is that it is more suited to low-voltage circuit design and hence consumes less power.

III. Stability Analysis

Stability is one of the main concerns in radio frequency amplifier design. Any reverse signal path from the output to the input can make the amplifier potentially instable. Therefore, unilateralization, or providing reverse isolation between the output and the input, is a widely used technique to ensure the stability of amplifiers. For every linear two-port device, a property can be defined that is invariant with respect to certain types of transformations [9], [10] implemented by linear lossless reciprocal embedding four-ports, shown in Fig. 3

$$U = \frac{|\det[Z - Z_t]|}{\det[Z + Z^*]} = \frac{|Z_{12} - Z_{21}|^2}{4\mathrm{Re}[Z_{11}] \cdot \mathrm{Re}[Z_{22}] - \mathrm{Re}[Z_{12}] \cdot \mathrm{Re}[Z_{21}]} \tag{3}$$

where Z is the open-circuit impedance matrix of the two-port, t denotes the transposition and * denotes the complex conjugate. Interestingly, this invariant property predicts the maximum gain after unilateralization; i.e., if the original linear two-port is unilateralized by the embedding network, the value of the maximum gain can be obtained from U [10]. Since U is invariant to the transformation done by the linear lossless reciprocal embedding network, the maximum gain can also be calculated by the z-parameters of the unilateralized device ($z'_{12} = 0$)

$$U = \frac{|Z'_{21}|^2}{4\mathrm{Re}[Z'_{11}] \cdot \mathrm{Re}[Z'_{22}]}. \tag{4}$$

It is worth noting that U is not the maximum gain obtainable from the two-port with an arbitrary four-port embedding. In fact the maximum obtainable gain is infinite, for instance when the two-port is used in an oscillator circuit. Therefore, it is important to note that U is the maximum gain only when the two-port is unilateralized; i.e., when there is no feedback between the input and output. If the condition of unilateralization is changed to stability, it can be shown that the maximum stable gain of a two-port can be as large as 4U for large values of U [11].

The LNA of Fig. 2 is visualized in Fig. 4 by an analogy with the embedding scenario of Fig. 3. The transistor is regarded as a linear two-port device, whereas the coupled inductors, or the transformers, form the embedding four-port.

The z-parameters of the transistor are calculated

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \frac{1}{g_m + c_{\mathrm{gs}} s} \times \begin{bmatrix} 1 & 1 \\ 1 - \frac{g_m}{c_{\mathrm{gd}} s} & 1 + \frac{c_{\mathrm{gs}}}{c_{\mathrm{gd}}} \end{bmatrix}. \tag{5}$$

After embedding, the z-parameters of the transformed network can be obtained from

$$Z' = \begin{bmatrix} Z'_{11} & Z'_{12} \\ Z'_{21} & Z'_{22} \end{bmatrix} \tag{6}$$

$$\bar{v}_{ni}^2 = \frac{4kT\gamma g_{d0}}{g_m^2} \frac{\left(R_S^2 + \left((L_G + L_S)\omega - \frac{1}{c_{\mathrm{gs}}\omega}\right)^2\right)\left(\frac{g_m^2 L_S^2}{c_{\mathrm{gs}}^2} + \left((L_G + L_S)\omega - \frac{1}{c_{\mathrm{gs}}\omega}\right)^2\right) c_{\mathrm{gs}}^2 \omega^2}{\left((L_G + L_S)\omega - \frac{1}{c_{\mathrm{gs}}\omega}\right)^2 + \left(\frac{g_m L_S}{c_{\mathrm{gs}}} + R_S\right)^2} \tag{1}$$

$$Z_{\mathrm{in}} = \left(\frac{g_m L_S}{c_{\mathrm{gs}}}\right) + j\left((L_G + L_S)\omega - \frac{1}{c_{\mathrm{gs}}\omega}\right) \tag{2}$$

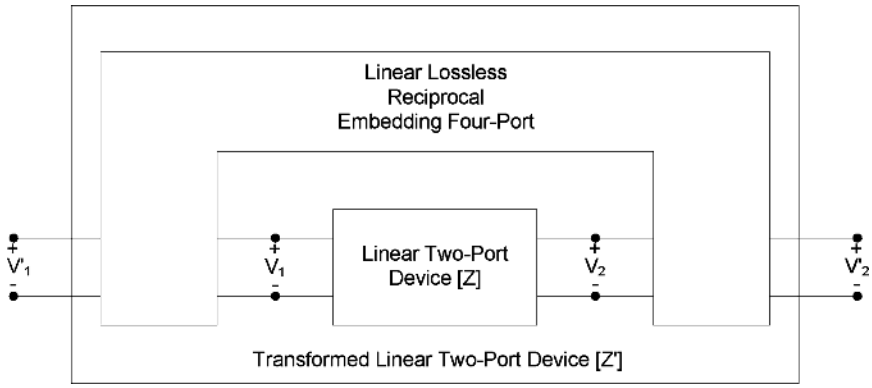

Fig. 3. Linear two-port device embedded within a linear lossless reciprocal four-port.

where z'_{11}, z'_{12}, z'_{21}, and z'_{22} are calculated from (7)–(10). The effect of L_G is then just a series reactance added to z'_{11}

$$Z'_{11} = z_{11} + L_S s - (z_{12} + L_S s + Ms) \times \frac{z_{21} + L_S s + Ms}{z_{22} + L_S s + L_D s + 2Ms} \tag{7}$$

$$Z'_{12} = -Ms + (L_D s + Ms) \times \frac{z_{12} + L_S s + Ms}{z_{22} + L_S s + L_D s + 2Ms} \tag{8}$$

$$Z'_{21} = z_{21} + L_S s - (z_{22} + L_S s + Ms) \times \frac{z_{21} + L_S s + Ms}{z_{22} + L_S s + L_D s + 2Ms} \tag{9}$$

$$Z'_{22} = -Ms + (L_D s + Ms) \times \frac{z_{22} + L_S s + Ms}{z_{22} + L_S s + L_D s + 2Ms}. \tag{10}$$

Defining the coupling factor, k_c, and the turn ratio n in (11) and (12), z'_{12} is converted to (13), after substitution of z-parameters from (4) in (8) and some manipulation. From (13) it is clear that z'_{12} can be made zero if the conditions of (14) are satisfied. By making z'_{12} zero, the required unilateralization is achieved

$$k_c = \frac{M}{\sqrt{L_D L_S}} \tag{11}$$

$$n = \sqrt{\frac{L_D}{L_S}} \tag{12}$$

$$Z'_{12} = \frac{L_D s\left(c_{\rm gd} - \frac{k_c}{n} \times c_{\rm gs}\right) + \frac{1-k_c^2}{n^2} \times c_{\rm gd} L_D^2 s^2 (g_m + c_{\rm gs} s)}{(c_{\rm gs} + c_{\rm gd}) s + \frac{c_{\rm gd} L_D}{n^2}(1 + 2k_c n + n^2) s^2 (g_m + c_{\rm gs} s)} \tag{13}$$

$$\begin{cases} k_c = 1 \\ n = \frac{c_{\rm gs}}{c_{\rm gd}} \end{cases}. \tag{14}$$

The conditions of (14) are the only solution to providing isolation at all frequencies. If k_c is not equal to one, the isolation can only be achieved if the circuit is modified, for instance by adding an inductor in parallel with $c_{\rm gd}$ which can neutralize the reactance between the source and the drain at a certain frequency. Therefore, without meeting the conditions of (14), it is not possible to obtain a frequency-independent isolation. In this work our attempt is to make k_c as close to one as possible.

In case of unilateralization which is obtained by meeting the conditions of (14), the input impedance of the LNA of Fig. 4 is derived from (15) which shows that the real part of the input impedance is zero (in fact limited to the gate resistance of the transistor) and the imaginary part can be made zero by properly adjusting the value of L_G

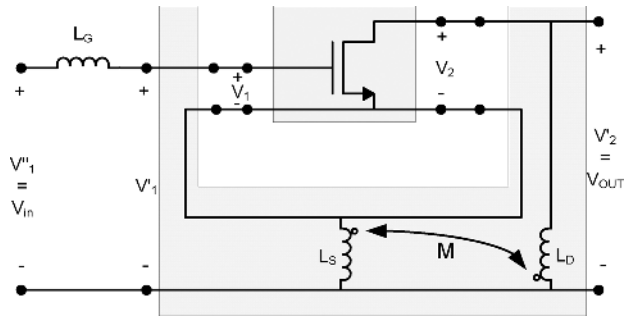

Fig. 4. LNA of Fig. 2 illustrated as a two-port device (a single transistor) embedded in a linear reciprocal four-port (transformer).

$$Z_{\rm in} = L_G j\omega + Z'_{11} = L_G j\omega + \frac{1}{j\omega(c_{\rm gs} + c_{\rm gd}).} \tag{15}$$

In case of unilateralization, if R_G (the gate resistance of the transistor) is not neglected and when L_G is in resonance with the capacitive part of $z_{\rm in}$ and z'_{11}, the z parameters of the circuits of Fig. 4 are derived from the following:

$$Z''_{11} = R_G \tag{16}$$

$$Z''_{12} = Z'_{12} = 0 \tag{17}$$

$$Z''_{21} = Z'_{21} = \frac{-g_m L_D}{1 - c_{\rm gd} L_D (c_{\rm gs} + c_{\rm gd})\omega^2 + \frac{g_m c_{\rm gd} L_D}{c_{\rm gs}}(c_{\rm gs} + c_{\rm gd}) j\omega} \tag{18}$$

$$Z''_{22} = Z'_{22} = \frac{L_D c_{\rm gs} j\omega}{1 - c_{\rm gd} L_D (c_{\rm gs} + c_{\rm gd})\omega^2 + \frac{g_m c_{\rm gd} L_D}{c_{\rm gs}}(c_{\rm gs} + c_{\rm gd}) j\omega}. \tag{19}$$

It is worth mentioning that the z, z', and z'' parameters are describing the transistor, the two-port seen from V'_1 and V'_2, and the two-port seen from V''_1 and V'_2, respectively (See Fig. 4).

The value of U can be calculated in two ways: the z' parameters from (16)–(19) can be substituted in (3) or (4); or the Z parameters from (5) can be substituted in (3) after adding R_G to

z_{11} to include the transistor gate series resistance. As expected and as evidence to the invariability of U under the transformation of Fig. 4, both approaches yield the same result

$$U = \frac{g_m}{4R_G c_{\rm gd}\omega^2(c_{\rm gs} + c_{\rm gd})}. \tag{20}$$

To confirm the predictions made by the above formulae, z''_{21} and z''_{12} of a voltage-voltage transformer feedback amplifier are simulated as a function of the turn ratio (n). The simulation is done by SPECTRE-RF periodic-scattering-parameter analysis at 60 GHz. The transistor width and transistor length are 32 μm and 65 nm, respectively. The biasing voltage of the gate of the transistor and $V_{\rm DD}$ are 0.7 and 1.2 V, respectively. The biasing current of the transistor is 4.9 mA. L_S is kept constant at 500 pH while $\rm n^2$ and hence L_D are swept from 0.1 to 5 and from 5 pH to 12.5 nH, respectively. The coupling factor between L_S and L_D is one. L_G is 207 pH to nullify the imaginary part of the input impedance. The extracted values for $c_{\rm gs}$ and $c_{\rm gd}$ are 21.8 and 11.5 fF, respectively. According to (14), perfect reverse isolation is obtained when $\rm n^2$ reaches 3.6. In Fig. 5(a), it is seen that the simulated z''_{12} is minimized at around 3.1, whereas the calculated z''_{12} is minimized at around 3.6. This difference between the prediction and simulation is due to the series source resistance (r_s) of the transistor which is not taken into account in our simple model and in fact shifts the real part of z''_{12} by a constant amount equal to r_s. As a result the real part of z''_{12} becomes zero at a different turn ratio than expected. However, the imaginary part of z''_{12}, as can be seen in Fig. 5(a), becomes zero precisely at the point predicted by calculations. Fig. 5(b) shows the simulated and calculated values of z''_{21}, illustrating that z''_{21} increases monotonically with n. Therefore, the reverse isolation can be achieved without sacrificing the gain. The discrepancy between the simulated and calculated values of z''_{21} and z''_{12} emanates mostly from the drain-bulk capacitance $(c_{\rm db})$ and also from the source-bulk capacitance $(c_{\rm sb})$ which are not taken into account in the simple transistor model used in our calculations. Fig. 5(c) shows the simulated z''_{12} and z''_{21} for different values of k_c (1, 0.9, 0.8, and 0.7) indicating that the proper choice of turn ratio can minimize z''_{12} only if the coupling (k_c) is equal to one.

It can be shown (see Appendix) that the electric coupling between the primary and secondary windings of the transformer $(c_{\rm ps})$, which is ignored in our simple model, does not influence the required condition of (14) for isolation, although it changes the values of predicted Z-parameters. The same is true about source-bulk and drain-bulk capacitances ($c_{\rm sb}$ and $c_{\rm db}$).

Furthermore, as shown in the Appendix, even the losses of the transformer do not change the requirements of (14) for isolation.

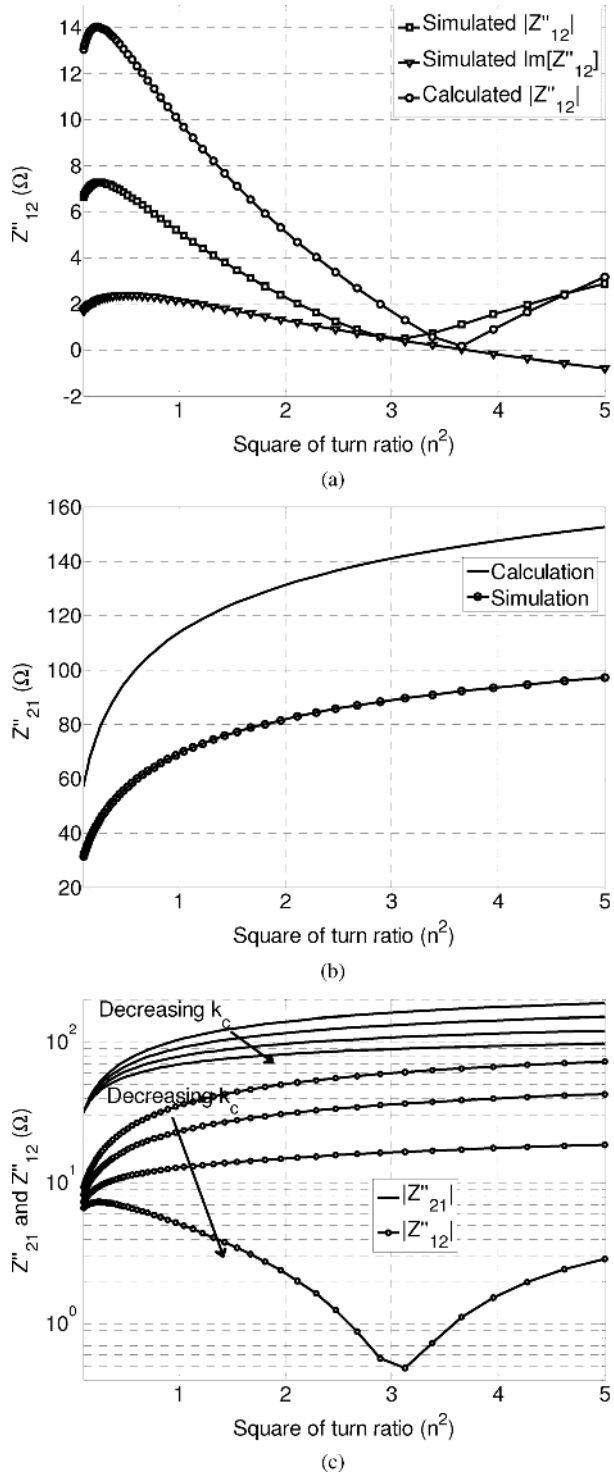

Fig. 5. z''_{21} and z''_{12} of the amplifier versus the square of turn ratio of the transformer showing the minimization of z''_{21} by proper choice of turn ratio and coupling factor. (a) Simulated and calculated magnitude of z''_{12} and simulated imaginary part of z''_{12} for $k_c = 1$. (b) Simulated and calculated magnitude of z''_{21} for $k_c = 1$. (c) Simulated magnitude of z''_{21} and z''_{12} for k_c values of 1, 0.9, 0.8, and 0.7.

IV. Noise Analysis

In order to perform a noise analysis, the circuit schematic of the LNA including the transistor channel noise and the source noise is shown in Fig. 6(a). Considering the transistor as a linear two-port, the channel noise can be transferred back to its gate, as shown in Fig. 6(b), using the T-parameters of the transistor. Then the resultant noise current source between the gate and the source of the transistor can be split into two, as shown in Fig. 6(c). Considering the whole circuit as a two-port, with one port between the gate of the transistor and the ground and the other port between the source of the transistor and the ground,

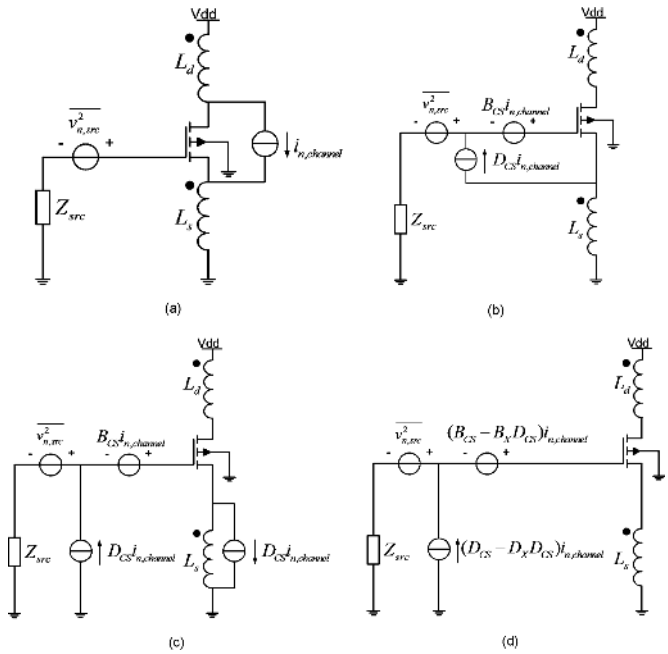

Fig. 6. Manipulating the internal noise source of the transistor to refer it to the input. (a) Original circuit schematic with the channel noise current source. (b) Using T-parameters of the transistor to refer the channel noise to the gate of the transistor. (c) Splitting the floating noise current source between gate and source. (d) Using T-parameters of the whole circuit to refer the remaining current source to the input.

and calculating the T-parameters of this two-port, the noise current source in parallel with L_S can be transferred back to the input, as shown in Fig. 6(d).

According to Fig. 6, only the B and D elements of the T matrices are needed. Therefore, the B and D elements of the T-matrix of the transistor are obtained from

$$B_{CS} = \frac{1 + R_G S(c_{\rm gs} + c_{\rm gd})}{c_{\rm gd}s - g_m} \tag{21}$$

$$D_{CS} = \frac{(c_{\rm gs} + c_{\rm gd})s}{c_{\rm gd}s - g_m} \tag{22}$$

where R_G is the gate resistance of the transistor. The B and D elements of the T-matrix of the other two-port, represented by the transistor gate as the input and the transistor source as the output with the ground considered as the common node, are derived from (23) and (24), shown at the bottom of the page, which in case of unilateralization and meeting the conditions of (14) are simplified to

$$B_x = \frac{1}{(1+n)g_m} \tag{25}$$

$$D_x = \frac{(c_{\rm gs} + c_{\rm gd})s}{(1+n)g_m}. \tag{26}$$

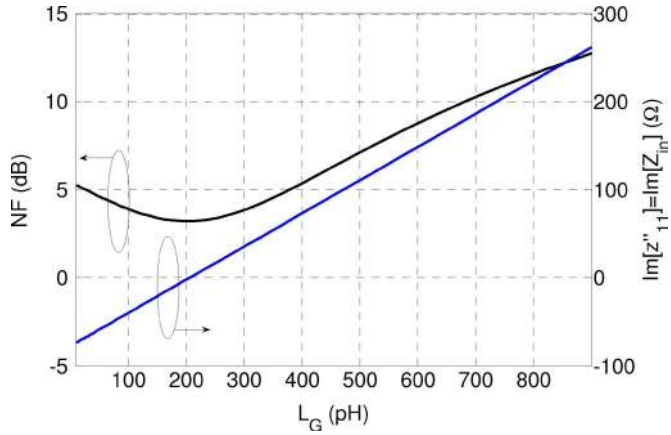

Fig. 7. Simulated imaginary part of the input impedance of the LNA of Fig. 2 and simulated noise figure of the same LNA versus L_G.

The total noise contribution referred to the input of the circuit is then obtained from

$$\overline{v_{n,i}^2} = 4KTR_G + |(B_{CS} - B_xD_{CS}) + (D_{CS} - D_xD_{CS})Z_{\rm src}|^2 4KT\gamma g_m. \tag{27}$$

The noise figure is then calculated from the following:

$$\mathrm{NF} = 1 + \frac{R_G}{R_{\rm src}} + \frac{\gamma}{g_m R_{\rm src}} \times \left(1 + \frac{(c_{\rm gs} + c_{\rm gd})^2\omega^2}{g_m^2(1+n)^2}\right)|1 + Z_{\rm src}(c_{\rm gs} + c_{\rm gd})j\omega|^2 \tag{28}$$

where $R_{\rm src}$ is the real part of the source impedance. According to (28), the NF can be minimized if the reactive part of the source impedance resonates with the gate-source and gate-drain capacitances ($c_{\rm gs}$ and $c_{\rm gd}$).

It is also deduced from (15) that the imaginary part of the input impedance is cancelled out when L_G resonates with $c_{\rm gs}$ and $c_{\rm gd}$. The imaginary part of the input impedance and the simulated NF versus L_G are shown in Fig. 7, showing that the minimum noise figure is achieved when the imaginary part of the input impedance is zero. Fig. 8 shows the simulated noise figure showing sharp increase in NF for small values of $R_{\rm src}$ and a relatively flat curve for larger values of $R_{\rm src}$. The simulation conditions are the same as Section III.

In fact, because $R_{\rm src}$ is in the denominator of the second and third term of (28), the NF shows strong dependence on $R_{\rm src}$ for small values of $R_{\rm src}$. However, for moderate and larger values of $R_{\rm src}$, $z_{\rm src}$ in the numerator of the third term becomes more influential, resulting in a pretty flat curve for NF (See Fig. 8).

In this analysis, for simplicity, the thermal channel noise of the transistor and the gate resistance of the transistor have been

$$B_x = \frac{1 + c_{\rm gd}s^2\left(1-k_c^2\right)L_D}{\left(1-k_c^2\right)L_D c_{\rm gd}s^2(c_{\rm gs}s + g_m) + (c_{\rm gs} - nk_c c_{\rm gd})s + (1+nk_c)g_m} \tag{23}$$

$$D_x = \frac{\left(1-k_c^2\right)L_D c_{\rm gd}s^2(c_{\rm gs}s + g_m) + (c_{\rm gs} + c_{\rm gd})s}{\left(1-k_c^2\right)L_D c_{\rm gd}s^2(c_{\rm gs}s + g_m) + (c_{\rm gs} - nk_c c_{\rm gd})s + (1+nk_c)g_m} \tag{24}$$

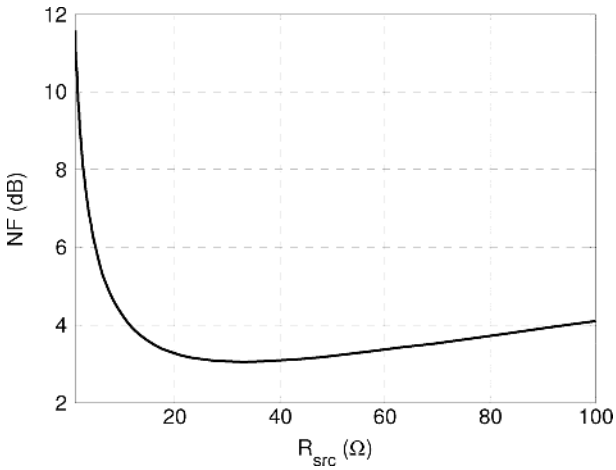

Fig. 8. Simulated noise figure of the LNA versus source resistance.

considered as the dominant noise sources in the circuit. However, the loss in other elements such as the losses of the transformer can appear as additional noisy elements in the circuit. Quantitative analysis of the impact of the transformer loss on the noise figure would require dealing with a more complicated circuit model.

V. Circuit Design

A two-stage differential variant of the circuit topology discussed in the previous sections has been designed, as shown in Fig. 9, in 65 nm LP bulk CMOS technology with 7 metal layers and an aluminum layer on top. The thickness of aluminum layer, metal 7, metal 6, and metal 5 is 1.45 μm, 0.9 μm, 0.9 μm, and 0.22 μm, respectively. The dielectric height between metal 7 and aluminum, between metal 6 and metal 7, between metal 5 and metal 6, and between silicon and metal 5 is 0.8 μm, 0.595 μm, 0.595 μm, and 2.13 μm, respectively. The main design objectives, aside from stability discussed in Section III, are low noise figure and high gain. Both are functions of the transistor biasing and width, passives choices, and source impedance $z_{\rm src}$. The transducer power gain of the LNA after unilateralization is obtained from (29), shown at the bottom of the page, where R_L is the load resistance (not shown in Fig. 9). From the last term of (29) it is clear that the resonance between L_G and $c_{\rm gs}+c_{\rm gd}$ maximizes the transducer gain, a condition identical to the one required for noise figure optimization and canceling the imaginary part of the input impedance.

The losses in the transformer can be modeled by two resistances, one in parallel with L_D and one in parallel with L_S, as shown in Appendix. These losses reduce the amount of power delivered to the load and thereby decrease the gain.

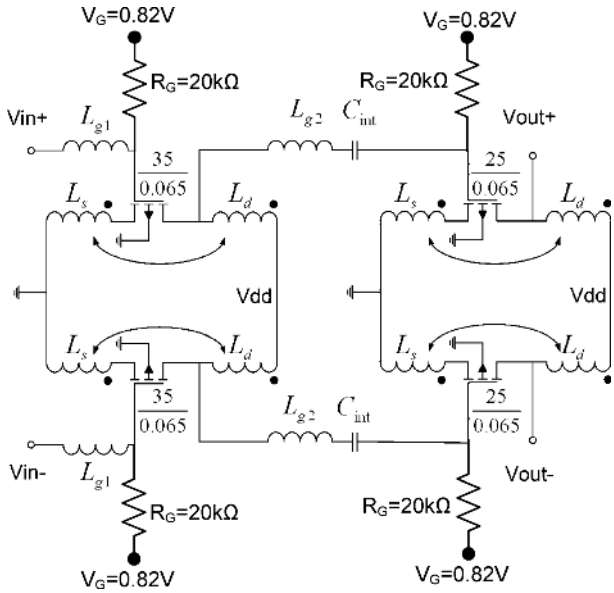

Fig. 9. Circuit schematic of the two-stage differential voltage-voltage transformer-feedback LNA: finger width of transistors is 1 μm, simulated values for L_D and L_S are 137 pH and 42 pH, respectively. L_{g1} and L_{g2} are 110 pH and 150 pH, respectively. Each transistor in the first stage draws 8.65 mA. Each transistor in the second stage draws 6.25 mA.

The transformer used in the LNA is designed using EM simulations with ADS Momentum. The resulting structure is shown in Fig. 10. The top inductor (L_S) consists of two metal lines in parallel to lower the inductance and increase the Q-factor. The bottom inductor (L_D) has two turns, connected through vias which are distributed all along the metal lines. Both inductors are placed exactly on top of each other to achieve the highest possible coupling $(|k| \approx 1)$. The width of the metal lines is chosen to be 3 μm. This decision constitutes a trade-off between Q-factor and self-resonance frequency (SRF) [12]. The simulated SRF of the transformer is 98 GHz. To satisfy (14) for isolation, a turn ratio n of 1.8 is chosen. While a coupling factor k_c of 1 is needed for satisfying (14), the best we could achieve was 0.76. The simulated Q-factors of the inductors are higher than 10 at the frequency of interest. Simulated values for L_D and L_S are 137 pH and 42 pH, respectively. A patterned shield is placed underneath the transformers to reduce substrate coupling.

Two stages are cascaded together, as shown in Fig. 9, to achieve an acceptable gain, as compared to state-of-the-art LNAs. The layout of the core of the LNA is shown in Fig. 11. The differential input of the first stage is shown on the left and the differential output of the second stage is on the right. The two stages are connected to each other with a DC-blocking capacitor between the output of TF1 and the input of $L_{\rm g2}$. All

$$G_T = \frac{g_m^2 L_D^2 n^2 (1+n) j\omega}{c_{\rm gd}} \times \frac{1}{n^2 + g_m L_D (1+n) j\omega - L_D n (c_{\rm gd}+c_{\rm gs})\omega^2} \times \frac{1}{n^2 R_L + L_D (n^2 + g_m (1+n) R_L) j\omega - L_D n (c_{\rm gd}+c_{\rm gs}) R_L \omega^2} \times \frac{1}{1 + (c_{\rm gd}+c_{\rm gs}) j\omega (R_G + R_S) - (c_{\rm gd}+c_{\rm gs}) L_G \omega^2} \tag{29}$$

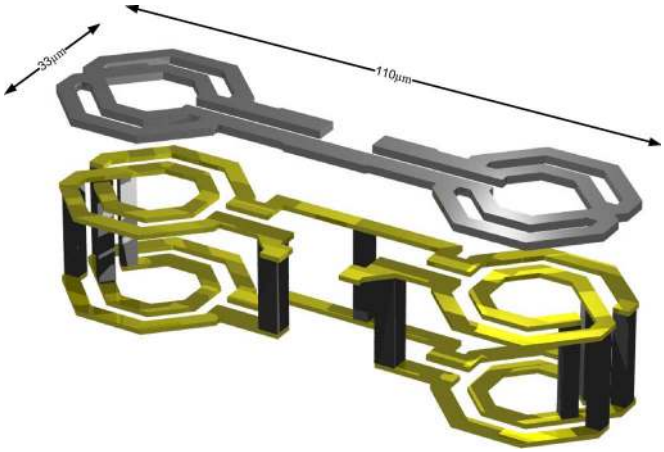

Fig. 10. Transformer structure. For clarity the vias connecting the two bottom metals are only shown at the beginning and the end of the metal strips.

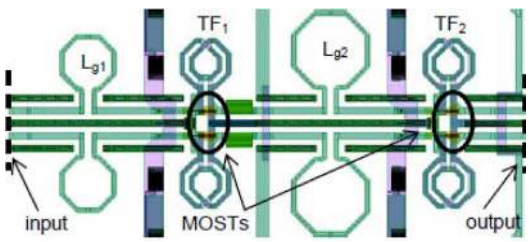

Fig. 11. Layout of the LNA (330 × 170 μm). Only the top metal layers shown to clarify the structure. Patterned shields not shown. The input and output reference planes are indicated by dashed lines.

the RF interconnects longer than 10 μm are simulated in ADS Momentum to account for their parasitic inductances, their parasitic capacitances, and their losses. The rest of the layout is simulated after RC-extraction. The parasitic inductances in the signal path are either included in the input transmission line or the gate inductance L_{g1}. The parasitic inductances in the ground and supply routing are minimized by meshing the ground and supply interconnects.

L_{g1} and L_{g2} are approximately 110 pH and 150 pH, respectively. The transistors are indicated in Fig. 11 and are situated underneath the metal lines connecting the transformer structures. Transistor width is 35 μm and 25 μm in stage 1 and stage 2, respectively. The finger width is 1 μm. The vertical lines surrounding the transformers are the DC power lines and biasing of the LNA. Coplanar waveguides (CPW) with shielding are used to connect different components to each other. This results in low coupling to the substrate and between components. Special attention is paid to keeping the connections between transistors and inductors as short as possible to avoid increasing the parasitic capacitances. For instance the drain and source inductors are placed so close to the transistors that they are just connected through vias.

The input and output of the LNA are connected to bondpads using CPWs (see Fig. 12) which result in losses and an impedance shift. The resulting source and load impedance of the circuit at the input and output indicated in Fig. 11 is approximately $37 + \mathrm{j}10\ \Omega$. Open, short, and load structures are added to de-embed the circuit. Differential coplanar waveguide

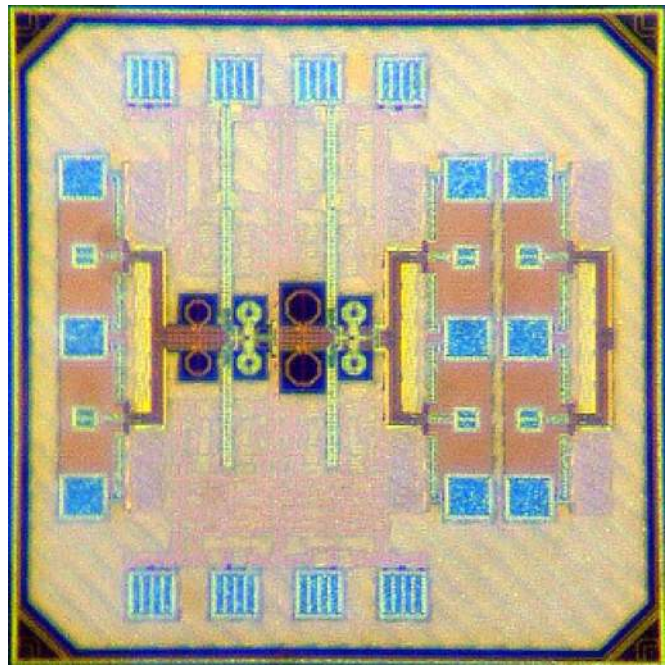

Fig. 12. Die photo including the whole LNA with bondpads on the left and one de-embedding structure on the right. Size of the die is 960 × 980 μm, size of the LNA is 330 × 170 μm.

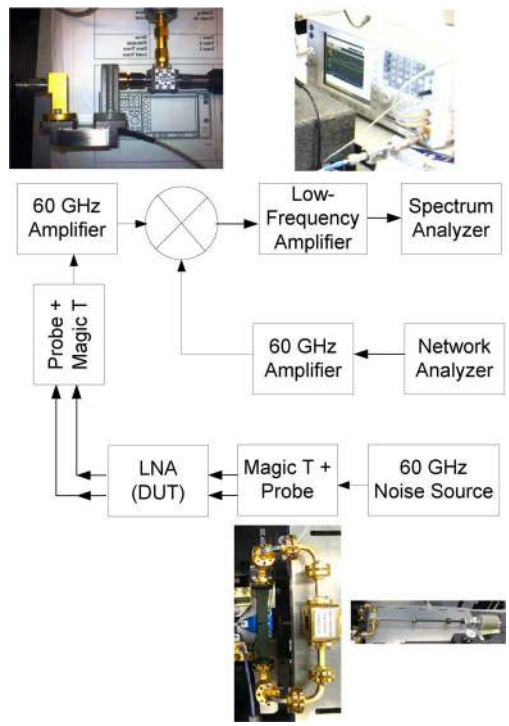

Fig. 13. LNA noise figure measurement setup.

used in the layout are chosen to have a characteristic impedance of $z_0 = 100\ \Omega$ differential, because the measurement equipment are 50 Ω single-ended. The signal lines are made with the top metal layer (metal 7) with 4 μm width. Two ground planes are placed at both sides of the signal line by stacking all metal layers. The spacing between the lines is also 4 μm. The bottom patterned shielding metal (metal 1) below the signal

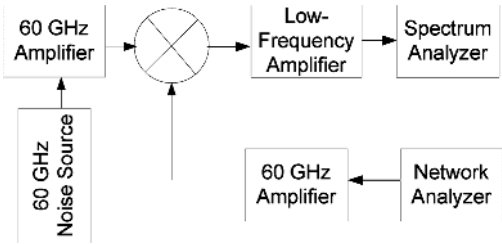

Fig. 14. Noise figure calibration for the LNA.

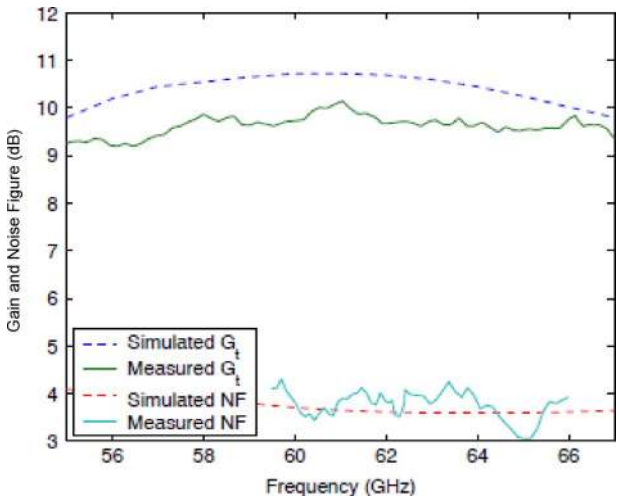

Fig. 15. Measured and simulated differential gain and noise figure.

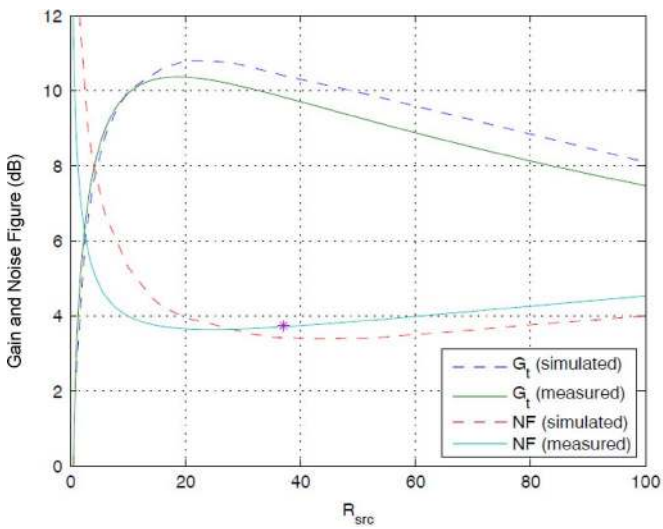

Fig. 16. NF and G_T variation as a function of $R_{\rm src}$. The star in the figure indicates the measurement result without use of the load-pull setup.

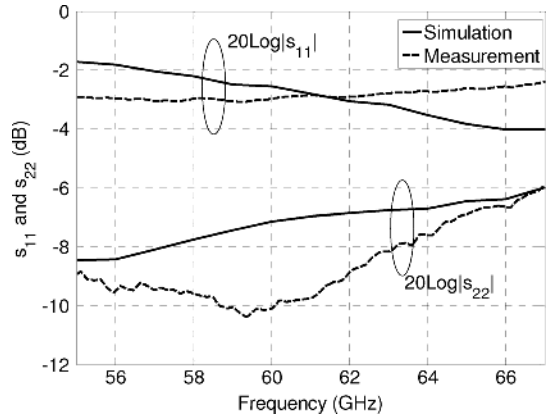

Fig. 17. Simulated and measured s_{11} and s_{22} for 100 Ω differential reference impedance.

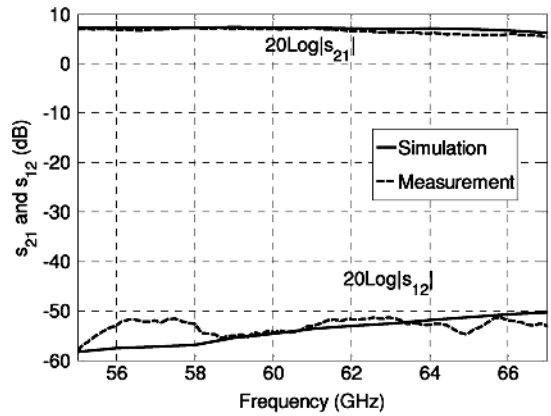

Fig. 18. Simulated and measured s_{12} and s_{21} for 100 Ω differential reference impedance.

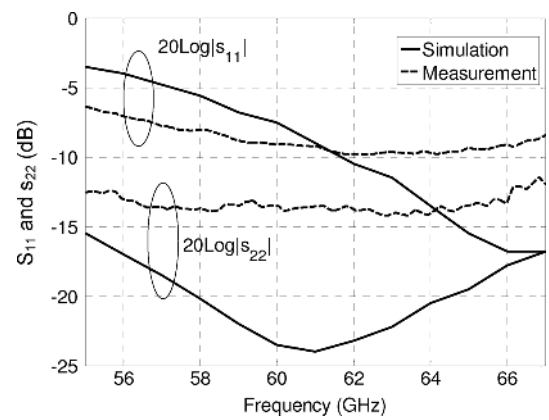

Fig. 19. Simulated and measured s_{11} and s_{22} for 30 Ω differential reference impedance at the input (representing the anticipated on-chip antenna) and (100 Ω || 30 fF) differential reference impedance at the output (representing the following stage which has a capacitive input.

line is also defined as ground to reduce substrate effects. Simulations show a loss of 1.18 dB/mm. A special effort has been put into making the design as symmetric as possible to reduce the common mode.

VI. Experimental Results

The LNA, fabricated in CMOS 65 nm technology, is measured using a differential measurement setup [13]. The DC power consumption is observed to be equal to the simulated value of 35 mW.

The S-parameters are measured using the Agilent E8361A power network analyzer. Calibrations are verified using WinCal XE software. After de-embedding the measured G_T with $z_{\rm src} = 30\ \Omega$ is 10 dB at 61 GHz (Fig. 13). The measured in-band deviation is ± 0.25 dB. The output-to-input isolation indicated by s_{12}

TABLE I
COMPARISON WITH OTHER WORKS

Reference	Process	Topology	G_T (dB)	NF (dB)	3 dB BW	IIP_3 (dBm)	V_{dd} (V)	P_{DC} (mW)
[14]	90nm	3 stage CS	15	4.4	10%	N/A	1.3	4
[15]	65nm (SOI)	2 stage casc.	12	8	22%	N/A	2.2	36
[3]	90nm	2 stage casc.	14.6	<5.5	25%	-6.8	1.5	24
[17]	65nm	2 stage casc. + 1 CS	22.3 (A_v)	6.1	13%	N/A	1.2	35
[16] (LNA+mixer)	45nm	2 stage casc.	26	6	N/A	-12	1.1	23
[18]	45nm	2 stage CS	10	3.2	25%	N/A	1.1	N/A
This work (Source 100Ω)	65nm	2 stage CS	8	4.5	—	—	1.2	35
This work (Source 30Ω)	65nm	2 stage CS	10	3.8	37% (simulated)	4	1.2	35

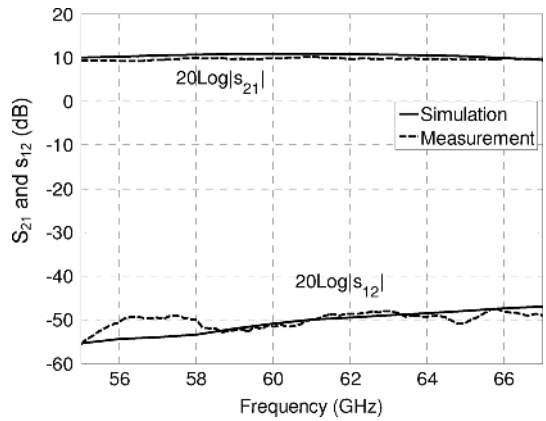

Fig. 20. Simulated and measured s_{12} and s_{21} for 30 Ω differential reference impedance at the input and (100 Ω || 30 fF) differential reference impedance at the output.

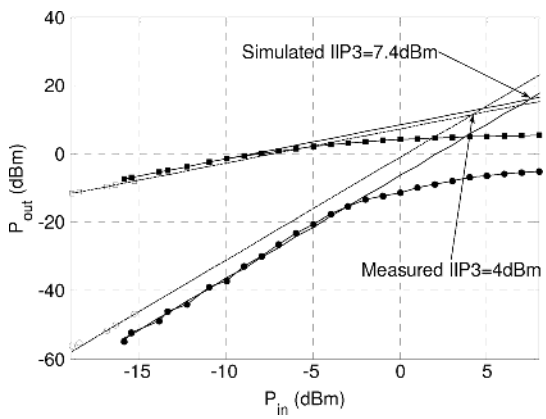

Fig. 21. Simulated and measured IP3 curves.

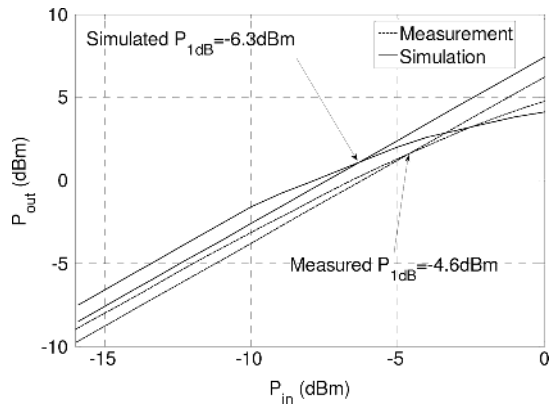

Fig. 22. Simulated and measured 1 dB compression point curves.

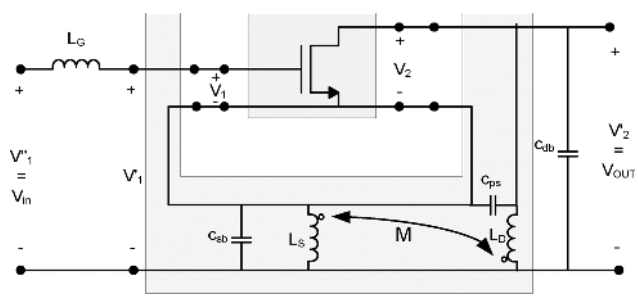

Fig. 23 Modified circuit schematic of Fig. 4 used to analyze the impact of $c_{\rm ps}$, $c_{\rm db}$, and $c_{\rm sb}$.

is below −47 dB over the entire measured band of 55–67 GHz and the group delay is close to 20 ps over the entire band of interest. The differential stability factor (K-factor) remains above 30 in the measured band.

The common mode maximum transducer gain is equal to −2 dB resulting in a CMRR of 12 dB. The s_{12} is below −42 dB, and the K-factor remains above 70.

The noise figure measurement of the 60 GHz LNA is impeded by the fact that the output of the LNA is at a higher frequency than supported by the spectrum analyzer. A passive mm-wave mixer is used in the noise measurement setup to downconvert the output of the LNA to the range of the spectrum analyzer. The noise figure measurement setup is illustrated in Fig. 13. The passive mixer can be included in the calibration setup obviating the need for its inclusion in post-measurement calculations, as shown in Fig. 14. The loss of the interface waveguides

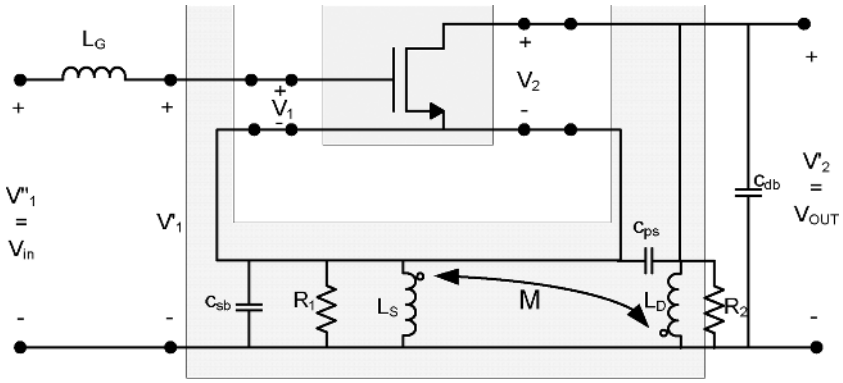

Fig. 24 Modified circuit schematic of Fig. 4 used to analyze the impact of $c_{\rm ps}$, $c_{\rm db}$, $c_{\rm sb}$, and the losses of the transformer.

and probe at the input of the DUT are measured separately and de-embedded from the measurement results manually.

The noise figure is measured in the band 59.5–66 GHz (Fig. 15). $z_{\rm src}$, looking from the input of the LNA towards the source, during this measurement is equal to $37 + {\rm j}10\ \Omega$, as a result of impedance transformation made by the input transmission lines and bondpads which are de-embedded from the measurement results. The input reflection coefficient seen by the noise source is below -15 dB. The average measured NF in this band is equal to 3.8 dB.

Fig. 16 shows the variations of NF and G_T for different values of source impedance using a source-pull measurement setup. This measurement is done by modifying the measurement setup of Fig. 13 through adding a source-pull between the noise source and the DUT [18]. The $\rm NF_{min}$ of the circuit is found to be 3.7 dB.

Figs. 17 and 18 show the simulated and measured s-parameters of the LNA for 100 Ω differential reference impedance at both input and output. However, the LNA is not designed for 100 Ω antenna and mixer. The on-chip differential antenna is expected to provide a 30 Ω impedance whereas the mixer following the LNA is expected to have a capacitive input of 30 fF in parallel with a 100 Ω. Therefore, s_{21} is optimized for such a configuration as illustrated in the simulated and measured s-parameters of Figs. 19 and 20.

The measured IIP3 is equal to 5 dBm at 57.5 GHz and 4 dBm at 60 GHz. Fig. 21 shows the IP3 curve for a two-tone input at 60 GHz with 1 MHz spacing. The measured 1 dB compression point is -4.6 dBm, as shown in Fig. 22.

The performance of the existing 60 GHz LNAs is compared with this work in Table I. The LNAs presented in [14], [15], [3], and [16] are single ended, and [17] has a differential output. The work presented here shows one of the lowest noise figures and the highest bandwidth. The relatively low gain is due to using only two cascaded stages. The reported gain is from the differential input to the differential output.

VII. Conclusion

A noise and isolation analysis is done on a voltage-voltage transformer feedback LNA topology providing design insight for lowering the noise figure and preserving stability in such circuits. It has been shown that a close analogy prevails between the classic concept of Masons's invariant and the isolation in this type of LNAs. Furthermore, the presented noise analysis provides closed-form equations which can capture the variation trends of the LNA noise figure as a function of the transistor and passives parameters. Using the analysis results, a two-stage fully integrated 60 GHz differential low noise amplifier is implemented in a CMOS 65 nm technology. Utilizing a voltage-voltage transformer feedback enables the neutralization of the Miller capacitance and the achievement of a flat 10 dB gain over the entire 6 GHz bandwidth. A noise figure of 3.8 dB is obtained.

Appendix I

We investigate the impact of $c_{\rm ps}$ (representing the electric coupling between the primary and the secondary), $c_{\rm sb}$, and $c_{\rm db}$ on the stability analysis performed in Section III. Afterwards we also investigate the impact of the transformer loss on the stability analysis. Solving the circuit of Fig. 23 for z''_{12} results in (A-1), shown at the bottom of the page, where z_{11}, z_{12}, z_{21}, and z_{22} are the z-parameters of the transistor as defined in (5). Forcing the numerator of (A-1) to zero and writing M and L_D in terms of n and L_S from (11)–(12), we obtain

$$n(L_S s(c_{ps} s Z_{22} + c_{sb} s Z_{12} + 1) + Z_{12}) = k_c(k_c n L_S s(c_{ps} s Z_{22} + c_{sb} s Z_{12} + 1) - Z_{12} + Z_{22}). \quad \text{(A-2)}$$

Further simplification yields

$$nL_S s(c_{ps} s Z_{22} + c_{sb} s Z_{12} + 1)\left(1 - k_c^2\right) + nZ_{12} = k_c(Z_{22} - Z_{12}). \quad \text{(A-3)}$$

$$Z''_{12} = \frac{(s(L_D(L_S s(c_{ps} s Z_{22} + c_{sb} s Z_{12} + 1) + z_{12}) - M(Ms(c_{ps} s Z_{22} + c_{sb} s Z_{12} + 1) - Z_{12} + Z_{22})))}{(Z_{22}\left(s^4(c_{db}(c_{ps} + c_{sb}) + c_{ps} c_{sb})\left(L_D L_S - M^2\right) + s^2(c_{db} L_D + c_{ds}(L_D + L_S + 2M) + c_{sb} L_S) + 1\right) + s\left(s^2(c_{db} + c_{sb})\left(L_D L_S - M^2\right) + L_D + L_S + 2M\right))} \quad \text{(A-1)}$$

$$\begin{cases} z_{12}'' = \dfrac{R_2 s(L_D(L_S s(c_{ps}sR_1z_{22}+c_{sb}sR_1z_{12}+R_1+z_{12})+R_1z_{12})-M(Ms(c_{ps}sR_1z_{22}+c_{sb}sR_1z_{12}+R_1+Z_{12})+R_1(z_{22}-z_{12})))}{B} \\ B = z_{22}(R_1R_2s^4(c_{db}(c_{ps}+c_{sb})+c_{ps}c_{sb})(L_DL_S-M^2)+s^3(L_DL_S-M^2)(R_2(c_{db}+c_{ps})+R_1(c_{ps}+c_{sb})) \\ \quad +s^2(R_1R_2(c_{db}L_D+c_{ps}(L_D+L_S+2M)+c_{sb}L_S)+L_DL_S-M^2)+s(L_DR_1+L_SR_2)+R_1R_2) \\ \quad +s(R_1R_2s^2(c_{db}+c_{sb})(L_DL_S-M^2)+s(R_1+R_2)(L_DL_S-M^2)+R_1R_2(L_D+L_S+2M)). \end{cases} \quad \text{(A-5)}$$

According to (A-3) for a frequency-independent nullification of z_{12}'', we need

$$\begin{cases} k_c = 1 \\ (n+1)Z_{12} = Z_{22} \end{cases} \quad \text{(A-4)}$$

which after substituting z_{12} and z_{22} from (5), results in the same conditions specified in (14).

For considering the impact of the transformer loss on the stability analysis, we have to solve the circuit of Fig. 24 for z_{12}'' which results in (A-5), shown at the top of the page. Forcing the numerator of (A-5) to zero and writing M and L_D in terms of n and L_S from (11)–(12), we obtain

$$nL_Ss(c_{ps}sR_1Z_{22}+c_{sb}sR_1Z_{12}+R_1+R_1Z_{12})\left(1-k_c^2\right) + nR_1Z_{12} = k_cR_1(Z_{22}-Z_{12}). \quad \text{(A-6)}$$

Once again for a frequency-independent nullification of z_{12}'' the conditions of (A-4) and consequently (14) must hold without any influence by R_1 and R_2.

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Pooyan Sakian was born in Ghom, Iran, in 1981. He received the B.Sc. and M.Sc. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran, and the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands in 2003, 2006, and 2011, respectively.

His research interests include analog and RF IC design for wireless communications.

Erwin Janssen was born in Deurne, The Netherlands, on July 20 1982. He received the B.S. degree in electrical engineering from Fontys Hogescholen, Eindhoven, The Netherlands, in 2004, and the M.S. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, The Netherlands, in 2008, where he is currently working toward the Ph.D. degree.

His main research interests are concerned with the digital compensation of nonlinear distortion in RF receivers.

Arthur H. M. van Roermund (SM'95) was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in electrical engineering in 1975 from the Delft University of Technology, Delft, The Netherlands, and the Ph.D. degree in applied sciences from the K.U. Leuven, Belgium, in 1987.

From 1975 to 1992, he was with Philips Research Laboratories, Eindhoven. From 1992 to 1999 he was a Full Professor at the Electrical Engineering Department, Delft University of Technology, where he was Chairman of the Electronics Research Group and Member of the management team of DIMES. From 1992 to 1999 he was Chairman of a two-years post-graduate school for "chartered designer". From 1992 to 1997 he was a consultant for Philips. In October 1999 he joined Eindhoven University of Technology as a Full Professor, chairing the Mixed-signal Microelectronics Group. Since September 2002, he has been Director of Research of the Department of Electrical Engineering. Until 2009, he was a member of the supervisory board of the NRC Photonics Research Centre. He is chairman of the board of ProRISC, the microelectronics platform in the Netherlands, and Vice Chair of the ICT-research platform for the Netherlands (IPN). Since 2001, he has been one of the three organizers of the yearly workshop on Advanced Analog Circuit Design (AACD). He authored/co-authored 470 articles and 29 books.

Dr. van Roermund received the Simon Stevin Meester award in 2004 for his scientific and technological achievements. In 2007 he was member of an international assessment panel for the Department of Electronics and Information of Politecnico di Milano, and in 2009 for Electronics and Electrical Engineering for the merged Aalto University Finland.

Reza Mahmoudi received the M.Sc. degree in electrical engineering with a thesis entitled "A Measurement System for Noise Parameters" from the Delft University of Technology, Delft, the Netherlands, in 1993 where he joined the Microwave Component Group until 1999, and the Designers Certificate from Delft in 1996 with a thesis entitled "A Systematic Design Method for a Feed-Forward Error Control System." This work was the initial step leading to his Ph.D. thesis.

He has worked for Philips Discrete Semiconductors in Nijmegen, the Netherlands, and Advanced Wave Research in El Segundo, CA. Since April 2003, he has been with the Department of Electrical Engineering at Eindhoven University of Technology/Eindhoven, The Netherlands. He is currently an Associate Professor in the field of "ultra-high frequency front-end electronics" and ultrahigh speed communication as well as high resolution imaging systems are forming his research areas. He has participated with 76 academic publications.