Analysis and Design of a Charge Pump Circuit for High Output Current Applications

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Abstract

A charge pump circuit has been developed that can deliver high currents even for a system supply voltage of 3 V. The circuit consists of capacitances, connected by MOS switches. The influence of the on-resistance of the switches on the circuit's output resistance has been analysed. The switches are implemented by PMOS transistors. The source bulk potential of these transistors is kept constant to prevent an increase in threshold voltage of the transistors. The maximum output voltage is determined by the breakdown voltage of the switches and not by the MOST's threshold voltage. The circuit has been realised and measurement results match with the calculated values.

1 Introduction

EEPROM circuits require high voltages up to 15 V for programming and erasing. For flexibility the system can only use the standard supply voltage, so it is necessary to generate the high voltages on-chip. A so-called charge pump circuit is used to transform the supply voltage up to the desired high voltage. Increase of the number of EEPROM cells in one system requires an increase in current to be delivered by the high voltage generator. An improved charge pump circuit is presented that can generate the required high voltage and currents, even for the lower system supply voltages used by new generation EEPROMs.

2 A charge pump circuit using switches

Charge pump circuits consist of a chain of capacitors, which are booted up by two non-overlapping clock signals. Dickson [1] described a circuit where the charge is transferred from one capacitor to the next one by a diode or by a MOS transistor connected as a diode. Witters *et al* [2] gave an extended analysis of this circuit. The charge is transferred from a capacitor to the next one if the clock driving the first capacitor is high, and the clock driving the next capacitor is low. At the end of charge transfer a potential difference, equal to the threshold voltage of the MOST, is lost for every transistor. This threshold voltage increases if the source bulk voltage of the transistor increases due to the body effect. If the threshold equals the clock amplitude, the output voltage can not be increased by using more capacitors. Especially for low supply voltages this effect limits the maximum output voltage of the circuit.

Every capacitor C is booted up by the effective clock pulse V_ϕ' defined in equation (1). The output voltage is given in equation (2) and output resistance in equation (3). These equations are only valid if the clock cycle is long enough to transfer the charge from a capacitor to the next one.

$$V_\phi' = \frac{C}{C + C_{par}} V_\phi \qquad (1)$$

and C_{par} is parasitic capacitance between top plate of C and substrate.

$$V_{out} = V_{dd} + nV_{\phi}' - \frac{ni_{out}}{fC} - \sum_{i=1}^{n} V_{T_{Mi}} \qquad (2)$$

($V_{T_{Mi}} = V_T$ of transistor i; n= number of stages)

$$R_{out} = \frac{n}{fC} \qquad (3)$$

The disadvantage of the threshold voltage can be overcome by replacing the MOS diodes by switches (figure 1). The control of the switches requires a more complex clock circuit. If a low clock signal for a conducting switch is assumed, the clock scheme is given in figure 2. The output voltage for this circuit is equal to equation (2) without the threshold voltage term and the output resistance is given in equation (3).

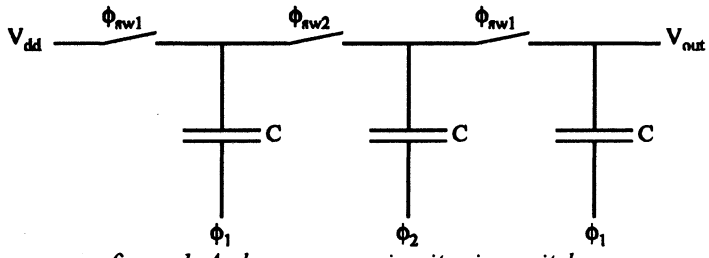

figure 1 A charge pump circuit using switches

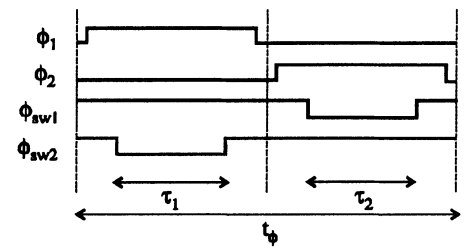

figure 2 Clock signals for a charge pump using switches

The switches have a non-zero on-resistance that influences the output resistance. Taking this into account the total output resistance is given in equation (4).

$$R_{out} = \frac{n}{fC}\coth\frac{\tau}{R_{on}C} \qquad (4)$$

$$R_{on} < \frac{2\tau}{3C} \qquad (5)$$

If the on-resistance meets the constraint of equation (5), the increase in the output resistance due to the on-resistance of the switch is less than 10%. For small values of R_{on} equation (4) is equal to equation (3) and the on-resistance has a negligible influence on the total output resistance of the circuit.

3 Implementation of the switches

The switches can be implemented by MOS transistors in their linear region. If, for simplicity, the threshold voltage is approximated by the linear function [4] described in equation (6) the on-resistance of a MOST in its linear region is given in equation (7). All the terminal voltages used in this equation are referred to the bulk of the MOST.

$$V_T = V_{T0} + \alpha V_s \text{ and } \alpha = \frac{C_{ox} + C_{dep}}{C_{ox}} \qquad (6)$$

$$R_{on} = \frac{1}{k\left(V_g - V_{T0} - \alpha V_{\overline{ds}}\right)} \text{ and } V_{\overline{ds}} = \frac{V_d + V_s}{2} \qquad (7)$$

We assume an N-well process where NMOS transistors are located in the substrate while PMOSTs are located in a separate N-Well. Both types of transistors need a bias circuit for the switches, if the amplitude of the switch clock is equal to the supply voltage. Umezawa *et al* [3] described a circuit using NMOS transistors as switches. The on-resistance of the switches increases for every switch in the chain, since the source-substrate potential increases and $V_{\overline{ds}}$ increases. This limits the output voltage to the same maximum value as the charge pump using MOS transistors as diodes. Since fewer stages are necessary to reach the maximum output value, the output resistance of this circuit is superior to the circuit using MOSTs as diodes.

If PMOS transistors are used, their N-wells have to be connected. To avoid substrate currents, the N-well potential has to be above the source and drain potential continuously. The capacitor voltage that is two nodes further in the chain can be used to bias the N-well. In figure 3 such a circuit is given. In this circuit also a biasing transistor M_b is drawn. This transistor keeps the gate-drain voltage of the switch transistor M_s equal to zero if the switch is in the off state. Note that the drain potential is above the source potential in the off state so the switch transistor is switched off for zero gate-drain voltage. During charge transfer the biasing transistor is switched off and the gate of the switch transistor is controlled by the switch clock. The maximum output voltage of this charge pump is not limited by an increasing threshold voltage, since the source-well potential remains constant. The output voltage can be increased by adding more capacitors to the chain until the breakdown voltage of the capacitors or the breakdown voltage of the N-well-substrate junction is reached.

The N-wells of the last two stages can not be biased according to the described method. For these stages two extra cells can be used only pumping the wells. Since these extra cells do not have to deliver a current, the N-well of these cells can be connected to the drain of the switch transistor. The capacitors of these extra cells can be small and extra area consumption is small. The gate of the bias transistor of the first stage can not be connected to the input of the first cell (in this case the supply voltage). If this gate is connected to ϕ_2, the biasing is correct.

The complete charge pump is given in figure 4. Cell 4 is not connected to a main clock, but to ground, so the output voltage is not pulsed. The open circuit output voltage is four times V_{DD}. If a higher output voltage is required, more cells can be added before cell 1. The parasitic capacitance between the top plate of the capacitor and the substrate is mainly caused be the capacitance between the N-well, that contains both transistors of the cell, and the substrate. This capacitance has to be minimised for a maximal output voltage. Using equation (5) the minimal dimensions for the switch transistor and the N-well can be determined.

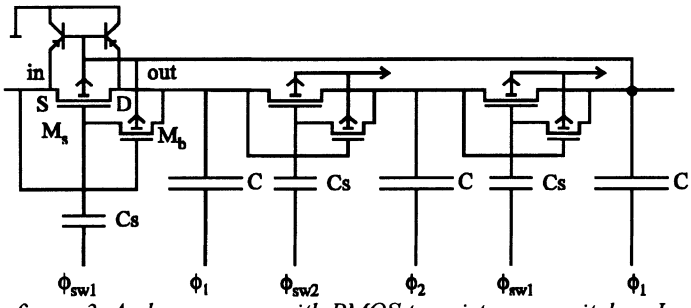

figure 3 A charge pump with PMOS transistors as switches. In the first cell the parasitic PNP transistors are shown.

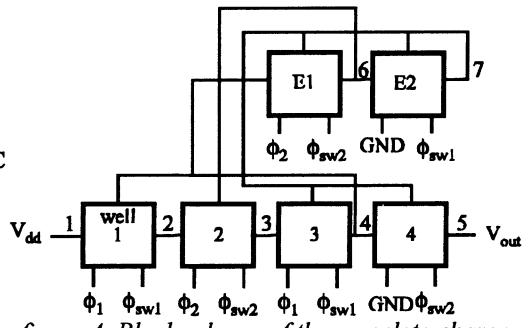

figure 4 Block scheme of the complete charge pump

4 Start up of the circuit

An analytical expression for the start up behaviour of a charge pump using discrete diodes is given by Di Cataldo *et al.* [5]. This does not include the effects of the parasitic transistors. If all the clocks are disabled, the circuit is a chain of diodes formed by the sources of the switches and the N-wells. The potential of the N-wells will approach the supply voltage due to the diode currents. If the clocks are enabled, Φ_1 becomes high and boots up nodes 2 and 4 (see figure 4). The PNP transistors under the source (see figure 3) of cells 2, 4 and E1 are forward biased and the basis current charges the nodes 3, 5 and 6. The current causes an increase of the basis potential and a decrease of the emitter potential, so the transistor currents decrease. If Φ_{sw2} becomes low the basis emitter junctions are shorted and the transistor currents are cut off. A high level of Φ_2 boots up nodes 4 and 6. The PNP transistors under the source of cells 3 and E2 are activated, until Φ_{sw1} becomes low. The collector current of the PNP transistors flows into the substrate and this charge can not be used to built up the high voltage. The substrate current is a majority carrier current so the latch-up risk is small.

At the beginning of the next clock cycle, the potential of every node is equal or higher than the previous node. The wells of the switches are at a higher potential than the sources and drains, thus the forward emitter basis voltages of the PNP transistors are smaller in this cycle compared to the first cycle. Simulations, incorporating the PNP transistors, showed that the well potentials are always above the source potentials of the switches in every cell, after four clock cycles. The PNP transistors are not active from this moment and no substrate current is lost in the substrate.

5 Measurement results

The circuit of figure 4 has been realised in the 2.5 μm CMOS process of the MESA Research Institute. The charge pump circuit had been specified to deliver 100 μA and 14 V using a 5 V supply voltage and clock amplitude. The maximum clock frequency was 5 MHz. The capacitance C was chosen 10 pF. According to equation (3) the output resistance was 60 kΩ and the circuit could meet the specifications. The switch time τ was 40 ns. The on resistance of the switches was determined by equation (5) to 2 kΩ, which leads, according to equation (7), to a W/L ratio of 10 for the switch transistors. The switch capacitors C_s were 0.2 pF. This value is a compromise between a large voltage swing on the gate of the switch and area consumption. The

well-substrate capacitance is less than 10% of the capacitance value C for zero bias. This capacitance decreases for an increasing bias voltage and the capacitances in the end of the chain are even smaller.

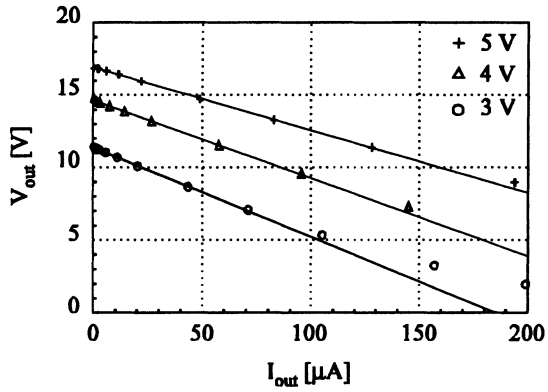

figure 5 Measured output voltage vs. output current for different clock voltages

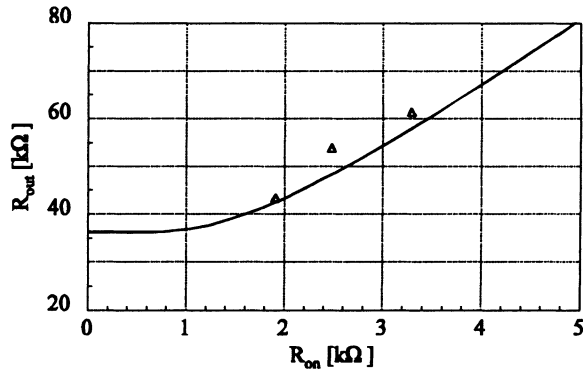

figure 6 Output resistance vs. switch on-resistance (line = calculated, triangles = measured).

Measurements on separate capacitances showed a value of 16.6 pF for the capacitor. This increase was caused by a change of the process after the design of the circuit

In figure 5 the output voltage of the charge pump circuit is given for different supply voltages and clock amplitudes at a clock frequency of 5 MHz. The figure shows that the circuit operates at 3 V.

The output resistance of the charge pump is calculated for the three measurement series in figure 5. The switch on-resistance has been determined from measurements on separate transistors. Figure 6 shows the output resistance of the circuit as a function of the switch-on resistances. In the figure also calculations according to equation (4) are shown.

Figure 7 shows the start up behaviour of the charge pump. The circuit load was 1 MΩ//6.5 pF for the upper curve and 91 kΩ//6.5 pF for the lower curve. In the latter case the chargepump delivers 85 μA in the steady-state condition.

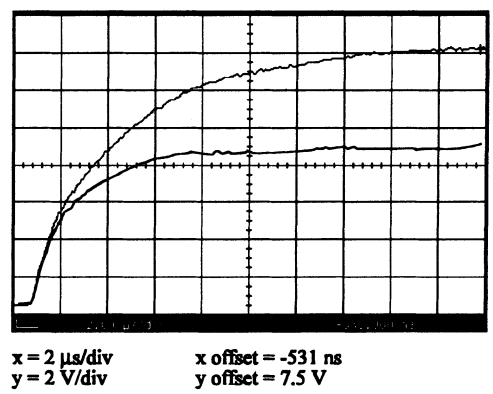

figure 7 Start up of the charge pump for a 1 MΩ and 91 kΩ load

6 Conclusions

A charge pump circuit has been developed that can deliver high currents even from 3 V system supply voltages. The maximum output voltage is not determined by the electrical parameters of the MOS transistors, but by breakdown voltages. This circuit has been analysed and measurements have been performed. The analysis and measurements showed a good matching.

Acknowledgements

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