Analysis and Design of a Family of Low-Power Class AB Operational Amplifiers

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Abstract

A new class AB output stage is presented which extends a family of recently proposed stages based on current mirrors without requiring extra-compensation capacitances. In-depth circuit analysis also shows the significant advantage of such stages for low-power consumption and leads to the derivation of an optimum design strategy. Experimental realizations are described, in particular a micropower amplifier for cardiac pacemaker application.

1. Introduction

This paper deals with the design and application of a family of low-power class AB operational amplifiers.

The initial goal of this work was to design an amplifier for battery-powered implantable medical devices, such as cardiac pacemakers. The whole system is supposed to consume not more than a few microamperes so that the battery may last several years. Therefore, operational amplifiers with minimum current consumption (below 1 microampere) are essential. Class AB amplifiers contribute to minimize power, particularly when the signal to be processed, as in this case the cardiac signal, is "active" during only a small part of the system cycle.

General constraints for this kind of application are detailed next. The nominal voltage of the Lithium-Iodine battery is 2.8V, but the system must be operative downto 2V. The selected quiescent current control mechanism must therefore be insensitive to supply voltage variations.

Although conceived in this framework, the proposed circuit architecture is analyzed in a general way, and we present various realizations reaching transition frequencies up to 10MHz, in a micropower 2µm CMOS on SOI technology.

The paper is organized as follows. Section 2 presents the circuit architecture, its principle of operation, the reduction in consumption it allows, and stability criteria for its design. Section 3 considers a method to synthesize the circuit aiming at minimizing power consumption. The experimental results are presented in Section 4 and compared with recently reported circuits. In Section 5 we summarize the main conclusions.

2. Circuit architecture

Our family of class AB output stages is presented in Fig. 1 considering two almost equivalent topologies. During the development of this work two groups reported the application of the architecture shown in Fig. 1.b [1], [2]. In these works however stability criteria were not explicited and designs did not exploit the principle proposed here, which allows to reduce the power consumption.

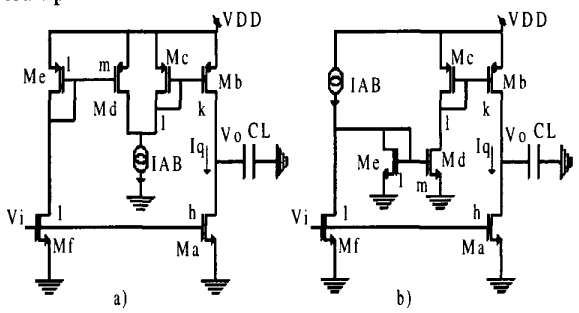

Figure 1. Class AB output stages.

Class AB operation is achieved after splitting the signal to the output on one hand by the output transistor

Ma and on the other hand by transistor Mf and current mirrors Me - Md and Mc - Mb. When Ma-Mf are n-MOS transistors, b-type architecture may be preferable to avoid the use of two p-MOS current mirrors as in Fig. 1.a. On the other hand, the new a-type architecture we propose here may be superior when Ma is to be p-MOS. The quiescent current control is based on the current comparison performed at the node where the I_{AB} current source is connected. In quiescent conditions the output current at the Vo terminal is zero and the output branch quiescent current (Iq in Fig. 1) must be such that the sum of the scaled versions of Iq at Mc and Md is equal to I_{AB}. This condition yields:

(1)

$$Iq_{a)} = \frac{k.I_{AB}}{1+\frac{k.m}{h}} \qquad Iq_{b)} = \frac{k.mI_{AB}}{1+\frac{k.m}{h}}$$

for Fig. 1a) and 1b) respectively, where h, k and m are the current mirrors gain factors shown in Fig. 1.

The ac behavior of this stage presents some interesting characteristics. The current mirrors provide a low impedance signal path to the output. On the contrary to well-known class AB output stages [4], this fact allows to avoid extra compensating capacitances in the output stage, provided the current mirrors frequency response is taken into account and circuit stability is guaranteed by adequate design. Furthermore, as we show in the next paragraphs, we can exploit the current mirrors gain to boost the transconductance of the stage and reduce consumption for a given bandwidth and phase margin.

The total equivalent transconductance of this stage under class AB operation, defined as the ratio between the total signal output current i_o and the input signal voltage v_i is given by Eq. (2).

(2)

$$gm = gm_a(1+\frac{km}{h})D(s)$$

where gm_a is the transconductance of the output transistor, Ma and D(s) represent the contribution of the frequency response of the current mirrors. Although, as will be discussed later, these may introduce high frequency doublets, the circuit can be properly stabilized even if the stage transconductance is multiplied by factors as high as 25. It is also interesting to consider the effect on the transconductance to consumed current ratio (g_m/I_D) of the stage, which can be used as guiding parameter in the design and is a figure of merit for the stage [3]. It is given by Eq. (3a) and (3b) for circuit 1a) and 1b) respectively.

(3a)

$$(gm/I_D) = (gm/I_D)_a \cdot \frac{(1+\frac{km}{h})}{(1+\frac{1}{k}+\frac{m}{h}+\frac{1}{h})} D(s)$$

(3b)

$$(gm/I_D) = (gm/I_D)_a \cdot \frac{(1+\frac{km}{h})}{(1+\frac{1}{k}+\frac{1}{km}+\frac{1}{h})} D(s)$$

In this case multiplication factors as high as 12 can be achieved.

Let us now consider the influence of the current mirrors response. The D(s) factor is given by Eq. (4). The factor (1+km/h) that multiplies the transconductance in Eq. (2) is noted by *gmmult*, while w_c(resp. w_e) is the angular frequency of the pole of the current mirror Mb-Mc (resp. Md-Me). The latter is given by the ratio of the Mc (Me) transconductance over the total capacitance at the Mc (Me) gate node.

(4)

$$D(s) = \frac{1+\left(\frac{1}{w_e}+\frac{1}{w_c}\right)\frac{s}{gmmult}+\frac{1}{w_e w_c}\frac{s^2}{gmmult}}{\left(1+\frac{s}{w_e}\right)\left(1+\frac{s}{w_c}\right)}$$

The doublet introduces an important phase shift near the w_c and w_e frequencies. This phase shift increases with *gmmult* and sets maximum values for the *gmmult* factor. Next section shows the method applied to determine the optimum solution.

Let us now summarize the factors that determine the achievable total consumption reduction. Consider we apply this output stage as the output stage of a Miller amplifier, since the op amp non dominant pole is proportional to the output stage transconductance, we will be decreasing the output stage current in a proportion comparable to the increase in the output stage g_m/I_D ratio, when compared to the equivalent class A amplifier. The increase in g_m/I_D is not completely translated into a decrease in current, because the non dominant pole must be slightly increased with respect to the class A case to have the same phase margin while allowing the phase shift introduced by the doublets. Taking this factors into account, reductions of quiescent current of 3 to 4 times with respect to the class A case are achievable.

3. Design for minimum power consumption

This section presents the design method of a Miller amplifier with the described output stage and a R-C compensation network. The schematic diagram of the

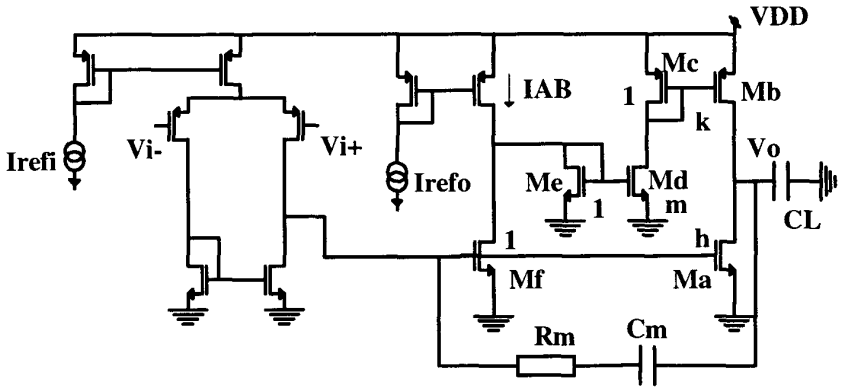

Figure 2. Schematic diagram of the class AB amplifier

amplifier is shown in Fig. 2. The R-C network eliminates the right half plane zero of the Miller amplifier allowing to reduce the overall consumption, by further decreasing the requirements on the output stage transconductance.

In what follows we will first present a method to select the current mirrors gain factors in order to guarantee a given phase margin, while achieving a maximum reduction in quiescent current with respect to a class A implementation.

The phase margin is determined by the position of the non dominant pole with respect to the transition frequency of the amplifier and the current mirrors frequency response, which as shown in Eq. (4) depends only on the poles frequency and the mirrors gain (through *gmmult*). Let us express this relationship by Eq. (5):

(5)

$$PM = f\left(w_{ndp}/w_T, w_e, w_c, k, h, m\right)$$

The non dominant pole of the Miller amplifier is given by Eq. (6):

(6)

$$w_{ndp} = \frac{g_{mo}}{\frac{C_1 C_L}{C_m} + C_L + C_1} \cong \frac{g_{mo}}{\left(\frac{C_1}{C_m} + 1\right) C_L}$$

where g_{mo} is the output stage transconductance, C_m is the Miller compensating capacitance, C_1 is the parasitic capacitance at the input of the output stage and C_L is the load capacitance.

The selection of the k,h and m parameters affect the amplifier phase margin because of their influence on both the non dominant pole (through their effect on g_{mo}) and the current mirrors frequency response. They also change the total quiescent current of the output stage. We now describe how the optimum solution to these trade-offs was found.

First we derived simplified approximate analytical expressions for the current mirrors poles. The main goal is to allow to decouple different steps of the synthesis procedure like the selection of k,h and m, the sizing of the first stage transistors and the determination of the Miller capacitance that otherwise should be carried out through a more complex iterative process. These expressions are based on the following assumptions:

a) the parasitic capacitance at the input of the second stage C_1 is approximately given by the gate capacitance of Ma and Mf. It is supposed to be negligible with respect to the Miller capacitance C_m.

b) the gate capacitances also dominate in the parasitic capacitances that define the current mirrors poles (reasonable hypothesis when the current mirror factor is larger than 1).

These assumptions are valid in the amplifiers under consideration and are even more appropriate in the case of SOI technology than in Bulk CMOS technology, due to the lower drain-substrate capacitances.

For the sake of simplicity in the illustration of the procedure we will also suppose transistors Mc, Me and Mf to be minimum sized transistors and the rest of the output transistors being of minimum length (which is usually the case).

Under these conditions, applying Eq. (6) and the strong inversion approximation for gate capacitances, the current mirrors poles in structure 1b) are given by Eqs (7a) and (7b). Analog expressions can be derived for the circuit of Fig. 1a).

(7a)

$$w_c = \frac{g_{mc}}{C_c} = \frac{g_{mo}}{\underbrace{C_L}_{w_{ndp}}} \frac{\left(g_m/I_D\right)_c}{\left(g_m/I_D\right)_a} \frac{1}{k.gmmult} \frac{C_L}{C_1} \frac{(h+1)}{(k+1)}$$

(7b)

$$w_e = \frac{g_{me}}{C_e} = \underbrace{\frac{C_L}{g_{mo}}\left(\frac{g_m}{I_D}\right)_a}_{w_{ndp}} \frac{1}{k.m.gmmult} \frac{C_L}{C_1} \frac{(h+1)}{(m+1)} \left(\frac{g_m}{I_D}\right)_e$$

where $(g_m/I_D)_i$ is the transconductance over current ratio for transistor i (with i = a, e, c). The $(g_m/I_D)_i$ values are chosen a priori by the designer based on considerations such as transition frequency and output current. Therefrom, considering equations (5), (7a) and 7(b) we have a set of equations with the unknowns k, h, m and w_{ndp}/w_T. We then find, with the aid of an optimization program, the set of values which results in a given phase margin value while minimizing the ratio I_A/I_{AB} where I_A is the consumption of a class A output stage with the same phase margin and I_{AB} is the total quiescent current consumption of the class AB output stage.

4. Experimental implementations

Three amplifiers, with the architecture shown in Fig. 2, were designed and fabricated in a thin film CMOS on SOI process.

The measured main performances of these amplifiers are summarized in Table 1. The data included are: total quiescent current (I_{DD}), transition frequency (f_T), load capacitance (C_L), phase margin (PM), DC open loop gain (A0), current mirrors factors k, h and m, output stage quiescent current reduction with respect to equivalent class A circuit (I_A/I_{AB}); the transition frequency divided by the total quiescent power (GHz/W) as a figure of merit of power efficiency as suggested in [5] and the minimum channel length used (L_{min}). All data are given considering a 2V supply voltage.

Amplifier A1 is intended for application in cardiac pacemakers as a 70Hz to 200Hz bandpass R-C filter that amplifies and processes the cardiac signal to detect whether the heart has spontaneously contracted, in which case stimulation is not necessary.

In order to minimize consumption amplifier A1 was designed to have 60° phase margin with closed loop gain of 18. The GHz/W figure of merit of this amplifier is calculated using the 3dB cut off frequency of this closed loop configuration, instead of the transition frequency.

Amplifiers A2 and A3 have typical characteristics required in many systems and their performances are compared in Table 2 and 3 with other similar amplifiers recently reported. In the first row of these tables, the technology used for the amplifier is shown.

Table 2 and Table 3 show the advantage of the proposed architecture for low-power applications, especially in terms of significantly increased frequency/power (GHz/W) ratios. Amplifiers A2 and A3 have lower, though acceptable, DC gain due to the low load resistance considered, but when considered with a purely capacitive load (as amplifiers [1] and [7]), the resulting gain is about 100 dB for A2 and 86 dB for A3.

Table 1. Amplifiers measurement data

	A1	A2	A3
I_{DD}	96nA	35µA	132µA
f_T	11.5kHz(1)	1.2MHz	10MHz
C_L	50p	15p	13p
PM(°)	56	53	55
A0 (dB) (@ $R_L(\Omega)$) (2)	80 @ 7M > 100 @ ∞	76 @ 10k 100 @ ∞	68 @ 10k 86 @ ∞
k,h,m	7,2,3	8,1,3	2,2,6
(I_A/I_{AB})	3.1	1.6	1.5
GHz/W	59	17	38
L_{min}(µm)	3	3	2

(1) 3dB frequency at closed loop gain of 18
(2) expected values

Table 2. Amplifier A2 comparison.

	A2	[1]	[6]	[7]
Techno.	SOI 3µm	SOI 2.4µm	Bulk 2µm	Bulk 0.7µm
V_{DD} (V)	2	10	2	1.5
I_{DD} (µA)	35	60	700	307
R_L/C_L	10k/15p	50p	10k/20p	15p
A0 (dB)	76	100	100	84
f_T (MHz)	1.2	1.2	1	1.3
GHz/W	17	2	0.7	2.8

Table 3. Amplifier A3 comparison.

	A3	[2]	[8]	[8]
Techno.	SOI 2µm	BiCMOS	Bulk 1.6µm	Bulk 1.6µ m
V_{DD} (V)	2	1	1.8	1.8
I_{DD} (µA)	132	1200	180	221
R_L/C_L	10k/13p	10k	10k/5p	10k/5p
A0 (dB)	68	110	88	90
f_T (MHz)	10	4.5	5	5.8
GHz/W	38	3.8	15.4	14.6

The measured total harmonic distortion for amplifier A1 with a 60 Hz fundamental, closed loop gain of 21 and 1.87Vpeak to peak output voltage is 0.5%. This result shows that although distortion might be a concern due to

the asymmetric output stage, reasonable values are achieved.

5. Conclusions

A new design approach for a recent family of low-power class AB output stage has been presented. The current consumption is reduced by increasing the output stage transconductance to current ratio by exploiting current gain through current mirrors. An analytical procedure to determine the gain of the current mirrors that provides the maximum reduction in consumption while preserving stability has been presented. Significant reductions of the output stage quiescent current by factors up to 3 or 4 with respect to the class A output stage are achieved, implying only a small increase in complexity. The comparison with other recently reported amplifiers show the advantages of this approach when power consumption is a primary concern.

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