Analysis and Design of a Forward-Flyback Converter Employing Two Transformers

Yonghan Kang , Byungcho Choi, and Wonseok Lim

School of Electronic and Electrical Engineering,
Kyungpook National University,
1370, Sankyuk-Dong, Buk-Gu, Taegu, 702-701, Korea

Abstract – This paper presents the steady-state analysis and design of a forward-flyback converter that employs two transformers and an output inductor. By utilizing two separate transformers, the proposed converter allows a low-profile design to be readily implemented while retaining the merits of a conventional single-transformer forward-flyback converter with secondary center tap. By using an output inductor, the proposed converter efficiently reduces the output ripple to an acceptable level. The design and performance of the proposed converter are confirmed with experiments on a 100 W prototype converter.

I. Introduction

Recently, telecommunication and data-communication industries have placed more demanding requirements on the power supplies in order to increase the functional density and decrease the equipment cost. The on-board power supplies for telecommunication electronics should be implemented in a low-profile design while complying with stringent specifications for the efficiency and power density. To cope with these challenges, many advanced converter topologies have been proposed by the researchers [1-9]. Among these, the forward-flyback converter has been considered as one of promising candidates for the on-board dc-to-dc converters for telecommunication electronics. The forward-flyback converter features with a secondary-side circuit that is well suited for an efficient delivery of a high current with small ripple component. In addition, the forward-flyback converter has an inherent zero voltage switching (ZVS) capability due to an asymmetrical operation [10]. However, the copper loss in the primary side of this converter can be large because the operation of the converter during the flyback-mode is supported by the large dc magnetizing current of its transformer.

As a practical solution to reduce the primary-side copper loss of the forward-flyback converter, two separate transformer can be employed [4] as a substitute for a single conventional transformer with a center tap [1,2]. The use of two separate transformers offers following advantages. First, the turns of primary transformer winding is reduced to half of a conventional forward-flyback converter with a single transformer, thereby reducing the primary copper loss. Secondly, the use of two separate transformers enables the smaller low-profile cores to be utilized, thereby facilitating a low-profile design. Finally, while one of two transformers works as a normal transformer, the other transformer in effect functions as an output inductor. This implies that the output inductor of a forward-flyback converter can be removed if two transformers are used. Indeed, a two-transformer forward-flyback converter presented in [4] does not use any output inductor. However, this paper will demonstrate that this approach may not satisfactory to the practical low-profile on-board converters in which the magnetizing inductor of the transformer is commonly not large enough.

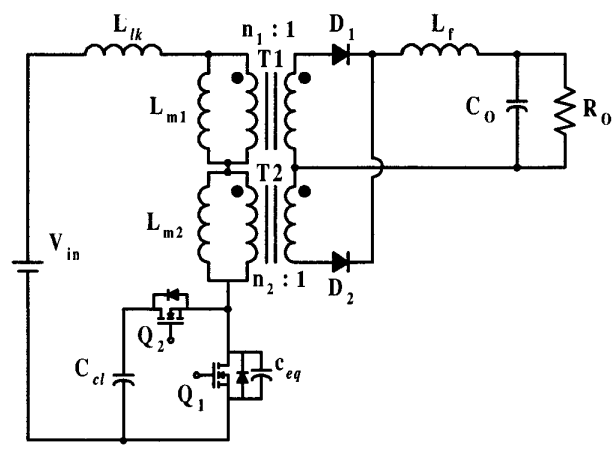

Fig. 1 Forward-flyback converter with two transformers.

This paper presents a forward-flyback converter that could retain the advantage of the existing topology [4] while overcoming its shortcoming. Fig. 1 shows the circuit diagram of the proposed forward-flyback converter. The converter employs two transformers as practiced in [4], yet it contains an additional output filter inductor L_f . As will be demonstrated in this paper, the output filter plays a critical role in reducing the output current ripple to an acceptable level.

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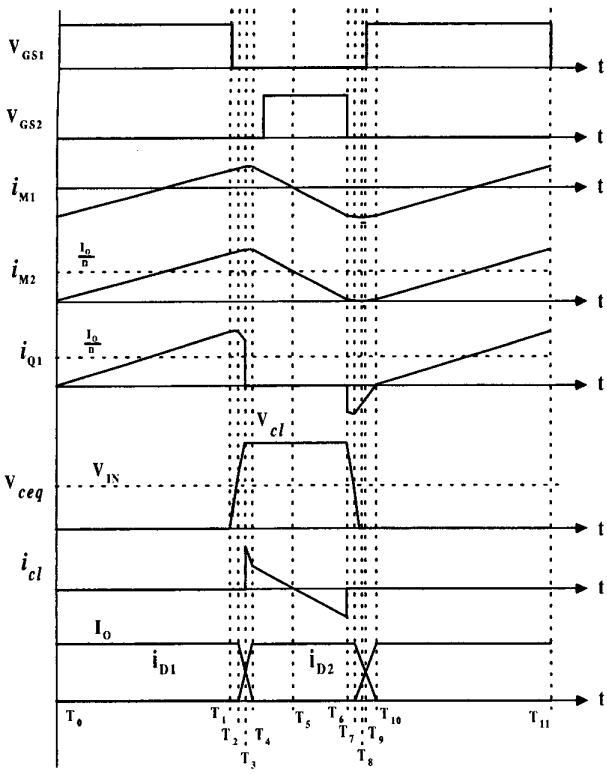


Fig. 2 Key waveforms of proposed converter.

II. STEADY-STATE ANALYSIS

The key waveforms of the proposed converter are illustrated in Fig. 2. The following assumptions are made to simplify the analysis:

- The filter inductor, L_f, the clamp capacitor, C_{cl}, and the output capacitor, C_o, are sufficiently large that the current through L_f, i_{Lf}, the voltage across C_{cl}, V_{cl}, and the voltage across C_o, V_o, can be considered as a constant.
- The magnetizing inductances, $L_{mi}\,(i=1,2)$, and turns ratios, $n_i\,(i=1,2)$, of two transformers are identical.
- All leakage inductances are reflected to the primary side.
- The leakage inductance, L_{lk}, is much smaller than the magnetizing inductance. The C_{eq} appearing across Q_1 in Fig. 1 is a sum of the output capacitors of the switches, Q_1 and Q_2, the parasitic capacitors of the transformers, and the junction capacitors of the secondary-side diodes.

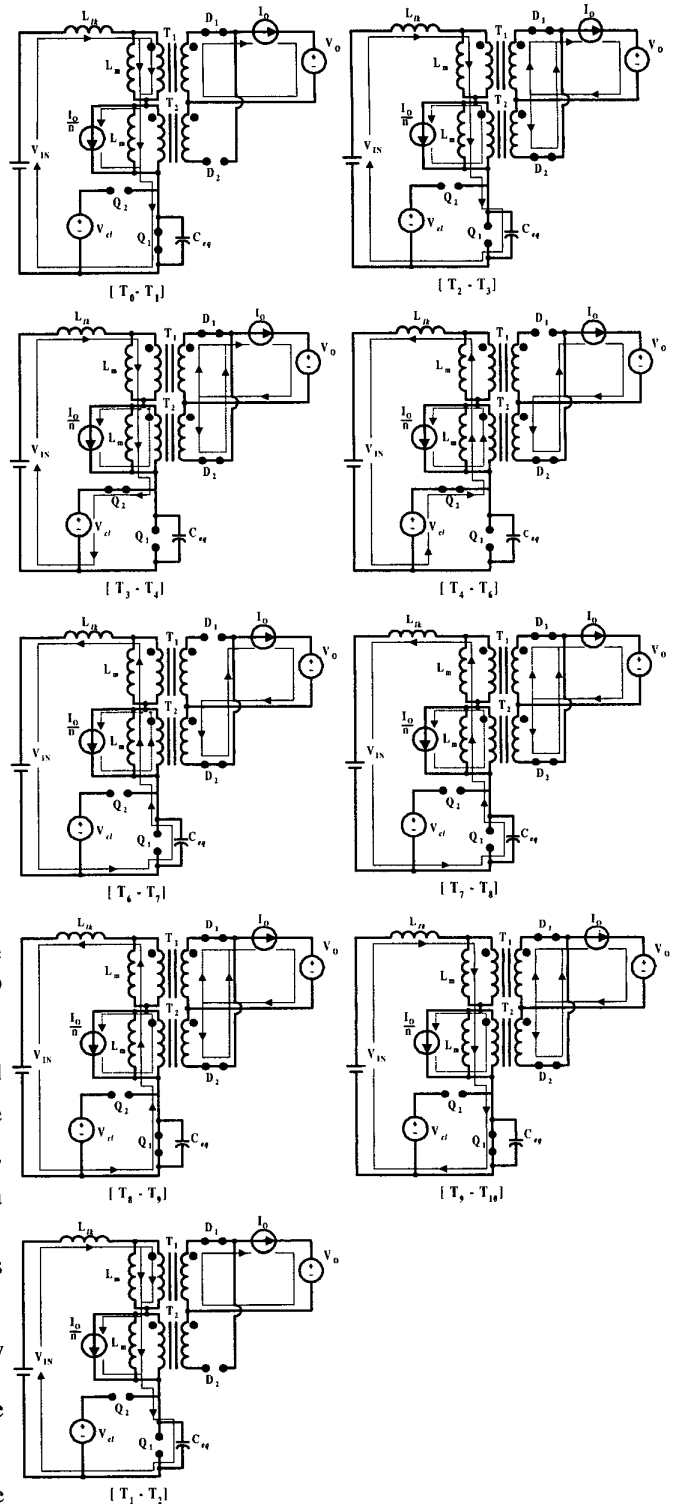


Fig. 3 Topological stages of proposed converter.

Fig. 3 shows the topological stages of the proposed converter. Referring to Figs. 1 through 3, the steady-state operation of the proposed converter is explained as follows:

A. Period $[T_o, T_1]$- The main switch, Q_1, turns on and it delivers the sum of the reflected secondary current and the magnetizing current i_m:

$$i_{Q1} = \frac{I_o}{n} + i_m = \frac{I_o}{n} + \frac{V_{in}}{2L_m}(t - T_o). \quad (1)$$

The transformer, $\mathbf{T_1}$, functions as a normal transformer and transfers the energy from the primary side to the secondary side. During this period, the transformer, $\mathbf{T_2}$, operates as an inductor and supports the reflected secondary current. Fig. 4(a) shows a simplified circuit diagram of the power stage in which the magnetizing inductance and input voltage are reflected to the secondary side. The reflected magnetizing inductor and the output inductor collectively work as a filter inductor, thereby reducing the current ripple efficiently.

B. Period $[T_1, T_2]$- The switch Q_1 turns off at T_1 and the voltage across the equivalent output capacitor, V_{Ceq}, increases almost linearly up to the input voltage, V_{in}, by a charging current of:

$$i_{Ceq} \cong \frac{I_o}{n} + i_m(T_1). \quad (2)$$

When V_{Ceq} reaches the input voltage, the secondary-side diode, D_2, starts conducting.

C. Period $[T_2, T_3]$- In this period, the leakage inductance, L_{lk}, resonates with the equivalent output capacitor C_{eq}. Accordingly, the leakage inductance current, i_{Llk}, decreases in a resonant manner:

$$i_{Llk} = \left(\frac{I_o}{n}\right) + \frac{\Delta i_m}{2} cos[\omega_r(t - T_2)] \quad (3)$$

where Δi_m denotes the peak-to-peak value of the ac magnetizing current and $\omega_r = \frac{1}{\sqrt{L_{lk} C_{eq}}}$ is the resonant frequency. On the other hand, V_{Ceq} increases in a resonant fashion:

$$V_{Ceq} = V_{in} + Z_r\left(\frac{I_o}{n} + \frac{\Delta i_m}{2}\right) sin[\omega_r(t - T_2)] \quad (4)$$

where $Z_r = \sqrt{\frac{L_{lk}}{C_{eq}}}$ is the characteristic impedance of the resonant circuit.

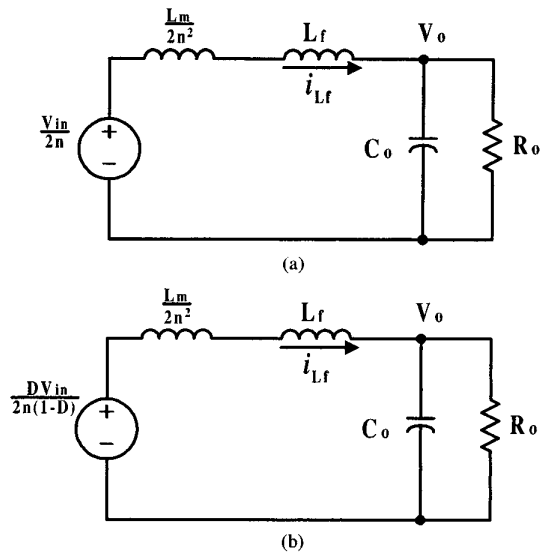


Fig. 4 Simplified circuits of power stage. (a) Main switch closed. (b) Clamp switch closed.

D. Period $[T_3, T_4]$- At T_3, the body diode of the clamp switch, Q_2, conducts and thus V_{Ceq} is clamped at V_{cl}. For a ZVS operation, the switch Q_2 should be turned on between T_3 and T_5. The leakage inductance current decreases with the slope of $\frac{V_{cl} - V_{in}}{L_{lk}}$.

E. Period $[T_4, T_6]$- The secondary side diode D_1 turns off and D_2 conducts at T_4. The output current is supported by the dc magnetizing current of the transformer $\mathbf{T_2}$. During this period, the transformer $\mathbf{T_1}$ operates as an inductor, and carries the magnetizing current as shown in Fig. 3. The magnetizing current decreases with the slope of $\frac{V_{cl} - V_{in}}{2L_m}$. As shown in Fig. 4(b), the reflected magnetizing inductance of $\mathbf{T_1}$ assists to reduce the current ripple.

F. Period $[T_6, T_7]$- The switch Q_2 turns off at T_6 and C_{eq} is discharging linearly from V_{cl} to V_{in} by a nearly constant discharging current:

$$i_{Ceq} \cong -i_m(T_6). \quad (5)$$

G. Period $[T_7, T_8]$- At T_7, the rectifier diode D_1 starts conducting and the leakage inductance L_{lk} resonates with C_{eq}. The leakage inductance current i_{Llk} increases and V_{Ceq} decreases in a resonant manner:

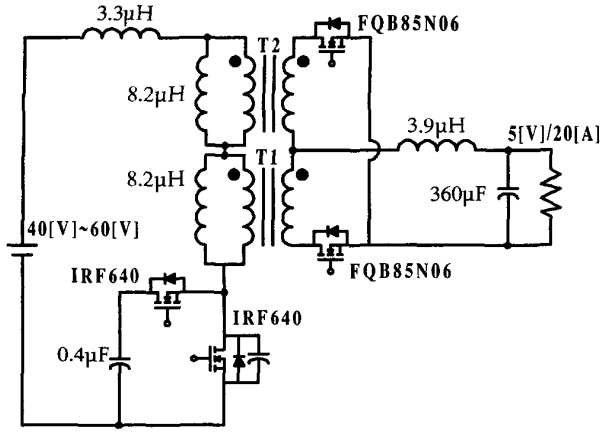


Fig. 5 Power stage parameters of prototype converter.

$$i_{Llk} = -\frac{\Delta i_m}{2} cos[\omega_r(t - T_7)] \quad (6)$$

$$V_{Ceq} = V_{in} - Z_r \frac{\Delta i_m}{2} sin[\omega_r(t - T_2)]. \quad (7)$$

This period terminates when V_{Ceq} reduces to zero and the body diode of Q_1 begins conducting.

H. Period $[T_8, T_9]$- The voltage V_{Ceq} remains zero, and both the leakage inductance current, i_{Llk}, and the switch current, i_{Q1}, increase with the slope of $\frac{V_{in}}{L_{lk}}$. The switch Q_1 should be turned on during this period to achieve a ZVS operation.

I. Period $[T_9, T_{10}]$- The switch current i_{Q1} becomes positive and flows through Q_1. At T_{10}, the rectifier diode D_1 carries the entire output current, and the diode D_2 turns off. The next switching cycle begins at the end of this period.

III. Design Example

In order to verify the performance of the proposed converter, a 100 W prototype converter was implemented with the following specifications:

- Input Voltage : 40 V – 60 V
- Output Voltage / Current : 5 V / 20 A
- Switching Frequency : 250 kHz .

A. Selection of switches and synchronous rectifiers

The power stage diagram of the prototype converter is shown in Fig. 5. For the given clamp circuit, the clamp voltage is determined as:

$$V_{cl} = \frac{V_{in}}{1 - D}. \quad (8)$$

One good approach to designing a converter with an active clamp circuit is to force the voltage stress at the minimum input voltage to be equal to the voltage stress at the maximum input voltage [9]. For the proposed converter, this design criterion implies:

$$V_{cl} = \frac{V_{in,min}}{(1 - D_{max})} = \frac{V_{in,max}}{(1 - D_{min})}. \quad (9)$$

The output voltage of the proposed converter is given by:

$$V_o = \frac{DV_{in}}{n} - V_F \quad (10)$$

where n represents the turns ratio of the transformers and V_F denotes the forward voltage drop of the schottky diode or the voltage drop at $R_{ds(on)}$ of the synchronous rectifier (SR). From (9) and (10), it is determined that D_{max} = 0.6 and D_{min} = 0.4 [9]. From (10), the turns ratio of the transformer is obtained as n = 4.5. From the selected turns ratio, the new maximum and minimum values of duty ratio are determined as D_{max} = 0.58 and D_{min} = 0.39. From (8), the clamp voltage is determined as $V_{cl,max}$ = 98 V and $V_{cl,min}$ = 96 V. It should be noticed that, during the conduction period of Q_2, the voltage across Q_1 can be increased by a voltage rise that appears across the clamp capacitor. The voltage rise is caused by the charging and discharging current in the clamp capacitor. Figs. 6(a) and (b) show the voltage and current waveforms of Q_1 and Q_2 measured at the nominal input voltage. As shown in Fig. 6(a), the voltage across Q_1 was measured at 8% above the clamp voltage. As shown in Fig. 6(b), the measured clamp voltage was increased about 33% over the theoretical value calculated at the nominal input voltage. The increase in the clamp voltage was caused by the fact that the actual duty ratio becomes larger than the theoretical value due to a substantial voltage drop across the large leakage inductance. The voltage stresses of the secondary-side diodes are determined as:

$$V_{D1,max} = \frac{V_{cl,min} - V_{in,min}}{n} \approx 12V \quad (11)$$

$$V_{D2,max} = \frac{V_{in,max}}{n} \approx 13V. \quad (12)$$

The measured voltage across SR was also larger than the calculated value due to the increased duty ratio.

B. Design of transformers

As shown in the steady-state analysis, $\mathbf{T_1}$ functions as a normal transformer while $\mathbf{T_2}$ works as a flyback transformer.

TABLE 1

Summary of Transformers and Output Filter Inductor Design

	Core		Turns	Wire	Air Gap	Inductance
T1 & T2	EFD2020	Primary	9Ts	AWG38×70	0.89mm	8.2μH
		Secondary	2Ts	0.11mm foil 2 strands		
L_f	MPP55350		5Ts	AWG38×200 2 strands		3.9μH

Therefore, the primary winding of $\mathbf{T_1}$ is determined as:

$$N_p = \frac{V_{in} D}{2\Delta B\, A_e f_s} \tag{13}$$

where ΔB denotes the flux excursion and A_e represents the cross-sectional area of the core. By choosing ΔB = 0.2 T and using EFD2020 core with A_e = 31mm^2, the number of the primary winding is determined as $N_p \geq 7.2$. From this result, the numbers of primary and secondary windings were selected as N_p = 9 Ts and N_s = 2 Ts. Since the transformer, $\mathbf{T_2}$, operates as a flyback transformer, it should have an air gap determined by:

$$W_g = \frac{A_e B_{max}}{2\mu_o}\left(l_g + \frac{l_e}{\mu_a}\right) = \frac{V_o I_{o,max}(1 - D_{min})}{\eta_{min} f_s} \tag{14}$$

where l_e is the length of the effective magnetic path and η_{min} is the estimated minimum efficiency. From the selected number of the primary winding, ΔB is determined as 0.16 T. With $B_{max} = \Delta B$ = 0.16 T and η_{min} = 0.85, the length of air gap is determined as 0.89 mm. The same air gap was placed inside $\mathbf{T_1}$ in order to force $\mathbf{T_1}$ and $\mathbf{T_2}$ to have the same magnetizing inductance. The design results of the transformers and output inductor are summarized in Table 1.

C. Selection of clamp capacitor

Two conditions should be considered in selecting the clamp capacitor. First, by using the condition that the half of the resonance period between the magnetizing inductance, L_m, and the clamp capacitor, C_{cl}, is much larger than the off-time of the main switch, the clamp capacitor, C_{cl}, is determined as:

$$C_{cl} \geq \frac{(1-D)^2}{2 L_m \pi^2 f_s^2} \ . \tag{15}$$

Secondly, during the time period in which the clamp switch is conducting, the voltage across the clamp switch has a rise due to the current through the clamp capacitor. For the proposed forward-flyback converter, it was found that the current through the clamp capacitor becomes nearly symmetrical. From these conditions, it follows:

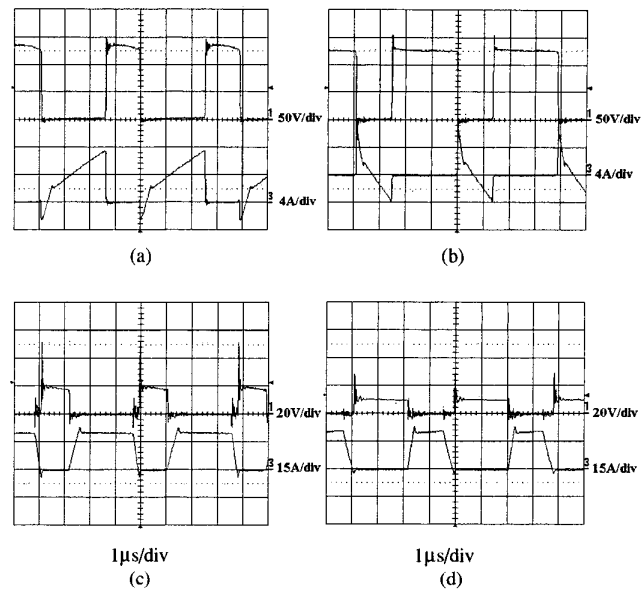


Fig. 6 Experimental voltage and current waveforms with Io =20 A. (a) Main switch. (b) Clamp switch. (c) Forward SR. (d) Flyback SR.

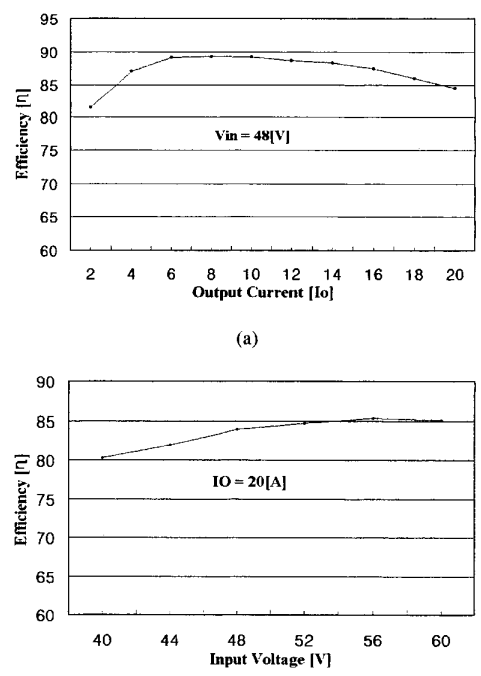
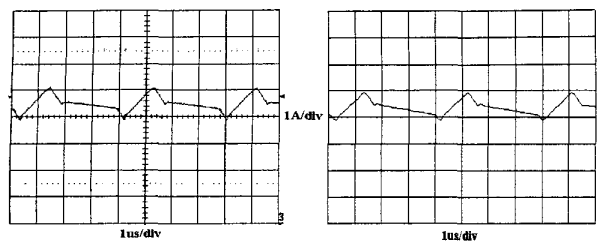


Fig. 7 Measured efficiency. (a) Vin = 48 V. (b) Io = 20 A.



(a) (b)

Fig. 8 Output current ripple of proposed converter. (a) Measurement. (b) Simulation.

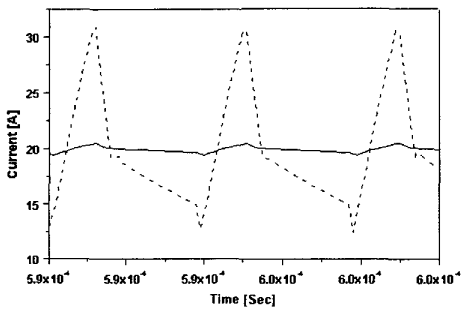


Fig. 9 Comparison of output current ripple. The solid line is the current ripple of the proposed converter and the dash line is that of the conventional converter presented in [4].

$$\frac{\Delta V_{cl}}{V_{cl}} \cong \frac{D(1-D)^2}{4 L_m C_{cl} f_s^2}. \tag{16}$$

From (16) with assumption of $\frac{\Delta V_{cl}}{V_{cl}} \leq 0.2$ and the condition of (15), the clamp capacitor is determined as $C_{cl} \geq$ 0.35μF.

As shown in Fig. 6(a), the prototype converter achieves a ZVS at the nominal input voltage with a full load condition. Figs. 6(c) and (d) show the voltage and current waveforms of SRs. The current through SRs exhibits a slow transient behavior due to the large leakage inductance. This slow response could increase the conduction loss at SRs. The efficiency of the prototype converter is shown in Fig. 7. At the full load condition, the maximum efficiency of 85.3% was measured with V_{in} = 56 V.

Fig. 8 shows the measured and simulated waveforms of the ripple component of the output current. The output current ripple is limited at 1A peak-to-peak value as shown in Fig. 8. Fig. 9 shows the output current of the prototype converter in comparison with that of a conventional forward-flyback converter presented in [4]. The conventional forward-flyback converter has the same power stage parameters as those used in the prototype converter except for the absence of the output inductor. As shown in Fig. 9, the conventional forward-flyback converter exhibits an excessive current ripple because the reflected magnetizing inductance of the transformer is too small to limit the current ripple at an adequate level. The prototype converter resolves this problem with a small output inductor.

IV. Conclusions

This paper presented the analysis and design of a forward-flyback converter that employs two separate transformers and an output inductor. The performance of the proposed converter was confirmed with experiments on a 100 W prototype converter. The efficiency was measured at the nominal input voltage with the different load condition. The maximum efficiency was measured at 40% of the full load. Also, under full load condition, the efficiency was measured for the entire input range. The maximum efficiency was 85.3%. It has been shown that, by using a small output inductor, the proposed converter readily overcomes the demerit of the conventional forward-flyback converter that relies on only the reflected magnetizing inductance of the transformer to control the current ripple.

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