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Analysis and Design of a Multi-Core Oscillator for Ultra-Low Phase Noise

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Abstract—In this paper, we exploit an idea of coupling multiple oscillators to reduce phase noise (PN) to beyond the limit of what has been practically achievable so far in a bulk CMOS technology. We then apply it to demonstrate for the first time an RF oscillator that meets the most stringent PN requirements of cellular basestation receivers while abiding by the process technology reliability rules. The oscillator is realized in digital 65-nm CMOS as a dual-core LC-tank oscillator based on a high-swing class-C topology. It is tunable within 4.07–4.91 GHz, while drawing 39–59 mA from a 2.15 V power supply. The measured PN is −146.7 dBc/Hz and −163.1 dBc/Hz at 3 MHz and 20 MHz offset, respectively, from a 4.07 GHz carrier, which makes it the lowest reported normalized PN of an integrated CMOS oscillator. Straightforward expressions for PN and interconnect resistance between the cores are derived and verified against circuit simulations and measurements. Analysis and simulations show that the interconnect resistance is not critical even with a 1% mismatch between the cores. This approach can be extended to a higher number of cores and achieve an arbitrary reduction in PN at the cost of the power and area.

Index Terms—Basestation (BTS), class-C oscillator, coupled oscillators, figure of merit (FoM), LC-tank, phase noise.

I. Introduction

RECEIVERS in cellular basestations (BTS) work in the presence of powerful unwanted blockers while being required to sense weak desired signals. To avoid distortion through reciprocal mixing, phase noise (PN) of BTS oscillators must satisfy extremely stringent performance requirements. Monolithic SiGe/Bi-CMOS technology, together with discrete external components, are used nowadays for such RF front-ends. However, due to power consumption and cost reasons, together with an increasing deployment, there is a strong motivation for their full monolithic integration in CMOS.

The stringent PN requirements originate from the in-band blocking characteristics imposed by the Global System for Mobile Communications "GSM900 normal basestation" [1]. Fig. 1 illustrates the worst case scenario when a blocker is present at 800 kHz away from the desired signal. The oscillator PN ($\mathcal{L}$) is integrated over the channel bandwidth, BW (here,
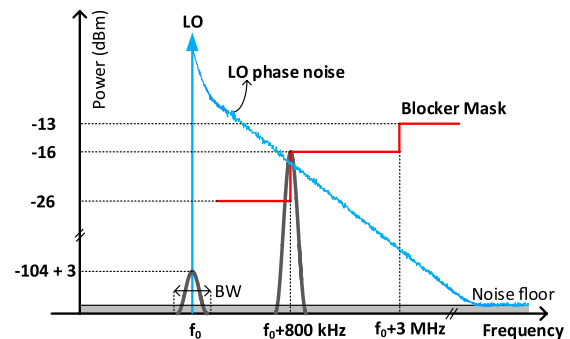
Fig. 1. Blocker levels in a GSM900 system as a function of offset frequency.

200 kHz), and mixed with the blocker of power P_b at 800 kHz away and then down-converted on top of the desired signal, P_s. In order to maintain the minimum carrier-to-interference ratio (C/I) of 9 dB set by the GSM standard [1], an oscillator must satisfy the strict PN according to

$$P_b + [\mathcal{L}(\Delta f) + 10 \log(BW)] < P_s - \left(\frac{C}{I}\right). \quad (1)$$

Per Fig. 1, $P_b = -16$ dBm and $P_s = -101$ dBm. Therefore, the PN at 800 kHz should satisfy -147 dBc/Hz, which is 20 dB lower than that required in mobile stations (MS) [1].

Extensive efforts [2]–[14] have been made to improve PN in CMOS oscillators while maintaining good figure-of-merit (FoM), i.e., normalized PN per 1 mW of power consumption

$$\text{FoM} = |\text{PN}| + 20 \log_{10}\left(\frac{f_0}{\Delta f}\right) - 10 \log_{10}\left(\frac{P_{\text{DC}}}{1 \text{ mW}}\right) \quad (2)$$

where f_0 is the oscillating frequency, Δf is the frequency offset from f_0, and P_{DC} is the power consumption. However, none of the prior works has managed to satisfy the toughest BTS phase noise specifications even given ample margin to the reasonably expected limit on power consumption (see the "current" and "FoM" entries in Table I). Furthermore, a recent work in [15] has established fundamental limits on the FoM performance of oscillators and has re-introduced a metric termed excess noise factor (ENF), something akin to a noise figure (NF) of an LNA. As it turns out, state-of-the-art oscillators are just a few dB away from that fundamental limit. Hence, the only realistic avenue for substantial PN performance improvements is to increase the power consumption P_{DC} while maintaining a good FoM. This appears to invariably lead to an increase in the oscillation amplitude V_{osc} of the resonating LC-tank according to (based on (2) in [4])

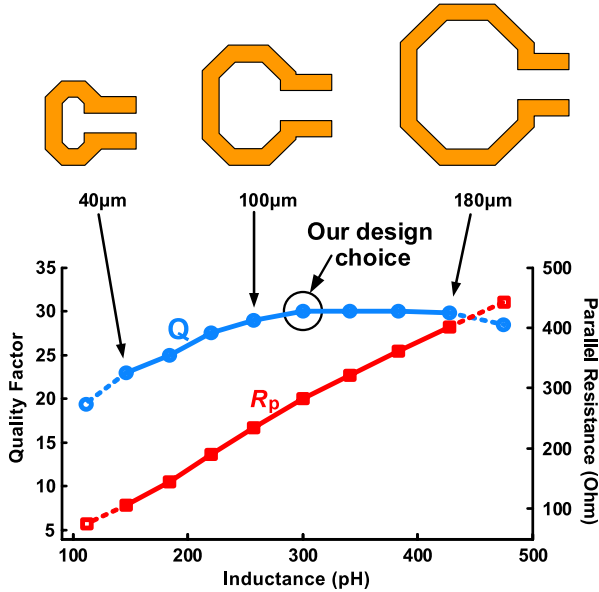$$V_{\text{osc}} = \sqrt{P_{\text{DC}} \cdot \alpha_I \cdot \alpha_V \cdot Q \cdot \omega_0 L} \quad (3)$$

Fig. 2. By continually reducing the inductor size (value), at some point Q-factor starts degrading.

where α_I and α_V are the current and voltage conversion efficiencies, Q is the tank's quality factor, $\omega_0 = 2\pi f_0$, and L is the tank inductance. α_I and α_V are largely fixed by the chosen oscillator topology.

For an optimal power consumption efficiency (i.e., FoM), Q should be kept as high as possible. Attempting to further improve the PN by increasing P_{DC} will result in large V_{osc}, which will eventually lead to serious device reliability concerns [4]. Hence, based on (3), a reasonable strategy in delivering more effective P_{DC} would be decreasing L while keeping V_{osc} at its maximum tolerated level. As pointed out later in Section II, there is a technological limitation on how low L can go. To conclude, each CMOS process seems to have a technological limitation on phase noise of a given oscillator topology (i.e., α_I and α_V).

In this paper, we propose to break that limit by a dual-core oscillator topology [16] and then demonstrate it in bulk CMOS. The rest of the paper is organized as follows. Section II presents a background discussion on various techniques to improve PN. Section III elaborates more on the multi-core oscillators. Section IV discusses the effect of different practical impairments in multi-core oscillator design and is followed by measurement results in Section V.

II. PHASE NOISE REDUCTION TECHNIQUES

A. Parameter Optimization

In 1966, Leeson presented an empirically derived PN ($\mathcal{L}$) model of oscillators [17]

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left(F \frac{4kTR_p}{V_{osc}^2} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right) \qquad (4)$$

where k is Boltzmann's constant, T is the absolute temperature, R_p is an equivalent parallel tank resistance, and F is a noise factor of the active device.

Leeson's equation shows the dependency of PN on Q. The inductor's Q-factor in bulk CMOS is limited in best case to 30, even with an ultra thick metal option. Furthermore, oscillators need to cover a certain tuning range ($> 15\%$) to account for variations in process, voltage and temperature (PVT). Such tuning is typically done with switched capacitors, which also have a limited Q-factor. In addition, there is a trade-off between the tuning range and Q of these switches. Consequently, the tank's Q does not have much margin left for further improving the PN in scaled CMOS.

Furthermore, advances in the CMOS technology lead to systematic reductions in the supply voltage, V_{DD}. Maximum practical voltage swing V_{osc} in the oscillator gets saturated to less than twice V_{DD}. Hence, the voltage scaling will directly lead to the PN degradation, as per (4). Moreover, FoM of the oscillator is also dependent on the voltage efficiency, $\alpha_V = V_{osc}/V_{DD}$, which tends to be degraded with supply scaling. It has been shown that [16]

$$\text{FoM} = \frac{4Q^2 \cdot \alpha_I}{F \cdot 4kT} \times \frac{V_{osc}}{V_{DD}} \times 10^{-3} \qquad (5)$$

where α_I is the current efficiency (conversion factor of the bias current into the fundamental current harmonic).

An important parameter is an inductance value, L, of the LC-tank. Equation (5) is written such that FoM does not depend *directly* on L. However, L affects the equivalent parallel resistance of the tank as $R_p = L\omega Q$. By decreasing L and, consequently, R_p (while managing to keep Q constant), PN can be reduced, as per (4). However, the bias current should be increased to keep the maximum oscillation amplitude with, hopefully, a constant FoM.

To maximally reduce the PN, one might pick a high-Q inductor at first and then try to lower the inductance by shrinking its radius or reducing its number of turns. Although a multi-turn inductor might have a slightly higher quality factor, by choosing a 1-turn inductor, a much lower inductance value can be obtained. Reducing the radius of an inductor results in a lower inductance (see Fig. 2). However, after a certain point, the quality factor starts dropping dramatically as series resistance losses (e.g., due to vias, interconnecting metal) start to dominate. By trading off between a low L and high Q, we can find the optimum point from which further increasing the inductance would worsen the PN, but lowering the inductance would drop Q and thus worsen FoM and perhaps even PN. At that point, the oscillator could have the lowest possible PN in a given process technology with a good FoM. In other words, to improve the PN of the oscillator, the term $R_p/Q^2 = L\omega/Q$ from (4) needs to be reduced. From Fig. 2, this ratio cannot keep on decreasing indefinitely since at certain point Q drops more than L. Moreover, there is a limit on how small the inductor can become before it gets limited by vias and other fixed routing parasitics.

B. High-Swing Class-C Topology

Based on Leeson's equation, another parameter that can be exploited to improve PN is F (i.e., amplifier's noise factor).
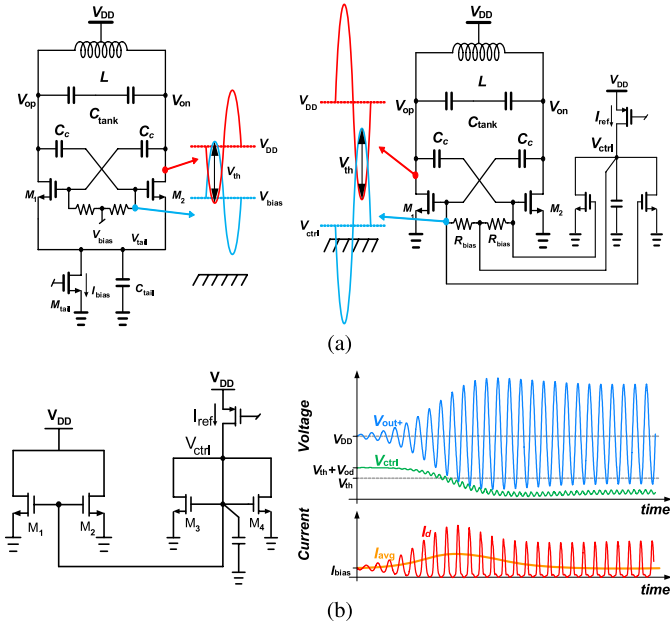
Fig. 3. Schematic of the original class-C oscillator (left), and high-swing class-C (HSCC) oscillator used in this work (right); (b) conceptual diagram of DC biasing and related start-up waveforms.
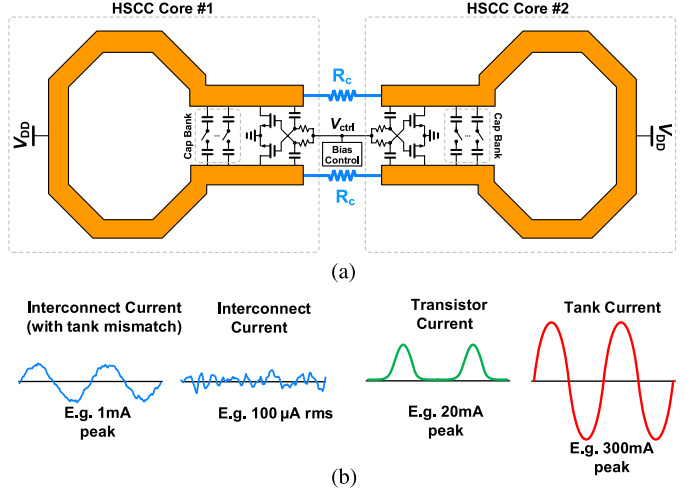

Fig. 4. (a) Dual-core high-swing class-C (HSCC) oscillator, and (b) related current waveforms. Note the internal LC-tank current is Q times larger than the oscillator drain current, I_{DC}.

There are a number of efforts to reduce F by shaping the tank voltage and reducing the effective noise of active devices [2]–[4], [11].

A class-C oscillator was first introduced in [11] and, according to [15], its ENF is very competitive. Its schematic is shown in Fig. 3(a) (left). As noted above, the PN improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage V_{bias}. Unfortunately, the original class-C oscillator restricts the fixed V_{bias} from being set low enough, otherwise the oscillator might not start up.

In [18], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [11]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [18], a simple RC bias is chosen. The oscillator schematic is shown in Fig. 3(a) (right) while Fig. 3(b) focuses on the concept of adaptive DC bias of the oscillator, where, for the ease of explanation, the inductors and resistors are shorted and the capacitors are open. The currents of the core transistors are mirrored and, after a comparison against the reference bias current I_{ref} and then integration, the resulting control voltage V_{ctrl} is applied to the cross-coupled $M_{1,2}$ transistor gates. At start-up, since there is no current through the oscillator, V_{ctrl} node rises to $V_{\text{th}} + V_{\text{od}}$. As the waveforms demonstrate, the amplitude feedback scheme produces the maximum V_{ctrl} to ensure the reliable start-up and adaptively reduces at steady-state for class-C operation with high output voltage swing.

The value of R_{bias} should not be too small as it could load the tank's Q and not too large as to avoid amplitude instability (squegging) due to the RC network delay in the feedback loop of amplitude control. The noise contribution from R_{bias} has no negative impact since it will be filtered out by the low-pass combination of R_{bias} and C_c. The alternative method of using

the transformer coupling could also be beneficial with regard to amplitude stability.

To summarize our approach so far: After choosing the class-C oscillator topology to obtain the FoM performance close to the theoretical limit, then maximizing the output swing to minimize PN, while optimizing the inductor and the capacitor bank, the final oscillator should reasonably have the lowest possible PN. In the next section we demonstrate how to further improve PN by coupling multitude of such oscillators.

III. MULTI-CORE OSCILLATOR

To address the aforementioned limitations on the PN performance of a CMOS oscillator, we exploit an old idea of coupling multiple oscillators [19]–[21] and propose that such coupling can be resistive using, e.g., long and thin traces, which is often convenient in practical realizations. Fig. 4(a) depicts this idea for $N = 2$, i.e., a dual-core oscillator. Two identical oscillator cores [generally of any topology, but here the core is the high-swing class-C from Fig. 3(a) (right)] are "coupled" in parallel thus they are locked and oscillating in-phase. Each of the inductors has its own local capacitor bank. Hence, high resonant current of each LC-tank gets circulated only locally.

According to Leeson's formula (4), by doubling the capacitance and halving L (assuming R_c is low), the oscillation frequency remains the same but R_p becomes half, which reduces PN by 3 dB. Intuitively: equivalent current noise of core #1 experiences twice the capacitance and therefore its PN contribution is reduced by 6 dB. Similarly, PN contribution of core #2 is reduced by 6 dB. These two contributions originated from core #1 and #2 are uncorrelated, thus their powers are summed up. Therefore the total PN is reduced by 3 dB.

To get a deeper insight, let us consider the following: If we would apply this technique (i.e., doubling the capacitance) to a single core, the inductor needs to be scaled down also by a factor-of-two in order to maintain the frequency. Then, PN would improve because of the R_p reduction (as discussed in Section II). However, continual reduction of L at some point

hits the physical limitations of the technology where Q-factor starts dropping precipitously. This is exactly where we back off a bit and pick our inductor value, as indicated in Fig. 2. As a result, to move forward with the PN reduction, we then proceed to the multi-core approach. Note that each LC-tank in Fig. 4(a) needs a dedicated active device ($M_{1,2}$) in order to perpetuate its oscillation, and to constrain the large resonating current $Q \cdot I_{\text{DC}}$ between L and C [see Fig. 4(b)] from going to the other core. In other words, the active devices serve an additional purpose of allowing a weak coupling between oscillators in the multi-core arrangement.

In general, the presence of N tanks reduces the PN due to a single noise source by a factor N^2. There are now N current noise sources instead of just one. As the noise sources are all uncorrelated and equal in power, the total PN is N times contribution of one of them. So, the overall PN is N times better than with a single core

$$\mathcal{L}_N(\Delta\omega) = \mathcal{L}_1(\Delta\omega) - 10\log(N). \qquad (6)$$

Obviously, the total power consumption grows N times. This keeps FoM unchanged [16]. Hence, the lower PN would come at a cost of proportionately higher power consumption and area.

For a *weakly* coupled multi-oscillator system, the oscillators inject small currents into each other and hence require some time to correct for any resulting perturbations. These perturbations will affect the coupled system differently according to their frequency content. Low frequency noise perturbations will afford enough time for the system to respond and hence achieve the expected PN improvement while fast perturbations or high frequency noise will experience less such rejection. This will be demonstrated mathematically in Section IV and then supported through measurements in Section V. The conclusion is that the coupling factor mainly affects the bandwidth of the PN improvement; i.e., the larger the coupling factor, the wider the bandwidth of the PN improvement.

It should be clarified that coupled oscillators have been historically used to provide multiple phases (with the *quadrature* being the most prominent example [22]) for integrated transceivers. To construct a $2N$-phase LC oscillator, at least N (differential) oscillator cores are needed. In theory, they have the advantage of reduced phase noise: N-coupled oscillators have N times less phase noise than a single oscillator [20]. However, such coupling for the multi-phase generation might lead to a PN degradation in two ways: first, due to a reduction of effective Q caused by the shift from the tank's resonance and, second, due to additional noise from the coupling devices [10], [23], [24].

In [25], the cores are coupled *in-phase* through g_m transistor stages in a ring arrangement, so the flicker up-conversion is avoided from the coupling devices. However, that approach is limited to class-B oscillators and does not appear applicable to other topologies. Multi-core transformer coupling through differential coplanar transmission lines for a mm-wave oscillator is presented in [26]. However, that technique seems applicable only at mm-wave due to otherwise large transformer sizes. In addition, recent works on mode-switching oscillators aim to

significantly improve the trade-off between frequency tuning range and phase noise [27]–[29]. Low/high oscillation frequency can be selected there by switching a coupling capacitor between odd/even modes of two coupled LC oscillators. Hence, in one mode the phase noise was observed to improve due to the parallel arrangement.

In our approach, the multiple oscillators are simply coupled electrically through a finite (preferably, but not necessarily, small) resistance R_c of the interconnecting wire. As stated above, the general oscillator coupling technique has been known in the past (e.g., see [19]) and has been used in microwave circuits [20] and discrete-component circuits [21], but it has not yet been sufficiently exploited in monolithic oscillators to reduce phase noise to the point of reaching the cellular basestation performance. Similar on our approach originally disclosed in [16], authors in [30] paralleled 2/4 inductors in low-/high-band modes to reduce PN while widening the total tuning range. These PN advantages of coupled oscillators ($N = 1, 2, 3$) have also been recently verified for inverter-based ring oscillators in 16-nm FinFET CMOS technology [31].

IV. ANALYSIS OF IMPERFECTIONS IN MULTI-CORE OSCILLATOR

A major concern that comes along with practical implementations of multi-core oscillators is how to connect all of them in parallel. Since the footprint of inductors is bulky, interconnections between them are expected long. Hence, the resistance of these interconnects would play a role in the PN performance. In addition, the interconnection between the oscillator cores could be switchable, in which case channel resistance of NMOS/PMOS switches could be on the order of hundreds of Ω to a few kΩ. An example of such a reconfigurable three-core oscillator was presented in [31], in which transmission gates are engaged to couple two or three inverter-ring oscillators in order to improve phase noise at the cost of power consumption.

Another imperfection is a mismatch between free-running frequencies of the cores. In presence of a high interconnect impedance, mismatch increases the chance that the cores would oscillate at separated frequencies thus producing injection pulling spurs. Therefore, the coupling should be tight enough to achieve the desired PN performance.

As depicted in Fig. 4(b), in an ideal case (completely matched cores) no static or cyclic current is passing through the wires inter-connecting the two cores. Nonetheless, a very small noise current (with an average of zero) is going back and forth. The current inside the tank is Q times larger than the fundamental current component that injects into it. Thus, in a presence of a small mismatch between the cores, if interconnection resistance is small enough, a small cyclic current at the fundamental frequency would go through the inter-connection wires to balance the cores and force them to oscillate at the same frequency.

A. Interconnect Resistance

In order to investigate the effect of interconnect resistance, we start with a simple linear time-invariant model of an oscillator shown in Fig. 5(a). It includes noise of the active device
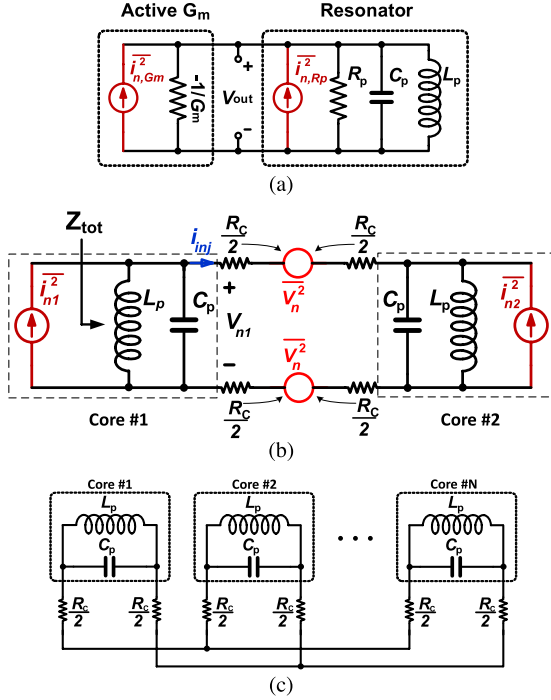
Fig. 5. Oscillator model for calculating PN: (a) simple linear model of an LC-tank oscillator; (b) dual-core oscillator model; (c) model of N star-connected oscillators.

$\overline{i_{n,Gm}^2}$ and the tank $\overline{i_{n,Rp}^2}$. Fig. 5(b) extends this model to the dual-core oscillator considering the interconnect resistance R_c between them. In this figure, the total current noise of each core, $\overline{i_{n,Gm}^2} + \overline{i_{n,Rp}^2}$, is represented as $\overline{i_n^2}$. In addition, the parallel resistance of the tank is canceled out in steady-state with a negative resistance of the active part. Although majority of oscillators operate in a strongly nonlinear region, linear analysis is still useful in gaining further insight.

Using a superposition of each core's noise, the total noise on each node can be calculated. Since all the noise sources are considered uncorrelated, their powers add up. The impedance of a single tank, Z_{tank}, oscillating at ω_0, can be approximated at a frequency offset $\Delta\omega$ as [19]

$$|Z_{\text{tank}}(\Delta\omega)| = \left| \frac{1}{2} \frac{R_p \omega_0}{Q \Delta\omega} \right|. \qquad (7)$$

The noise power at the differential node V_{n1} can thus be calculated from the superposition as follows:

$$\overline{V_{n1}^2} = \overline{i_{n1}^2} \cdot |Z_{\text{tot}}|^2 + \overline{i_{n2}^2} \cdot |Z_{\text{tot}}|^2 \cdot \left| \frac{Z_{\text{tank}}}{2R_C + Z_{\text{tank}}} \right|^2 \qquad (8)$$

where Z_{tot} is the total impedance seen from one side, defined in Fig. 5(b). Since the two cores are identical, we assume $\overline{i_n^2} = \overline{i_{n1}^2} = \overline{i_{n2}^2}$. Then, (8) is simplified to

$$\overline{V_{n1}^2} = \overline{i_n^2} \times \frac{1}{2} \times |Z_{\text{tank}}|^2 \times \frac{2R_c^2 + |Z_{\text{tank}}|^2}{R_c^2 + |Z_{\text{tank}}|^2}$$
$$= \overline{i_n^2} |Z_{\text{eq}}|^2. \qquad (9)$$

As defined in (4), $F = 1 + \overline{i_{n,gm}^2}/\overline{i_{n,R_p}^2}$, so the total noise of each core can be written as

$$\overline{i_n^2} = F \cdot \overline{i_{R_p}^2} = F \frac{4kT}{R_p}. \qquad (10)$$

The PN is calculated by dividing the noise power over the signal power. The noise calculated in (9) equally includes amplitude and PN contributions [32]. The amplitude noise is suppressed by the oscillator's nonlinearity due to its positive feedback, so only half of the power in (9) remains as noise in phase. Therefore, the PN of the dual-core oscillator is

$$\mathcal{L}(\Delta\omega) = 10 \, \log \left(\frac{\frac{V_1^2}{2}}{\frac{V_{\text{osc}}^2}{2}} \right)$$
$$= 10 \, \log \left(F \frac{4kTR_p}{V_{\text{osc}}^2} \left(\frac{|Z_{\text{eq}}|}{R_p} \right)^2 \right). \qquad (11)$$

Applying the same method for an N-core oscillator coupled in a star connection [Fig. 5(c)], results in a general equivalent impedance

$$|Z_{\text{eq}}|^2 = \frac{1}{N} \times |Z_{\text{tank}}|^2 \times \frac{NR_c^2 + |Z_{\text{tank}}|^2}{R_c^2 + |Z_{\text{tank}}|^2}. \qquad (12)$$

For $R_c \ll |Z_{\text{tank}}(\Delta\omega)|$, the third factor $(NR_c^2 + |Z_{\text{tank}}|^2)/(R_c^2 + |Z_{\text{tank}}|^2)$ is close to unity, such that $|Z_{\text{eq}}|^2 \approx |Z_{\text{tank}}|^2/N$. However, it increases with increasing R_c and the offset frequency $\Delta\omega$. Its maximum value can reach N such that $|Z_{\text{eq}}|^2 \approx |Z_{\text{tank}}|^2$. In terms of PN, the former case (i.e., tight coupling, $R_c \ll |Z_{\text{tank}}(\Delta\omega)|$) reduces the PN power N times with respect to the single-core oscillator. In the latter case, there is no benefit since the cores are completely decoupled. Summarizing

$$\overline{V_{n1}^2} = \begin{cases} \overline{i_n^2} \times \frac{|Z_{\text{tank}}|^2}{N} & R_c \to 0 \\ \overline{i_n^2} \times |Z_{\text{tank}}|^2 & R_c \to \infty. \end{cases} \qquad (13)$$

Fig. 6(a) plots an example of the maximum (i.e., $\Delta\omega \to 0$) PN improvement in the dual-core ($N = 2$) versus R_c. In our implementation, even with R_c as high as 5 kΩ, an improvement of 2.6 dB can still be obtained. Considering the PN versus $\Delta\omega$ with a certain R_c, at very low frequencies where $Z_{\text{tank}} \gg R_c$, the improvement is 3 dB. However, for very high offset frequencies where $Z_{\text{tank}}(\omega) \ll R_c$ the cores become decoupled and no improvement is achieved. Generalizing for N cores we have

$$\overline{V_{n1}^2} = \begin{cases} \overline{i_n^2} \times \frac{|Z_{\text{tank}}|^2}{N} & \Delta\omega \to 0 \\ \overline{i_n^2} \times |Z_{\text{tank}}|^2 & \Delta\omega \to \infty. \end{cases} \qquad (14)$$

The above PN model is verified against Spectre-RF simulations in Fig. 7 for $N = 1$ and 2, and with R_c of 10 kΩ and 1 kΩ. F is estimated 2. Based on the results, the analysis is in a good agreement with simulations.

Next, we calculate the noise voltage at R_c [Fig. 4(b)]. By using superposition at V_{n1} from two uncorrelated noise sources, PN can be derived as

$$\mathcal{L}(\Delta\omega) = 10 \log \left(2 \times \frac{4kTR_c}{V_{\text{osc}}^2} \left| \frac{Z_{\text{tank}}}{2R_c + 2Z_{\text{tank}}} \right|^2 \right). \qquad (15)$$
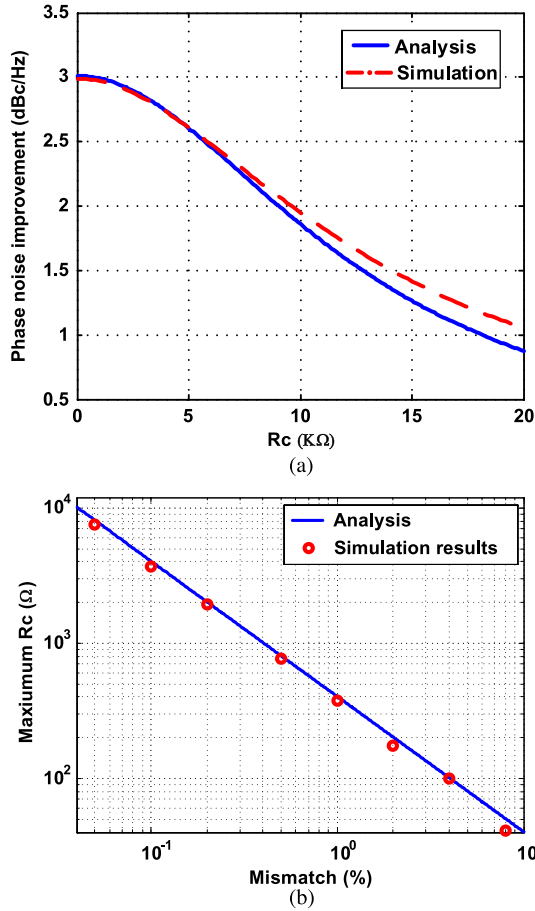
Fig. 6. (a) Effect of interconnect resistance on close-in PN improvement in a dual-core oscillator. (b) Maximum interconnect resistance to maintain a lock condition with resonant frequency mismatches between the cores.
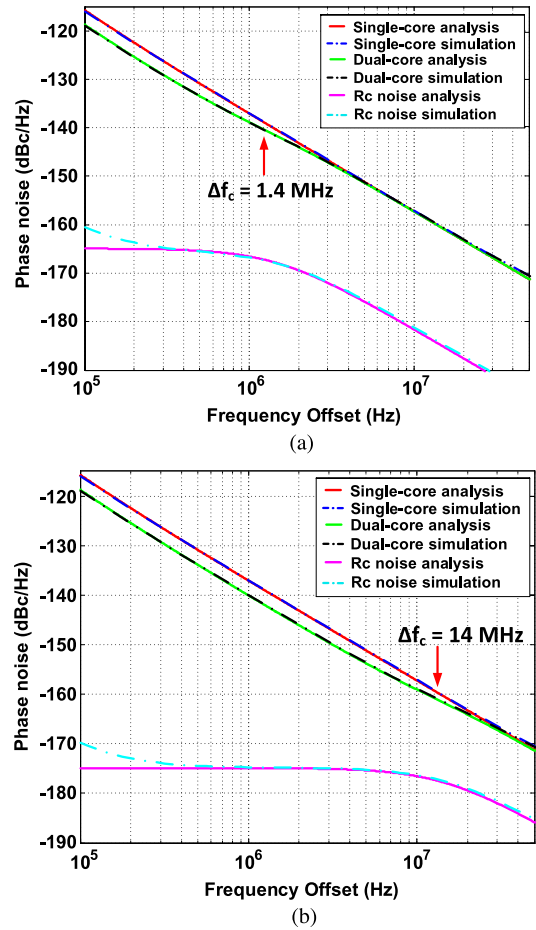

Fig. 7. Simulation and analytical plots of the phase noise with $F = 2$ in (10) including noise from R_c for two cases: (a) $R_c = 10\ k\Omega$, and (b) $R_c = 1\ k\Omega$.

This PN contributed by R_c is also plotted in Fig. 7. There is a small disagreement with the simulations due to disregarding the dynamic amplitude control in each oscillator, although the noise power level is insignificant for the realistic R_c values.

It is also insightful to calculate a corner frequency where the PN improvement starts degrading by half, from (15) and (12) as follows:

$$\Delta\omega_c = \frac{R_p\,\omega_0}{2R_c\,Q}. \tag{16}$$

This is also in agreement with the fact the PN improvement is within the lock range of the two oscillators, defined later in (17).

B. Mismatch Between the Oscillator Cores

In a realistic situation, there will certainly be resonant frequency mismatches between the oscillator cores. If, in addition, the interconnections between them are very weak, they could all be oscillating independently at their natural frequencies and so no PN improvement would be achieved.

To quantify the effect of mismatches, we start with the concept of injection locking. We consider one of the oscillators to be an aggressor, injecting current I_{inj} at an angular frequency ω_{inj} into a "victim" oscillator resonating at ω_0 with an internal

tank current I_{osc}, and whose quality factor is Q. As defined in [33], lock range ω_L and pulling strength η are re-stated in (17) and (18)

$$\omega_L \approx \frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \tag{17}$$

$$\eta = \frac{\omega_L}{|\omega_0 - \omega_{\text{inj}}|}. \tag{18}$$

The injection current (I_{inj}) in Fig. 5(b) can be evaluated as

$$I_{\text{inj}} = \frac{|V_{\text{osc}}|}{|2\,Rc + Z_{\text{tank}}(\Delta\omega_n)|} \tag{19}$$

where $\Delta\omega_n$ is the frequency shift from ω_0 after two oscillators are locked (for simplicity, let us assume $\Delta\omega_n = ((\omega_{osc1} - \omega_{osc2})/2)$). In order for both oscillators to maintain the lock condition, η should be larger than one. Applying this condition, together with (18) and (19), the maximum allowable R_c is calculated from

$$R_c < \frac{\omega_0\,R_p}{4Q}\sqrt{1 - \frac{1}{\Delta\omega_n}}. \tag{20}$$

This expression is validated against Spectre-RF simulations at different mismatches and the comparison is shown in Fig. 6(b). For instance, for a typical mismatch of 1%, the upper limit on the interconnect resistance R_c is 400 Ω.
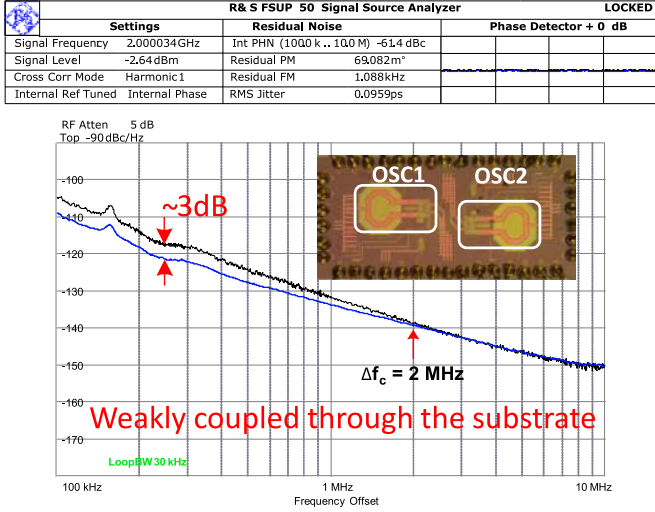
Fig. 8. Phase noise improvement through the parasitic coupling of two separate oscillators.
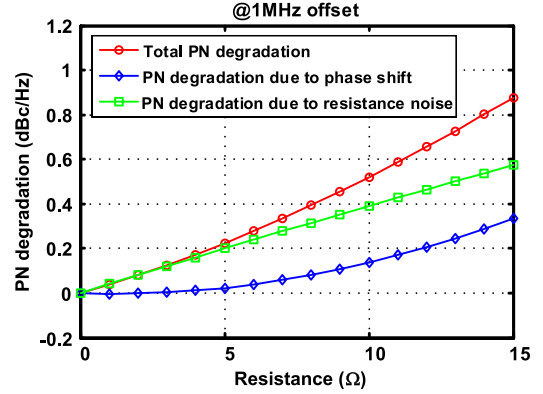

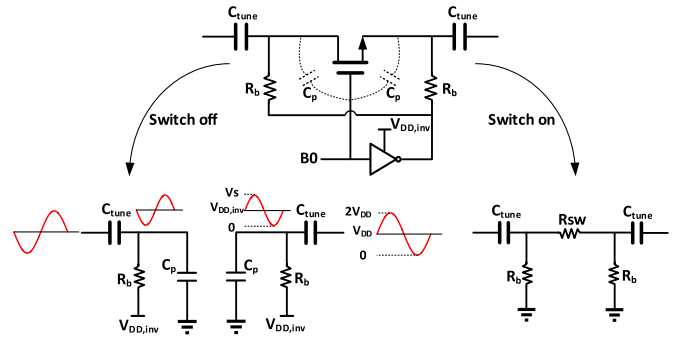Fig. 9. Phase noise degradation due to ohmic resistance in g_m cross-coupled connection.

Fig. 10. Switched-capacitor for coarse tuning of the oscillator frequency. $V_{\mathrm{DD,inv}} = 0.8$ V ensures a long-term reliability for thin-oxide devices.

In fully monolithic implementations, the natural coupling between various oscillators through substrate is mostly considered undesired as it could produce injection pulling spurs and lead to modulation distortion [34], [35]. Here, it is advantageous as it improves tolerance to mismatches in the oscillators' natural frequencies. In order to show that the natural substrate coupling can relax specification on the interconnection strength, the chip in [34] (shown in Fig. 8) is re-measured for our purposes. The chip contains two separate oscillators and the only interaction between them is parasitic substrate and magnetic coupling. In order to measure the amount of injection, two oscillators are forced to resonate 10 MHz away from each other, which leads to injection pulling spurs. Based on calculations according to [33], the power of the biggest injection pulling spur under a weak injection is

$$P(\omega_{\mathrm{spur}}) \approx \left(\frac{\omega_0}{4Q} \cdot \frac{I_{\mathrm{inj}}}{I_{\mathrm{osc}}} \cdot \frac{1}{\omega_m} \right)^2 \qquad (21)$$

where ω_m is the offset frequency of the generated spur. By measuring the spurious tone power, the injection current is calculated around 70 μA. By extracting V_{osc} from post-layout simulations, it turns out that the equivalent coupling resistance R_c is about 25 kΩ. Using (16), the calculated lock range is about 2 MHz. As shown in Fig. 8, at low frequencies, the PN improves 3 dB but degrades rapidly around 2 MHz (lock range) and reaching the PN level of a single core oscillator. These measurement results confirm the formulas derived above. To summarize: The natural parasitic substrate coupling between oscillators provides a certain level of injection locking that results in PN improvements, but a deliberate electrical connection would further push the region of the PN improvements to much higher frequency offsets.

V. DESIGN CONSIDERATIONS AND MEASUREMENT RESULTS

Since the ultimate goal in this work is to achieve the ultra-low PN, careful attention should be paid to the ohmic resistance R_{par} of the cross-coupled connection (in series with C_c). As

shown in Fig. 9, the delay is introduced ($R_{\mathrm{par}}C_c \approx 5$ ps) in the oscillator loop, which degrades the effective quality factor and reduces the center frequency. Moreover, the noise from R_{par} can degrade PN with total degradation as high as 0.5 dB when $R_{\mathrm{par}} = 10$ Ω, which could happen in case the layout is not carefully done.

To avoid AM-to-PM noise conversion, MOM capacitors are used here, instead of linear varactors, as they are less sensitive to the supply noise. A switched capacitor structure, shown in Fig. 10, is used to coarsely tune the resonant frequency. Here, a conventional topology is used but with a single modification, which will be explained shortly. The size of the switches is set as a compromise between their parasitic capacitance (too large switches would reduce the tuning range) and the PN degradation (too small switches would introduce a resistive loss, R_{sw}, in on-state, thus reducing the Q-factor of the switched capacitors, $Q_{\mathrm{on}} = 2/(\omega C_{\mathrm{tune}} \cdot R_{\mathrm{sw}})$). The switch pull-up/down resistor, R_b (here, 20 kΩ), needs to be chosen large enough to avoid the tank Q-factor degradation during the off-state, $Q_{\mathrm{off}} = 1/(R_b C_p \omega)$. However, floating the source/drain of the switch must be avoided, otherwise the transistor would enter undesirable regions. Since the stated objective is the ultra-low PN, large transistor sizes are used in the switched-capacitor bank. The bank contains 5-bit switchable capacitance, in which both the capacitors and switches are sized together in a binary fashion. The unit capacitance is 170 fF and its switch has a total width of 270 μm. Such a large unit size ensures excellent

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

		This Work	JSSC'13 [2]	JSSC'13 [3]	JSSC'15 [4]	ISSCC'12 [5]	ISSCC'12 [6]	RFIC'07 [7]	JSSC'06 [8]	JSSC'15 [9]	Mini Circuits MOS-975	Analog Devices ADF4350
Description		Dual-Core Class-C	Class-F	Class-D	Class-F2	Clip & Restore	Class-B/C	Colpitts	Class-B	Class-B	-	-
Technology		65nm	65nm	65nm	65nm	65nm	55nm	130nm	90nm	55nm	BiCMOS	BiCMOS
Tuning Range (GHz)		4.07-4.91 (18.6%)	2.94-3.78 (25%)*	3-4.8 (48%)	7.2-8.7 (18.8%)	3.64-4.03 (10.2%)*	3.35-4.6 (31.44%)*	1.5-1.65 (9.6%)	3.21-4.1 (24.3%)	7.4-8.4 (12.6%)		0.88-0.99 (11.8%)
Frequency (GHz)		4.07	3.7	4.8	4.2	3.92	3.35	1.56	0.915	4	3.3	0.915
Phase Noise (dBc/Hz)	3MHz	-146.7	-133	-136	-141.71	-142.2	-142	-150.38	-149	-141	-143.5	-163.4
	20MHz	-163.1	-149.5	-152.5	-158.18	-158.6	-158.48	-166.85	-167	-157.5	-160	-179.9
Phase Noise norm. to a 915MHz carrier (dBc/Hz)	3MHz	-159.7	-147.4	-150.5	-154.35	-154.3	-153.3	-155.02	-149	-153.8	-154.7	-163.4
	20MHz	-176.14	-163.9	-167	-170.8	-170.7	-169.75	-171.49	-167	170.3	-171.2	-179.9
Supply Voltage (V)		2.15	1.25	0.5	1.3	1.2	1.5	3.3	1.4	1.5	3.3	5
Current (mA)		59	12	14	32	21.5	18	88	18	4	70	33
FoM @ 3MHz (dB)		189	192.2	191	191	189.9	189	180	184.6	195	180.7	191
Area (mm²)		0.37¹	0.157	0.116	0.26	0.19	0.49	0.32²	0.52¹	0.19	-	-

¹ Including decoupling capacitor
² Including buffers
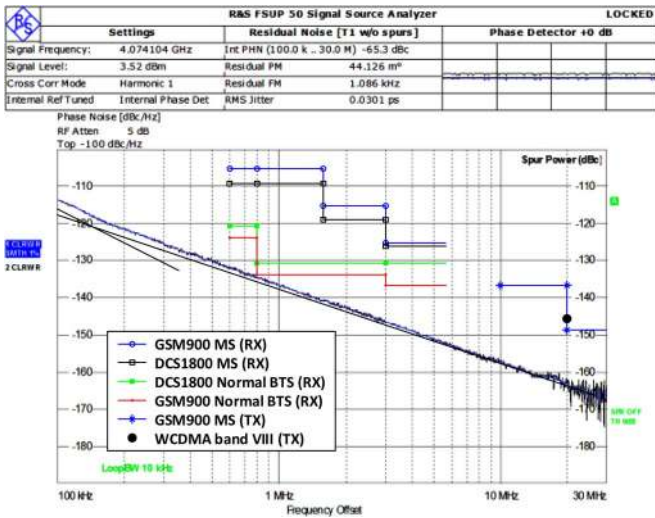
Fig. 11. Phase noise plot of the oscillator.

(a)

(b)

Fig. 12. (a) Chip micrograph; (b) related FR4 PCB board with wire bond length reduction.
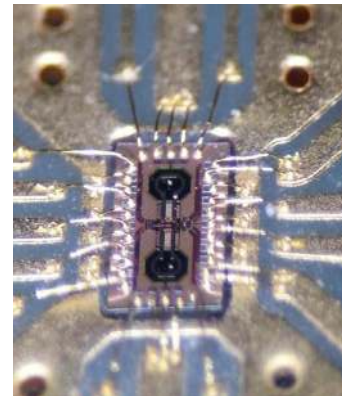
Q-factor in the switched-capacitor's on-state but it increases oscillator's parasitics thus limiting its tuning range.

In the off-state, the voltage swing at the drain of the switch driver is very high ($V_{osc} \cdot C_{tune}/(C_{tune} + C_p)$, with the capacitance ratio here 0.55–0.6) which is usually beyond the reliability limit of thin-oxide devices. To solve this, one could use larger thick oxide devices whose parasitic capacitances are higher in order to have the same Q. However, doing so would degrade the tuning range (C_{on}/C_{off} becomes smaller). Here, to tackle this problem, we propose to use a different supply voltage for the driver, $V_{DD,inv} = 0.8$ V. This way, the thin oxide devices can still be used while ensuring reliability and avoiding the tuning range degradation.

The dual-core HSCC oscillator is implemented in TSMC 65 nm LP CMOS. Its chip micrograph is shown in Fig. 12(a). The measured output frequency range is from 4.07 GHz to 4.91 GHz, yielding 18.6% tuning range. Measured phase noise (PN) is plotted in Fig. 11 together with normalized PN specifications of some of the toughest cellular basestation (BTS) and mobile (MS) communication standards [1]. The normalized measured PN is well below the receiver LO purity specifications of "GSM900 MS," "DCS1800 MS," and "normal BTS." The PN is also 0.6 dB below the toughest "GSM900 normal BTS"
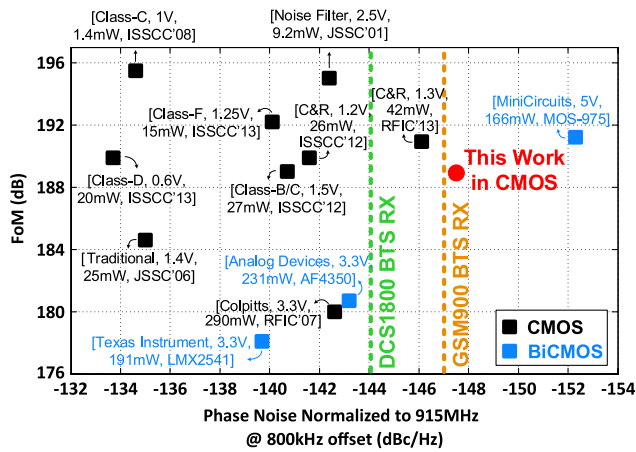
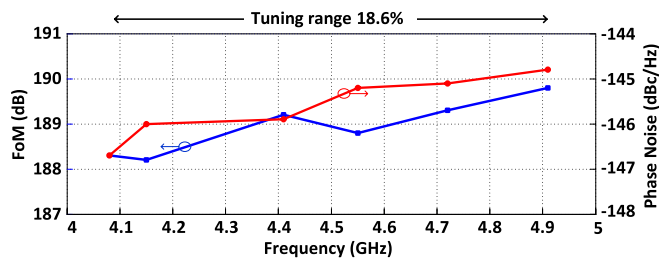Fig. 13. Comparison with state-of-the-art low phase noise oscillators.

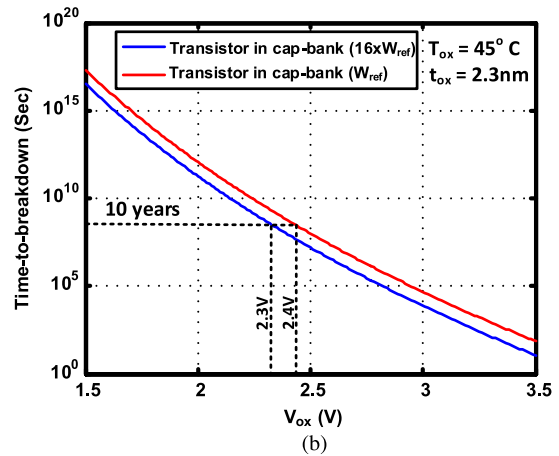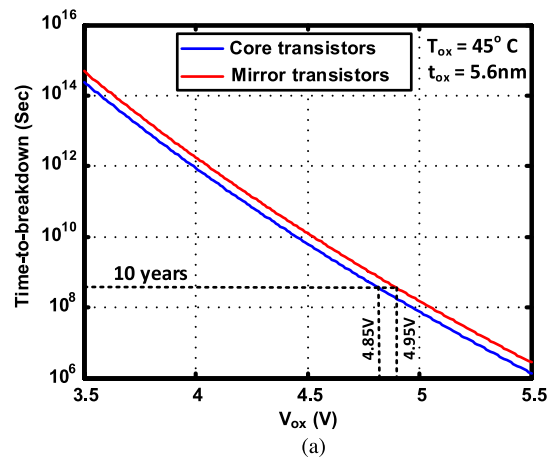Fig. 14. Measured phase noise and FoM at 3 MHz offset over the tuning range.

Fig. 15. (a) Estimated time-to-breakdown of this dual-core oscillator based on the measured parameter of 65 nm CMOS in [4]. (a) Thick oxide core transistors. (b) Thin oxide switched-capacitor transistors (W_{ref} is the smallest transistor width in the switched-capacitor bank).

at 800 kHz offset although this could degrade by up to 1.5 dB over the entire tuning range, which is mostly due to flicker noise upconversion. It also meets MS transmitter standards of GSM900 and WCDMA band-VIII with 14 dB and 17 dB margins, respectively. To the best of our knowledge, this is the first-ever reported oscillator in CMOS IC that reaches all these requirements. This PN could be further lowered by 3 dB by adding two more oscillator cores.

The implemented differential inductor is 300 pH, but its effective value will be a bit increased due to the routing of the capacitor bank. The total estimated Q from a post-layout simulations is around 20. The cross-coupled thick-oxide transistors are sized at (112 μm/280 nm), in order to ensure safe start-up with a reasonable margin for worst case conditions and proper class-C operation. The mirror ratio should also be chosen carefully (in this design, 5) in accordance with its bias capacitance to avoid potential squegging. The oscillator drains 39 mA to 59 mA from a 2.15 V power supply, which is much higher than the nominal 1.2 V supply of core transistors. Thick oxide devices are used instead to insure reliability. Each oscillator core has an independently controlled 5-bit binary-weighted coarse MoM capacitor bank. This chip was directly wire bonded on a PCB board. In order to reduce the effects of high current spikes in the supply voltage due to the wire-bond inductance, 250 pF decoupling capacitance is added on-chip. To further improve performance, the fabricated chip was placed in a hole in the PCB board to shorten the wire-bond length, as shown in Fig. 12(b).

Flicker noise corner frequency is 130 kHz at the lower end of the tuning range and it increases to 300 kHz at 4.91 GHz because of the switching off all the MoM capacitors. Fig. 13 compares PN and FOM of the dual-core oscillator versus state-of-the-art low-phase-noise CMOS oscillators and some commercial basestation oscillators made of discrete components. Table I compares it with other recently published state-of-the-art CMOS oscillators (and commercial BiCMOS oscillators). This oscillator has the lowest PN of -159.7 dBc/Hz and -176.1 dBc/Hz normalized to the 915 MHz carrier at 3 MHz and 20 MHz offsets, respectively. The measurements of the PN and FoM over the tuning range are depicted in Fig. 14. The average FoM over the tuning range is about 189 dB.

Based on (22), (23), and measurement data in [4] for exactly the same 65-nm CMOS technology, the lifetime estimation of this oscillator is plotted in Fig. 15(a) for both the core and mirror transistors. The plot indicates that the maximum voltage across the oxide for transistors should be less than 4.85 V to ensure 0.01% failure during 10 years of operation at 45 °C. The worst case maximum V_{ox} in this case is around 4.6 V, which demonstrates no reliability concerns.

As mentioned above, the switched-capacitor transistors used in this design are thin-oxide devices. In order to check their

reliability, the same figure (Fig. 15(b)) is plotted for this binary weighted bank. The maximum V_{ox} in this case is around 1.7 V, which is clearly well below the value for the 10-year operational guaranty.

VI. CONCLUSION

To further extend the phase noise (PN) performance barrier of CMOS oscillators, a dual-core LC-tank oscillator based on a high-swing class-C (HSCC) topology is introduced in this paper. Simple expressions for PN and interconnect resistance R_c are derived and verified against circuit-level simulations. Simulations and analysis show that R_c is not of a high importance up to a certain reasonably large value and that R_c should be limited due to mismatches between the two cores. This approach can be extended to a higher number of cores and to allow reaching far beyond the state-of-the-art PN levels at the expense of power consumption and area. The proposed oscillator was implement in 65 nm CMOS. Measurement shows that this oscillator can meet even the toughest PN specification of cellular basestations while ensuring long-term reliability.

ACKNOWLEDGMENT

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