energies

MDPI

Article

Analysis and Design of a New High Voltage Gain Interleaved DC–DC Converter with Three-Winding Coupled Inductors for Renewable Energy Systems

Shin-Ju Chen [1,*], Sung-Pei Yang [1,2], Chao-Ming Huang [1] and Ping-Sheng Huang [1]

[1] Department of Electrical Engineering, Kun Shan University, Tainan 710303, Taiwan
[2] Green Energy Technology Research Center, Kun Shan University, Tainan 710303, Taiwan
* Correspondence: sjchen@mail.ksu.edu.tw; Tel.: +886-6-205-0323

Abstract: In this article, a new non-isolated interleaved DC–DC converter is proposed to provide a high voltage conversion ratio in renewable energy systems. The converter configuration is composed of a two-phase interleaved boost converter integrating a voltage-lift capacitor and three-winding coupled inductor-based voltage multiplier modules to achieve high step-up voltage conversion and reduce voltage stresses on the semiconductors (switches and diodes). The converter can achieve a high voltage conversion ratio when working at a proper duty ratio. The voltage stresses on the switches are significantly lower than the output voltage, which enables engineers to adopt low-voltage-rating MOSFETs with low ON-state resistance. The switches can turn on under zero-current switching (ZCS) conditions because of the leakage inductor series reducing switching losses. Some diodes can naturally turn off under ZCS conditions to alleviate the reverse–recovery issue and to reduce reverse–recovery losses. The input current has small ripples due to the interleaved operation. The leakage inductor energy is recycled and voltage spikes on the switches are avoided. The proposed converter is suitable for applications in which high voltage gain, high efficiency and high power are required. The principle of operation, steady-state analysis and design considerations of the proposed converter are described in detail. In addition, a closed-loop controller is designed to reduce the effect of input voltage fluctuation and load change on the output voltage. Finally, a 1000 W laboratory prototype is built and tested. The theoretical analysis and the performance of the proposed converter were validated by the experimental results.

Keywords: high voltage gain DC–DC converter; three-winding coupled inductor; zero-current switching; closed-loop controller design

Citation: Chen, S.-J.; Yang, S.-P.; Huang, C.-M.; Huang, P.-S. Analysis and Design of a New High Voltage Gain Interleaved DC–DC Converter with Three-Winding Coupled Inductors for Renewable Energy Systems. *Energies* **2023**, *16*, 3958. https://doi.org/10.3390/en16093958

Academic Editors: Giampaolo Buticchi, Emilio Lorenzani and Giovanni Migliazza

Received: 1 March 2023
Revised: 28 April 2023
Accepted: 5 May 2023
Published: 8 May 2023

1. Introduction

The demand for renewable energies, such as fuel cells and photovoltaic arrays, has dramatically increased for electricity generation because of the shortage of fossil fuels and the growing climate change impacts [1]. The renewable energy system is shown in Figure 1. A 380 or 400 V_{dc} dc-bus voltage is necessary for grid-connected applications if the line voltage of the utility grid is 220 V_{ac}. However, the output voltages of fuel cells and photovoltaic arrays are typically lower than 50 V. Therefore, DC–DC converters with high voltage conversion ratios are necessary to boost the low voltages of green energy resources to the high dc-bus voltage required in renewable energy system applications.

High voltage gain DC–DC converters can be mainly divided into two types: isolated and non-isolated. The traditional isolated type adjusts the transformer turns ratio to obtain high voltage gain, such as in push–pull, half-bridge, forward and flyback DC–DC converters. However, high leakage inductance derived from the high turns ratio may result in high voltage spikes and poor efficiency. A boost converter of the non-isolated type can, theoretically, achieve high voltage gain by operating at a very large duty ratio. However, the voltage conversion ratio is practically limited due to parasitic elements [2]. In general,

high voltage rated MOSFETs have the characteristic of high ON-state resistance $R_{DS(ON)}$, and the high voltage-rated diodes have high forward voltage drop. Therefore, a high voltage gain DC–DC converter, having low voltage stresses on the switches and diodes, can contribute to reducing conduction losses. Consequently, low semiconductor voltage stress is important for efficiency considerations in the new high voltage gain converter topology.

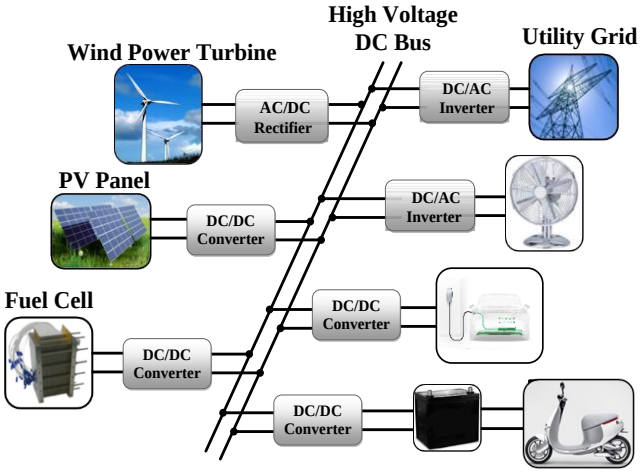


Figure 1. A renewable energy system.

In recent years, high voltage gain DC–DC converters have been researched in depth by means of different voltage-boosting techniques. The most widely used method is based on the coupled inductor technique. In [3], a coupled inductor-based soft switched high step-up converter with a voltage multiplier cell was proposed for DC microgrid applications. In [4], five categories of high step-up coupled-inductor boost converters were reviewed. Two configurations for two- and three-winding coupled inductor-based high step-up DC–DC converters were proposed for sustainable energy applications in [5]. In [6], a three-winding coupled inductor-based high voltage gain DC–DC converter was proposed for photovoltaic (PV) systems. The turns ratio of the coupled inductor can be utilized to increase design freedom for the voltage conversion ratio in addition to the duty ratio. The winding cross-coupled inductor contributes to the current sharing performance of the interleaved two-phase converter [7]. The voltage multiplier cell (VMC) is often composed of a coupled inductor and diode–capacitor to further extend the voltage gain and reduce the switch voltage stress [8–11]. A converter topology that integrates a built-in transformer, coupled inductor, diode and capacitor is proposed to extend the higher voltage gain [12,13]. To achieve high voltage gain with simple circuit structures a number of approaches have been proposed, such as the following: transformer-less and coupled inductor-less techniques of a hybrid switched-inductor in [14], modified active switched-inductor in [15], active switched-inductor and passive switched-capacitors in [16,17] and switched-capacitor in [18]. Three-level DC–DC converters have a simple configuration and decrease the switch voltage stress to half the output voltage [19,20]. To reduce switching losses, zero-voltage switching (ZVS) or zero-current switching (ZCS) in high voltage gain DC–DC converters were proposed in [21–23]. The review papers provide good references for research on high voltage gain DC–DC converters [24–27].

A new non-isolated high voltage gain, interleaved DC–DC converter, suitable for renewable energy applications, is proposed in this article. The techniques of voltage-lift, three-winding coupled inductors and voltage multiplier modules are used to increase the voltage conversion ratio and to reduce the voltage stresses on the power devices.

The characteristics and benefits of the presented converter are summarized as follows:

(1) The high voltage gain of the proposed converter can be obtained with an appropriate duty ratio.

(2) Low voltage-rated MOSFETs with low ON-state resistance $R_{DS(ON)}$ and low voltage-rated diodes with low forward voltage drop can be adopted to reduce conduction losses, due to their having low voltage stresses.
(3) The switches turn ON under the ZCS condition to reduce switching losses.
(4) The diode reverse–recovery issue is mitigated due to the leakage inductors of the coupled inductors, and voltage spikes on the switches are avoided because the leakage energy is recycled.
(5) The interleaved parallel input structure of the presented configuration decreases current stresses on the power devices and reduces the input current ripple.

The rest of this article is organized as follows. The operational principle of the proposed converter is presented in detail in Section 2. The steady-state analysis is given in Section 3. The driving circuit and the closed-loop controller design is demonstrated in Section 4. Section 5 demonstrates the simulation and experimental results when using a 1000 W laboratory prototype to validate the theoretical analysis and to assess the effectiveness of the presented converter. This article is concluded in Section 6.

2. Proposed Converter and Principle of Operation

2.1. Proposed Converter

The circuit configuration of the proposed converter topology is shown in Figure 2a. The proposed converter has two coupled inductors with three windings. Their own coupling references are denoted "●" and "○".

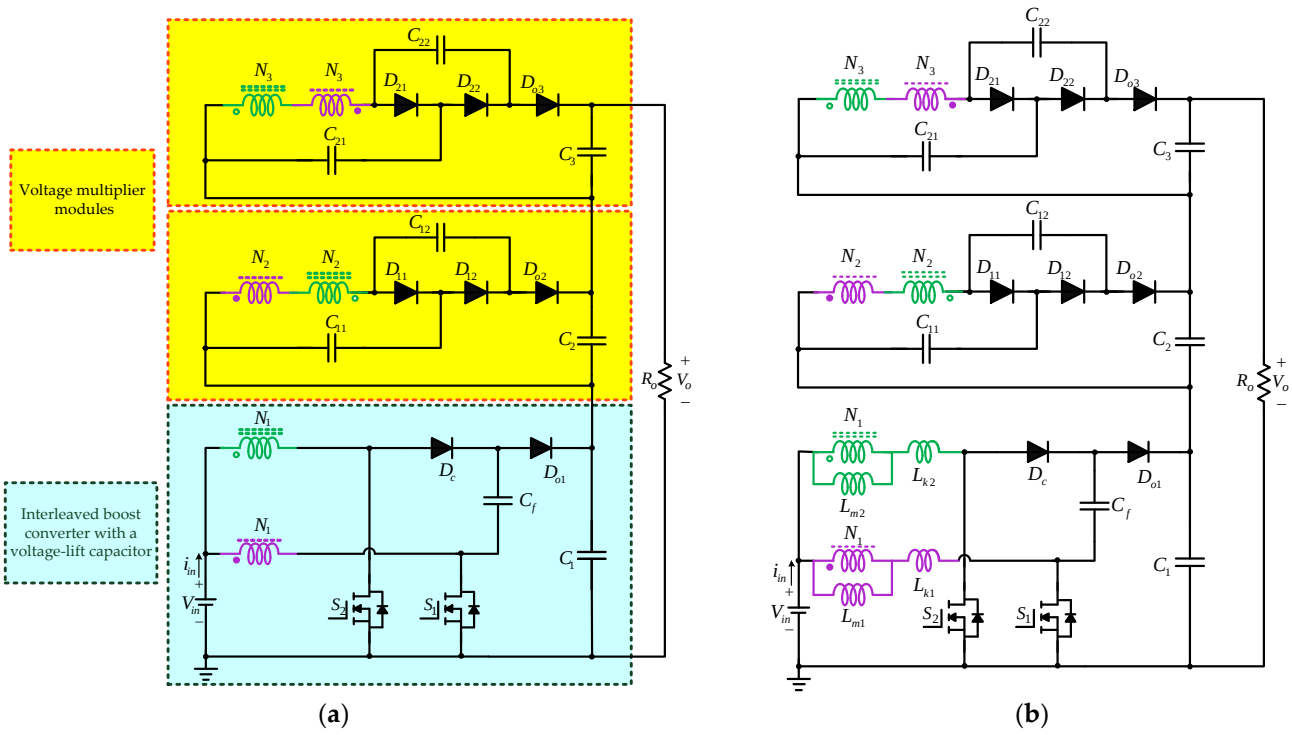


Figure 2. (**a**) Proposed high voltage gain DC–DC converter. (**b**) Equivalent circuit.

The first winding of each coupled inductor acts as an input filter inductor. The second and third windings of the coupled inductors are inserted in series integrating capacitors and diodes to form two voltage multiplier modules (VMMs). It should be pointed out that the arrangement positions of the series windings are different in the two VMMs, so that the output capacitors, C_2 and C_3, can be charged and discharged alternately to reduce the output voltage ripple. The proposed converter primarily consists of two parts: one part is the interleaved boost converter integrating a voltage-lift capacitor, and the other part is the stacked structure of two voltage multiplier modules on the output side to further

extend the voltage gain and reduce the voltage stresses on the power devices. Interleaved operation is adopted to help the current ripple cancellation on the input side.

Figure 2a, S_1 and S_2 present the following power switches: C_f is the voltage-lift capacitor, C_1, C_2 and C_3 are the output capacitors, C_{11} and C_{21} are the regenerative capacitors, C_{12} and C_{22} are the voltage-doubler capacitors, D_c is the clamp diode, D_{o1}, D_{o2} and D_{o3} are the output diodes, D_{11} and D_{21} are the regenerative diodes, D_{12} and D_{22} are the voltage-doubler diodes and R_o is the output load. The equivalent circuits for the coupled inductors consist of the ideal transformers with a turns ratio N_1:N_2:N_3, the magnetizing inductors L_{m1} and L_{m2}, and the leakage inductors L_{k1} and L_{k2}. Figure 2b shows the equivalent circuit of the presented converter.

2.2. Operational Principle

The switches S_1 and S_2 operate in an interleaved manner with phase shift 180° to lower the input current ripple due to ripple cancellation. The duty ratio of the switches is greater than 0.5 for high step-up voltage gain purposes. The key steady-state waveforms of the presented converter, operating in continuous conduction mode (CCM), are shown in Figure 3. According to the ON/OFF state of the switches and diodes in one switching period, the converter has eight operational stages, as illustrated in Figure 4.

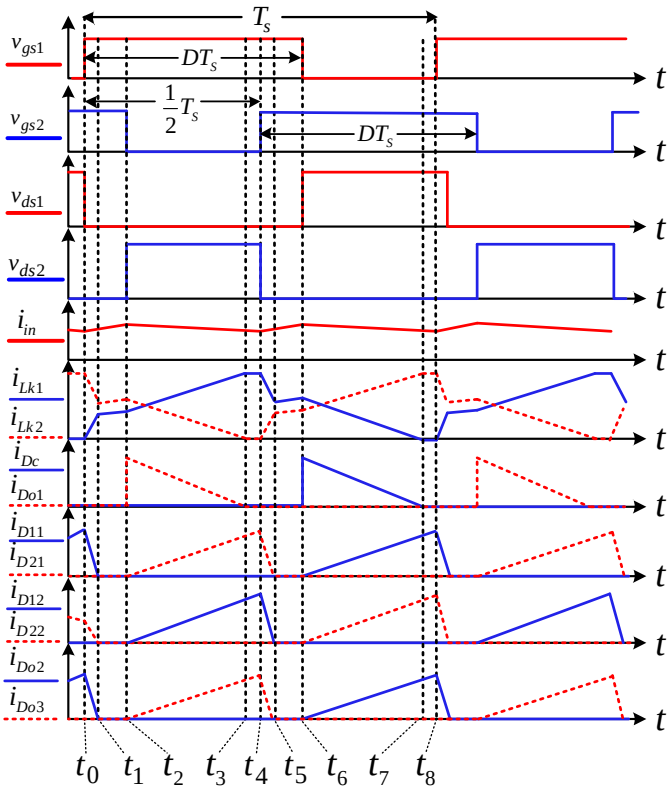
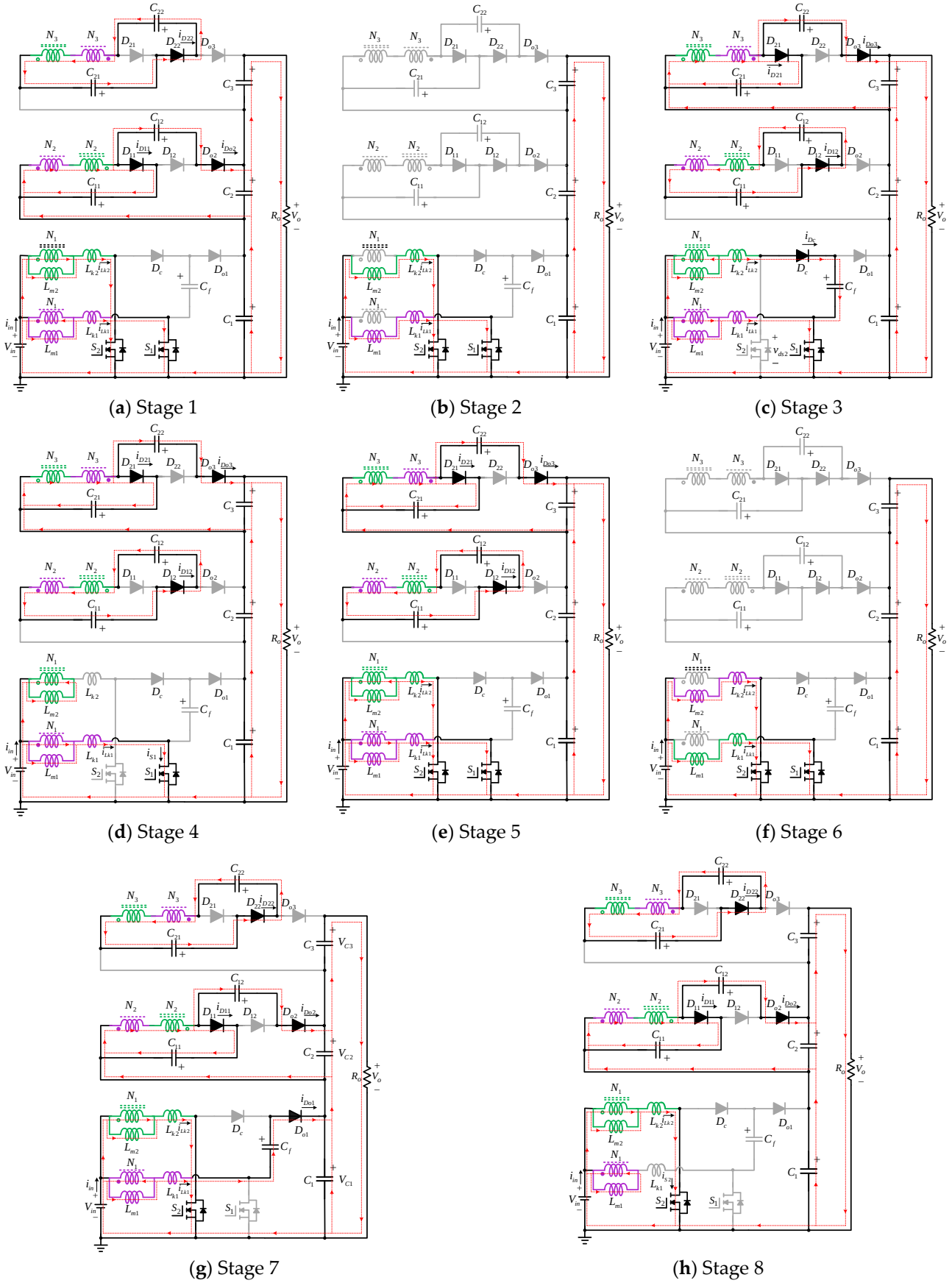


Figure 3. Key steady-state waveforms.

In order to simplify the circuit analysis, some assumptions are made, as follow:

1. All semiconductors (switches and diodes) are considered to be ideal.
2. All capacitors are sufficiently large, and the voltages on these capacitors are regarded as constant during one switching period.
3. The parameters of the three-winding coupled inductors are regarded as being identical; that is, the turns ratio $n = N_2/N_1 = N_3/N_1$, $L_{m1} = L_{m2} = L_m$ and $L_{k1} = L_{k2} = L_k$. The coupling coefficient of the coupled inductor is defined as $k = L_m/(L_m + L_k)$.



(**a**) Stage 1 (**b**) Stage 2 (**c**) Stage 3

(**d**) Stage 4 (**e**) Stage 5 (**f**) Stage 6

(**g**) Stage 7 (**h**) Stage 8

Figure 4. Operational stages.

Stage 1 [$t_0 \sim t_1$]: At the beginning of this stage, switch S_1 starts to conduct and S_2 keeps to the on-state. The diodes D_{o1}, D_c, D_{12}, D_{21} and D_{o3} are reverse-biased. Due to the existence of leakage inductor L_{k1} and the initial current $i_{Lk1}(t_0) = 0$, S_1 achieves ZCS turn-on because of the leakage inductor series. In this stage, the leakage current i_{Lk1} increases rapidly from its initial value (zero). The magnetizing energy stored in L_{m1} still transfers to the second and third windings of the coupled inductor when $i_{Lk1} < i_{Lm1}$. The currents i_{D11}, i_{D22} and i_{Do2} decrease and the descent rate is limited by the leakage inductors L_{k1} and L_{k2}. Therefore, the reverse-recovery issue of these diodes is lessened.

When the leakage current i_{Lk1} rises to reach $i_{Lk1} = i_{Lm1}$ at $t = t_1$, the currents i_{D11}, i_{Do2} and i_{D22} decrease to zero. The diodes D_{11}, D_{o2} and D_{22} turn OFF under the ZCS condition. During this stage, the leakage current i_{Lk1} is given by

$$i_{Lk1}(t) = i_{Lm1}(t) - n(i_{D11}(t) + i_{Do2}(t) + i_{D22}(t)) \tag{1}$$

Stage 2 [$t_1 \sim t_2$]: The switches S_1 and S_2 are turned ON, and all diodes are reverse-biased during this stage. The input voltage V_{in} supplies energy to the magnetizing inductors L_{m1} and L_{m2} as well as the leakage inductors L_{k1} and L_{k2}. The leakage currents i_{Lk1} and i_{Lk2} increase linearly. The output capacitors C_1, C_2 and C_3 provide energy to the output load. When the switch S_2 is turned OFF, the stage ends. During this stage, the leakage currents can be represented as

$$i_{Lk1}(t) = i_{Lk1}(t_1) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_1) \tag{2}$$

$$i_{Lk2}(t) = i_{Lk2}(t_1) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_1) \tag{3}$$

Stage 3 [$t_2 \sim t_3$]: The switch S_2 is turned OFF at $t = t_2$. The clamp diode D_c begins to conduct because the leakage current i_{Lk2} is continuous. The diodes D_{12}, D_{21}, D_{o3} and D_c are forward-biased. The current i_{Lk2} flows through D_c, C_f and S_1 to charge the voltage-lift capacitor C_f. The voltage across S_2 is clamped by the capacitor voltage V_{Cf}. The leakage current i_{Lk2} decreases and the energy stored in the magnetizing inductor L_{m2} is transferred to charge the capacitors C_{12} and C_{21} via the second and third windings of the coupled inductor during this stage. In the meantime, capacitors C_{11} and C_{22} are discharged. This stage is terminated when i_{Lk2} falls to zero at $t = t_3$.

Stage 4 [$t_3 \sim t_4$]: At the beginning of this stage, the leakage energy stored in L_{k2} is released completely. The clamp diode D_c is turned OFF with ZCS naturally. The magnetizing current i_{Lm2} is reflected from the first winding to the second and third windings completely. The operation of this stage is similar to stage 3. This stage ends when switch S_2 returns to conduct at $t = t_4$. The switch current i_{S1} is equal to the sum of i_{Lm1} and i_{Lm2} during this stage, which can be written as

$$i_{S1}(t) = i_{Lm1}(t) + n(i_{D12}(t) + i_{D21}(t) + i_{Do3}(t)) = i_{Lm1}(t) + i_{Lm2}(t) \tag{4}$$

Stage 5 [$t_4 \sim t_5$]: At the beginning of this stage, switch S_2 starts to conduct and S_1 keeps to the on-state. The diodes D_{o1}, D_c, D_{11}, D_{o2} and D_{22} are reverse-biased. Due to the existence of leakage inductor L_{k2} and the initial current $i_{Lk2}(t_4) = 0$, S_2 achieves ZCS turn-on because of the leakage inductor series. In this stage, the leakage current i_{Lk2} increases rapidly from its initial value (zero). The magnetizing energy stored in L_{m2} still transfers to the second and third windings of the coupled inductor when $i_{Lk2} < i_{Lm2}$. The currents i_{D12}, i_{D21} and i_{Do3} decrease and the descent rate is limited by the leakage inductors L_{k1} and L_{k2}. Therefore, the reverse-recovery issue of these diodes is lessened.

When the leakage current i_{Lk2} rises to reach $i_{Lk2} = i_{Lm2}$ at $t = t_5$, the currents i_{D12}, i_{D21} and i_{Do3} decrease to zero. The diodes D_{12}, D_{21} and D_{o3} are turned OFF with the ZCS condition. During this stage, the leakage current i_{Lk2} is given by

$$i_{Lk2}(t) = i_{Lm2}(t) - n((i_{D21}(t) + i_{D12}(t)) + i_{Do3}(t)) \quad (5)$$

Stage 6 [$t_5 \sim t_6$]: The switches S_1 and S_2 conduct, and all diodes are reverse-biased during this stage. The magnetizing inductors L_{m1} and L_{m2} as well as the leakage inductors L_{k1} and L_{k2} are supplied with energy by the input voltage V_{in}. The leakage currents i_{Lk1} and i_{Lk2} increase linearly. The output capacitors C_1, C_2 and C_3 provide energy to the output load. The stage ends when switch S_1 is turned OFF. During this stage, the leakage currents can be represented as

$$i_{Lk1}(t) = i_{Lk1}(t_5) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_5) \quad (6)$$

$$i_{Lk2}(t) = i_{Lk2}(t_5) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_5) \quad (7)$$

Stage 7 [$t_6 \sim t_7$]: Switch S_1 is turned OFF at $t = t_6$. The output diode D_{o1} begins to conduct because the leakage current i_{Lk1} is continuous. The diodes D_{11}, D_{22}, D_{o1} and D_{o2} are forward-biased. The leakage current i_{Lk1} flows through D_{o1}, C_f and C_1 to charge the output capacitor C_1 and to discharge the voltage-lift capacitor C_f. The voltage across S_2 is clamped by the voltages on the capacitors C_f and C_1. The switch voltage stress is equal to $-V_{Cf} + V_{C1}$. During this stage, the leakage current i_{Lk1} decreases and the energy stored in the magnetizing inductor L_{m1} is transferred to charge the capacitors C_{11} and C_{22} via the second third windings of the coupled inductor. In the meantime, capacitors C_{12} and C_{21} are discharged. This stage is terminated when the leakage current i_{Lk1} decreases to zero at $t = t_7$,

Stage 8 [$t_7 \sim t_8$]: At the beginning of this stage, the leakage energy stored in L_{k1} is released completely. The output diode D_{o1} is naturally turned OFF with ZCS. The magnetizing current i_{Lm1} is reflected from the first winding to the second and third windings completely. The operation of this stage is similar to that of stage 7. During this stage, the switch current i_{S2} is equal to the sum of i_{Lm1} and i_{Lm2}, which is derived from

$$i_{S2}(t) = i_{Lm2}(t) + n(i_{D11}(t) + i_{Do2}(t) + i_{D22}(t)) = i_{Lm1}(t) + i_{Lm2}(t) \quad (8)$$

When switch S_1 returns to conduct at $t = t_8$, this stage ends. Then, another new switching cycle begins.

3. Steady-State Analysis

In order to simplify the steady-state analysis of the suggested topology, the transient stages of stage 1 and stage 5 are disregarded, due to their significantly short times, and the leakage inductors are ignored with coupling coefficient $k = 1$.

3.1. Voltage Gain Analysis

By applying the volt-second balance principle to the magnetizing inductor L_{m2}, the voltage-lift capacitor voltage V_{Cf} can be obtained by

$$V_{Cf} = \frac{1}{1 - D} V_{in} \quad (9)$$

The result is identical to the output voltage of the traditional boost converter. In addition, the magnetizing inductor L_{m1} also satisfies the volt-second balance principle. We obtain

$$-V_{Cf} + V_{C1} = \frac{1}{1 - D} V_{in} \quad (10)$$

Therefore, the voltage of the output capacitor C_1 can be derived by

$$V_{C1} = \frac{2}{1-D} V_{in} \tag{11}$$

In stage 3, the magnetizing inductor voltages are given by

$$v_{Lm1} = kV_{in} \tag{12}$$

$$v_{Lm2} = k(V_{in} - V_{Cf}) = \frac{kD}{1-D} V_{in} \tag{13}$$

where the coupling coefficient is defined as

$$k = L_m/(L_m + L_k) \tag{14}$$

The voltage of the capacitor C_{21} can be calculated by the voltages of the third windings in series in the voltage multiplier module in stage 3. This is given by

$$V_{C21} = nv_{Lm1} - nv_{Lm2} = \frac{kn}{1-D} V_{in} \tag{15}$$

Moreover, by applying the Kirchhoff's Voltage Low (KVL) to the circuit of stage 3, the following equations can be obtained

$$V_{C12} + nv_{Lm2} - nv_{Lm1} - V_{C11} = 0 \tag{16}$$

$$V_{C3} + nv_{Lm2} - nv_{Lm1} - V_{C22} = 0 \tag{17}$$

In stage 7, the magnetizing inductor voltages are given by

$$v_{Lm1} = V_{in} + V_{Cf} - V_{C1} = -\frac{kD}{1-D} V_{in} \tag{18}$$

$$v_{Lm2} = kV_{in} \tag{19}$$

The voltage of the capacitor C_{11} can be calculated by the voltages of the series' third windings in the voltage multiplier module in stage 7. This is given by

$$V_{C11} = nv_{Lm2} - nv_{Lm1} = \frac{kn}{1-D} V_{in} \tag{20}$$

Moreover, by applying the Kirchhoff's Voltage Low (KVL) to the circuit of stage 7, the following equations can be obtained

$$V_{C2} + nv_{Lm1} - nv_{Lm2} - V_{C12} = 0 \tag{21}$$

$$V_{C22} + nv_{Lm1} - nv_{Lm2} - V_{C21} = 0 \tag{22}$$

Arranging the above equations, the voltages of the capacitors C_{12}, C_{22}, C_2 and C_3 can be obtained. The results are as follows.

$$V_{C12} = V_{C22} = \frac{2kn}{1-D} V_{in} \tag{23}$$

$$V_{C2} = V_{C3} = \frac{3kn}{1-D} V_{in} \tag{24}$$

From Equations (11) and (24), the output voltage of the proposed converter can be derived by

$$V_o = V_{C1} + V_{C2} + V_{C3} = \frac{6kn+2}{1-D} V_{in} \tag{25}$$

Consequently, the voltage gain M_k of the presented converter can be written in the form

$$M_k = \frac{V_o}{V_{in}} = \frac{6kn+2}{1-D} \tag{26}$$

The different curves of voltage gain with turns ratio n = 1, and various coupling coefficients, k = 1, 0.95, 0.9, are shown in Figure 5. Clearly, the coupling coefficient k has little influence on the voltage gain. If the leakage inductor is ignored (the coupling coefficient k = 1), then the ideal voltage gain of the proposed converter is written in the form

$$M = \frac{V_o}{V_{in}} = \frac{6n+2}{1-D} \tag{27}$$

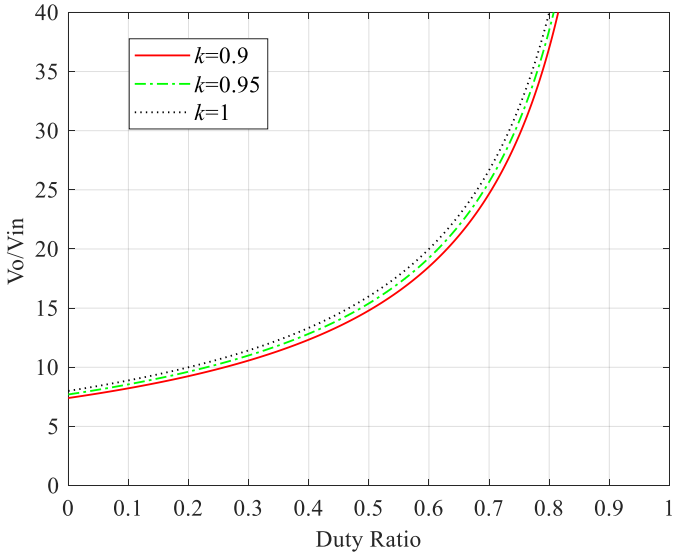


Figure 5. Voltage gain curves related to coupling coefficient (n = 1).

From Equation (27), it can be concluded that the voltage gain of the proposed converter has two degrees of design freedom, turns ratio n and duty ratio D. The high voltage gain of the proposed converter can be accomplished without an extremely large duty ratio if the designer selects the appropriate turns ratio of the coupled inductor. The voltage gain curves related to the turns ratio and the duty ratio are plotted in Figure 6. In fact, one can see that the voltage gain was 20 times with duty ratio D = 0.6 and turns ratio n = 1. Thus, the presented topology is suitable for high step-up voltage conversion.

Based on the operational principle of the presented topology, the voltage stress on switches S_2 and S_1 can be determined by stage 3 and by stage 7, respectively. With the help of Equation (27), the switch voltage stress is given by

$$V_{S2} = V_{Cf} = \frac{1}{1-D} V_{in} = \frac{1}{6n+2} V_o \tag{28}$$

$$V_{S1} = V_{C1} - V_{Cf} = \frac{1}{1-D} V_{in} = \frac{1}{6n+2} V_o \tag{29}$$

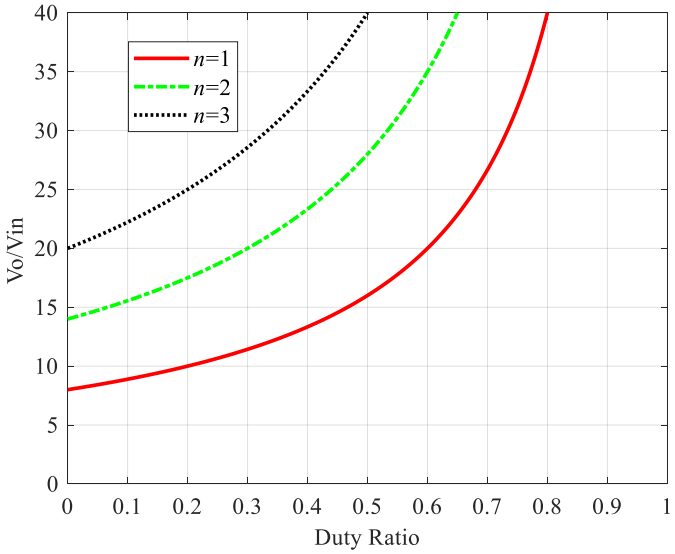


Figure 6. Voltage gain curves related to turns ratio (k = 1).

3.2. Voltage Stress Analysis

The switch voltage stress is much smaller than the output voltage. Therefore, MOSFETs with low rated voltage and low on-resistance $R_{DS(ON)}$ can be used to reduce the conduction losses. Moreover, the voltage stresses on the following diodes can be obtained from stage 3.

$$V_{Do1} = V_{C1} - V_{Cf} = \frac{1}{1-D}V_{in} = \frac{1}{6n+2}V_o \tag{30}$$

$$V_{Do2} = V_{C2} - V_{C11} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{31}$$

$$V_{D11} = V_{C12} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{32}$$

$$V_{D22} = V_{C22} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{33}$$

Similarly, the voltage stresses on the following diodes can be obtained from stage 7.

$$V_{Dc} = V_{C1} = \frac{2}{1-D}V_{in} = \frac{1}{3n+1}V_o \tag{34}$$

$$V_{D12} = V_{C12} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{35}$$

$$V_{D21} = V_{C22} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{36}$$

$$V_{Do3} = V_{C3} - V_{C21} = \frac{2n}{1-D}V_{in} = \frac{n}{3n+1}V_o \tag{37}$$

From the results in Equations (30)–(37), the voltage stresses on the diodes are much lower than the output voltage. Therefore, the designer can choose the low forward voltage drop diodes to reduce conduction losses. It is known that the voltage stress on the switch or diode in the interleaved boost converter is equal to the output voltage. Thus, the presented converter has the merit of low semiconductor voltage stress.

3.3. Design Consideration

3.3.1. Considerations of Coupled Inductor Design

If an appropriate duty ratio is selected, then the turns ratio of the coupled inductor can be calculated according to Equation (27) and is given by

$$n = \frac{V_o(1-D)}{6V_{in}} - \frac{1}{3} \tag{38}$$

In order to operate under CCM and current-ripple considerations, the magnetizing inductor of the coupled inductor is designed as follows. If the average current through the magnetizing inductor is denoted as I_{Lm} and its ripple current is denoted as Δi_{Lm}, then, the condition for the presented converter operating in CCM can be represented as

$$I_{Lm} > \frac{1}{2}\Delta i_{Lm} \tag{39}$$

Based on the operational principle, the ripple current Δi_{Lm} can be expressed as

$$\Delta i_{Lm} = \frac{V_{in}}{L_{\mathrm{m}}} DT_s \tag{40}$$

where T_s is the switching period. The average current I_{Lm} can be written in the form

$$I_{Lm} = \frac{P_o}{2V_{in}} \tag{41}$$

where P_o denotes the output power. Therefore, the value of the magnetizing inductor L_m must satisfy the following condition in CCM operation.

$$L_m > \frac{V_{in}^2 DT_s}{P_o} \tag{42}$$

Substituting Equation (27) into Equation (42), we obtain

$$L_m > \frac{(1-D)^2 V_o^2 DT_s}{(6n+2)^2 P_o} = \frac{D(1-D)^2 R_o}{(6n+2)^2 f_s} \tag{43}$$

where f_s is the switching frequency.

3.3.2. Considerations regarding Capacitor Design

The main consideration regarding each capacitor is suppression of the voltage ripple to an acceptable level. According to the operational principle of the presented converter, the output capacitor C_1 discharges to the load by the output current in a total time of about DT_s. Therefore, the ripple voltage on the output capacitor C_1 can be expressed as

$$\Delta V_{C1} \approx \frac{DV_o}{R_o C_1 f_s} \tag{44}$$

Substituting Equations (11) and (27) into Equation (44), we obtain

$$\Delta V_{C1} = \frac{(3n+1)DV_{C1}}{R_o C_1 f_s} \tag{45}$$

If the specification of the voltage ripple on the output capacitor C_1 is provided, then the design condition of the output capacitor C_1 can be given by

$$C_1 = \frac{(3n+1)D}{R_o f_s (\Delta V_{C1}/V_{C1})} \tag{46}$$

Similarly, if the percentage of voltage ripple is specified, then the design conditions of the output capacitors C_2 and C_3 can be, respectively, expressed as

$$C_2 = \frac{(6n+2)D}{3nR_o f_s(\Delta V_{C2}/V_{C2})} \tag{47}$$

$$C_3 = \frac{(6n+2)D}{3nR_o f_s(\Delta V_{C3}/V_{C3})} \tag{48}$$

The average charging current $\bar{i}_{C11(\text{charge})}$ of the regenerative capacitor C_{11} in one switching period is equal to the average current $\bar{i}_{D11}$ of the regenerative diode D_{11}. By applying the amp-second balance principle, the design condition of capacitor C_{11} can be expressed as

$$C_{11} = \frac{(6n+2)}{nR_o f_s(\Delta V_{C11}/V_{C11})} \tag{49}$$

The average discharging current $\bar{i}_{C12(\text{discharge})}$ of the voltage-doubler capacitor C_{12} in one switching period is equal to the average current $\bar{i}_{Do1}$ of the output diode D_{o1}. In a similar way to that of the design method of C_{11}, the design condition of the capacitance and the voltage ripple can be derived by

$$C_{12} = \frac{(6n+2)}{2nR_o f_s(\Delta V_{C12}/V_{C12})} \tag{50}$$

Similarly, the values of the capacitors C_{21} and C_{22} can be, respectively, derived by

$$C_{21} = \frac{(6n+2)}{nR_o f_s(\Delta V_{C21}/V_{C21})} \tag{51}$$

$$C_{22} = \frac{(6n+2)}{2nR_o f_s(\Delta V_{C22}/V_{C22})} \tag{52}$$

3.4. Converter Performance Comparison

In order to illustrate the performance of the presented converter, a comparison to the similar interleaved high voltage gain DC-DC converters published in [28–33] is shown in Table 1. If the turns ratio was $n \geq 1$ (the general case for high voltage gain purposes), it revealed the following results: (1) the voltage conversion ratio of the presented converter was the highest; (2) the switch voltage stress of the presented converter was the lowest, and was much lower than the output voltage; (3) the maximum diode voltage stress of the presented converter was the lowest, and was much lower than the output voltage; (4) the number of components was not the largest.

The voltage gain of the presented converter was higher than that of the converter in [33] if the turns ratio was $n > 1$. The switches turned on under the ZCS condition to reduce the switching losses in the proposed converter. The converter in [33] had the advantage of fewer components; however, the switches did not have the ZCS turn-on feature.

Table 1. Performance comparison.

Reference Converter	**[28]**	**[29]**	**[30]**	**[31]**	**[32]**	**[33]**	**Proposed**
Voltage gain	$\frac{3n+1}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{3n+D(2n-1)+2}{1-D}$	$\frac{5n+1}{1-D}$	$\frac{4n+4}{1-D}$	$\frac{6n+2}{1-D}$
Voltage stress on switches	$\frac{V_o}{3n+1}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+4}$	$\frac{V_o}{3n+D(2n-1)+2}$	$\frac{V_o}{5n+1}$	$\frac{V_o}{4n+4}$	$\frac{V_o}{6n+2}$
Maximum diode voltage stress	$\frac{2nV_o}{3n+1}$	$\frac{(2n+1)V_o}{2n+2}$	$\frac{nV_o}{n+2}$	$\frac{(n+1)V_o}{3n+D(2n-1)+2}$	$\frac{2nV_o}{5n+1}$	$\frac{(2n+1)V_o}{2n+2}$	$\frac{nV_o}{3n+1}$

Table 1. *Cont.*

Reference Converter	[28]	[29]	[30]	[31]	[32]	[33]	Proposed
Number of switches	2	2	2	2	2	2	2
Number of diodes	8	6	6	9	7	5	8
Number of capacitors	7	5	6	8	6	5	8
Number of coupled inductor	2	2	2	2	2	2	2
Voltage gain $n = 1$, $D = 0.6$	10	10	15	14	15	20	20

4. Driving Circuit and Controller Design

The converter operates in an interleaved mode. It was necessary to design a driving circuit to generate PWM signals with a phase shift of 180° to drive the power switches. The driving circuit implemented by the PWM IC KIA494 is shown in Figure 7.

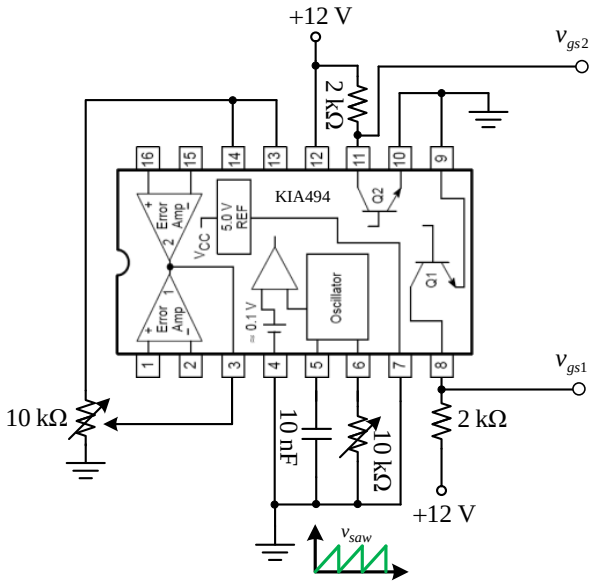


Figure 7. Driving circuit diagram.

In order to keep the output voltage at a specific value, regardless of input voltage fluctuations and load changes, the closed-loop control system, shown in Figure 8, was employed to obtain good output voltage regulation. In the block diagram, $C(s)$ is the controller transfer function and $1/V_P$ is the pulse-width modulator (PWM) gain, where V_P is the amplitude of sawtooth waveform in the PWM. Function $P(s)$ is the small signal transfer function of the presented converter from the duty ratio to the output voltage and K is the sensor gain of the output voltage. The controller $C(s)$ required a design such that the open-loop transfer function $T_{OL}(s)$ met the following specifications:

- A gain crossover frequency of 1 kHz ($2\pi \times 10^3$rad/s).
- A phase margin (P.M.) larger than 50°.
- The low frequency gain of the open-loop transfer function $T_{OL}(s)$ to be very high to reduce the steady-state error for the constant reference input.

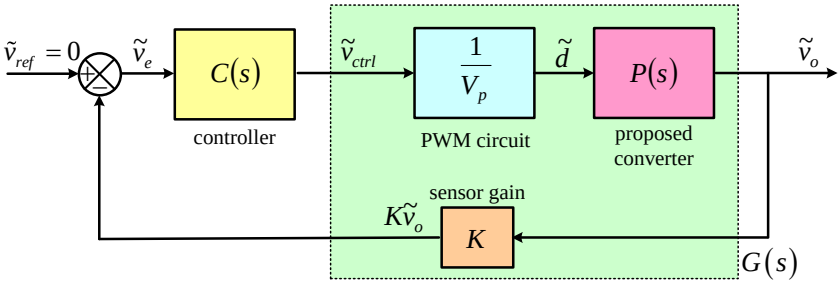


Figure 8. Functional block diagram of the feedback system.

The frequency response analyzer NF FRA51602 was used to measure the frequency response from the control signal $\tilde{v}_{ctrl}$ to the output voltage sensing signal $K\tilde{v}_o$ at the operating point of the proposed converter. Then, the curve fitting method, using the MATLAB software, was employed to establish the transfer function of $G(s)$, where

$$G(s) = \frac{K\tilde{v}_o(s)}{\tilde{v}_{ctrl}(s)} = \frac{K}{V_p}P(s) \tag{53}$$

The transfer function by the curve-fitting method is obtained by

$$G(s) = \frac{k\tilde{v}_o(s)}{\tilde{v}_{ctrl}(s)} = \frac{1.54}{\left(1+\frac{2.2}{1400}s+\frac{1}{1400^2}s^2\right)} \tag{54}$$

The Bode plots of the measured method and the curve-fitting method are shown together in Figure 9. From the comparison, it can be seen that the curves were quite consistent for the frequency range concerned. Consequently, the transfer function given in Equation (54) was utilized to design the controller.

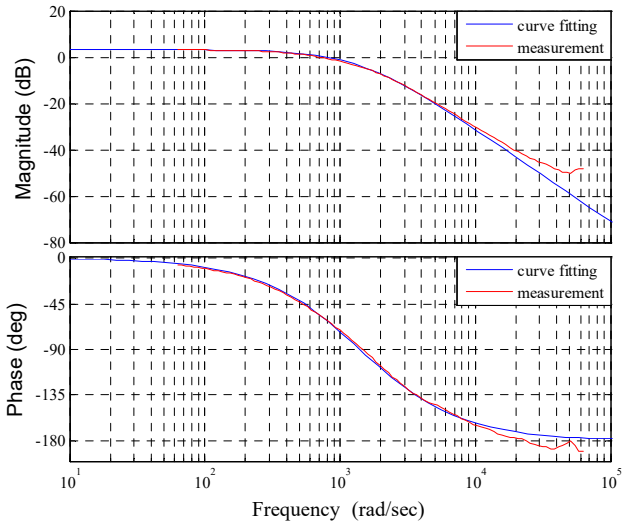


Figure 9. Comparison of frequency responses.

In this article, the *K* factor approach [34] was employed to design the well-known Type III controller. The electronic circuit with six passive components is illustrated in Figure 10, and the circuit transfer function is expressed by

$$\frac{\tilde{v}_{ctrl}(s)}{K\tilde{v}_o(s)} = -\frac{R_1+R_3}{R_1R_3C_2}\frac{\left(s+\frac{1}{R_2C_1}\right)\left(s+\frac{1}{(R_1+R_3)C_3}\right)}{s\left(s+\frac{1}{R_2C_1C_2/(C_1+C_2)}\right)\left(s+\frac{1}{R_3C_3}\right)} \tag{55}$$

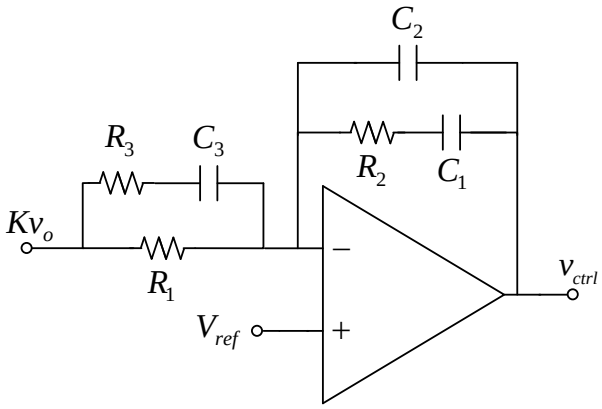


Figure 10. Controller circuit.

The controller consists of an integrator and two sets of phase leaders. The integrator is helpful to ensure a steady-state error of zero. The phase leaders are helpful to provide enough phase margin to keep the control loop stable. The controller transfer function was designed and obtained as

$$C(s) = \frac{1.13 \times 10^6 (s + 2024)(s + 1761)}{s(s + 24380)(s + 20903)} \tag{56}$$

with the parameters of the six components:

$$R_1 = 100\ \text{k}\Omega, R_2 = 426\ \text{k}\Omega, R_3 = 9.2\ \text{k}\Omega,\ C_1 = 1.16\ \text{nF}, C_2 = 0.105\ \text{nF}, C_3 = 5.2\ \text{nF}$$

The frequency response of the controller $C(s)$ is shown in Figure 11.

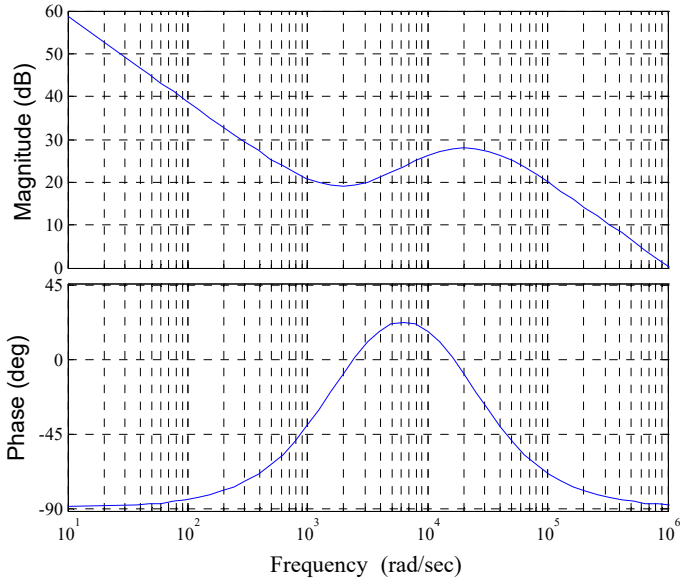


Figure 11. Frequency response of the controller.

The frequency response of the open-loop transfer function $T_{OL}(s) = C(s)G(s)$ was obtained as depicted in Figure 12. The control system provides a gain crossover frequency of $\omega = 2\pi \times 10^3$ rad/s, a phase margin of 50°, and very high DC gain. Thus, the designed controller satisfies the specification requirements of the voltage control system.

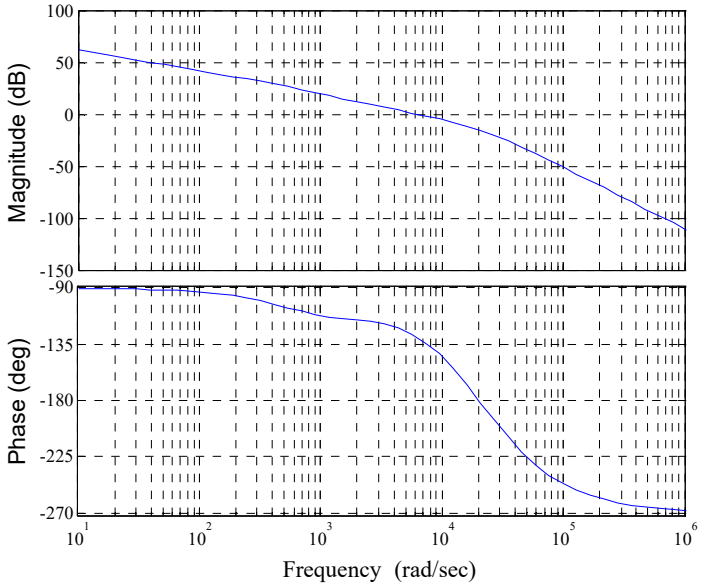


Figure 12. Frequency response of $T_{OL}(s)$.

5. Experimental Results

A 1000 W laboratory prototype, with voltage conversion from 24 V to 400 V, was implemented and tested to validate the performance of the presented converter. The detailed and complete circuit of the experiment with the closed-loop control is shown in Figure 13. The sensor gain K of the output voltage was equal to 1/100 in the closed-loop control system. Therefore, the reference signal V_{ref} was equal to 4 V. Figure 14 shows the prototype photograph. The components and parameters of the experimental converter are shown in Table 2. The simulation of the proposed converter was performed by the circuit simulation software Is-Spice, with the circuit shown in Figure 15. The Under the full load (1000 W) condition, the simulated results and the experimental results are demonstrated in Figures 16–24.

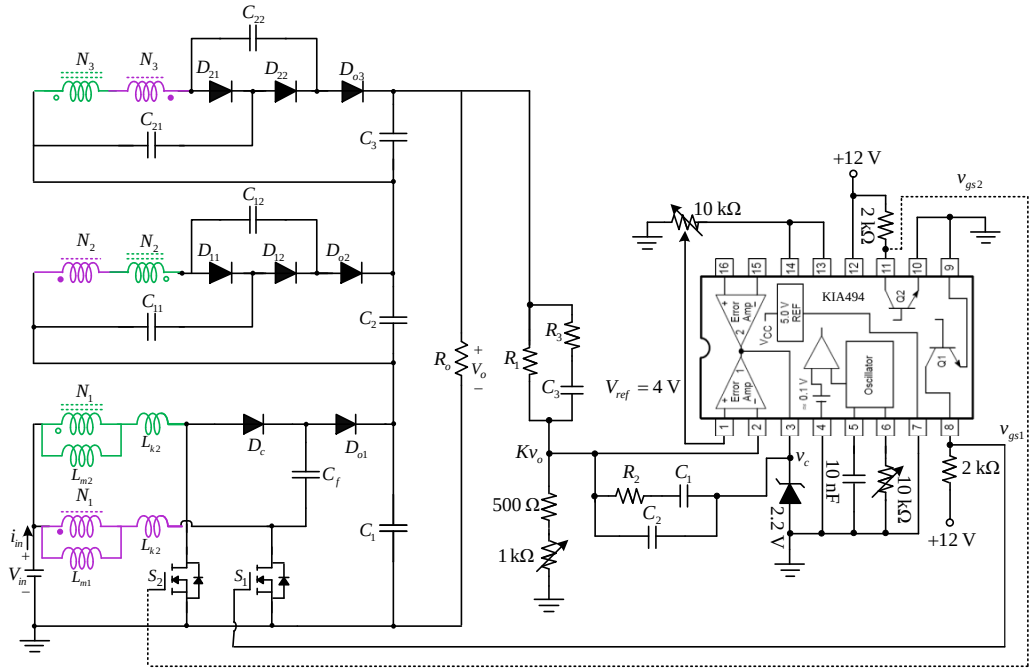


Figure 13. The complete circuit with feedback control.

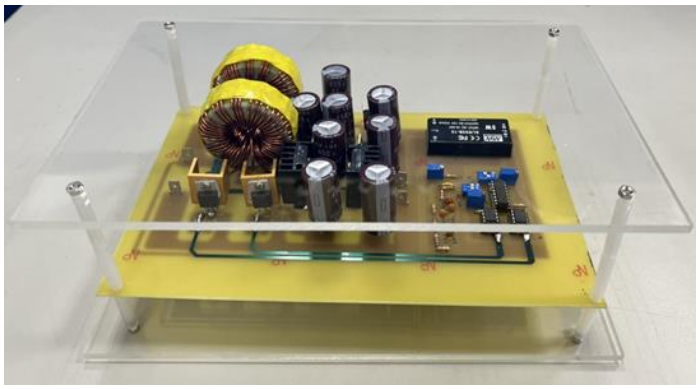


Figure 14. Prototype photograph.

Table 2. Parameters of prototype converter.

Components	Parameters
Magnetizing inductors L_{m1}, L_{m2}	73 µH
Leakage inductors L_{k1}, L_{k2}	0.6 µH
Turns ratio of coupled inductor n	1
Voltage-lift capacitor C_f	82 µF
Output capacitors C_1, C_2, C_3	150 µF
Regenerative capacitors C_{11}, C_{21}	82 µF
Voltage-doubler capacitors C_{12}, C_{22}	82 µF
Switching frequency f_s	50 kHz
Switches S_1, S_2	FDP036N10A
Diodes D_{11}, D_{21}, D_{12}, D_{22}, D_{o2}, D_{o3}	V30120C
Diodes D_c, D_{o1}	30CPQ200

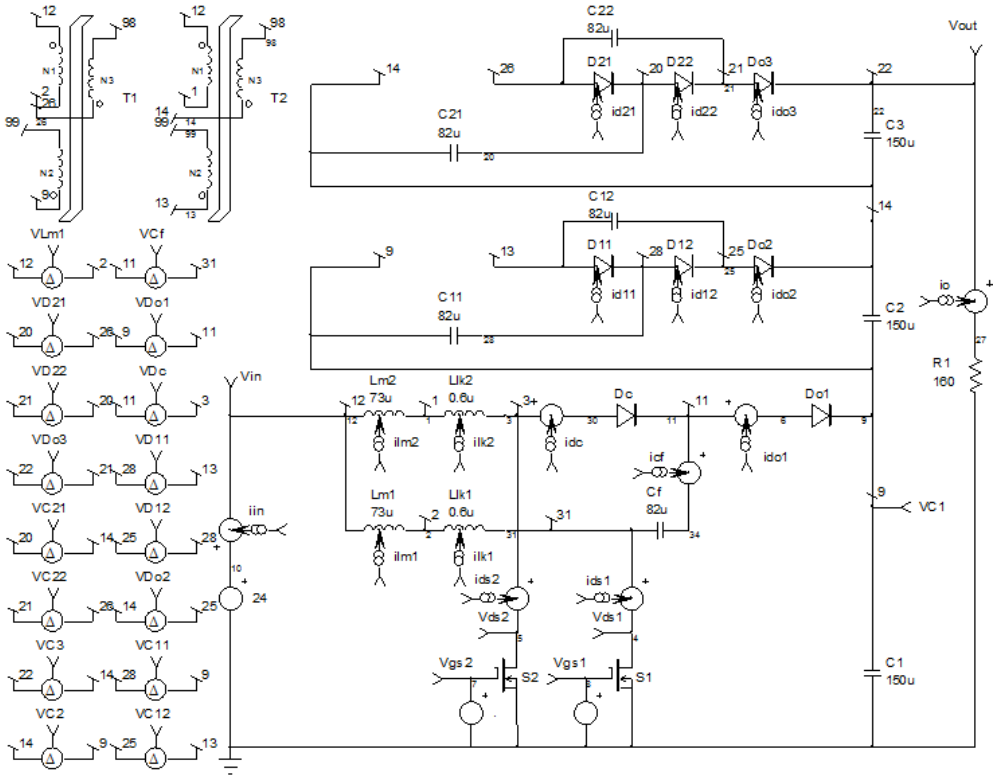
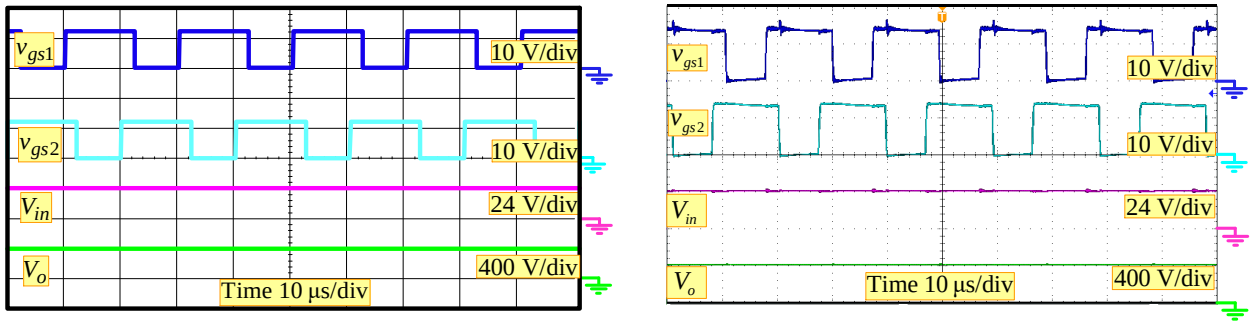
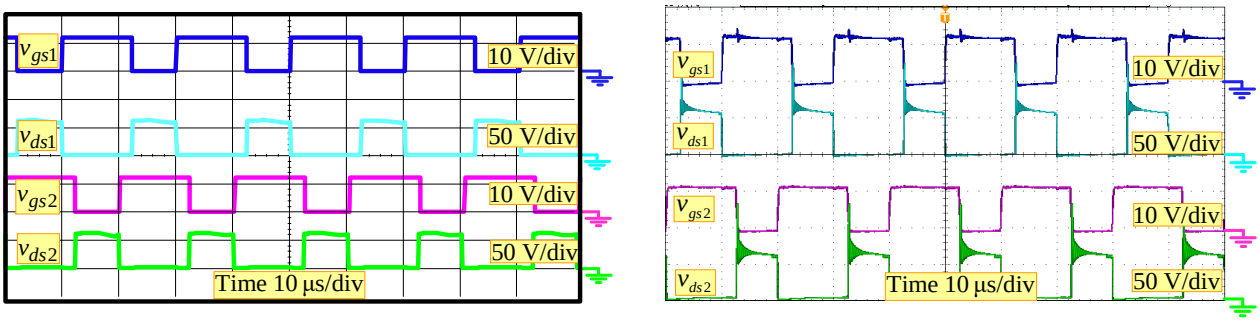


Figure 15. Is-spice simulation circuit.



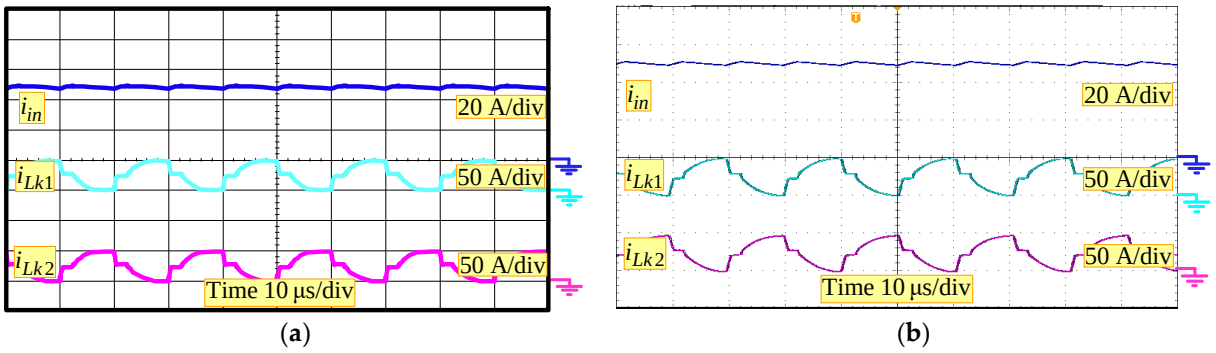
(**a**) (**b**)

Figure 16. Waveforms of gating signals, output voltage and input voltage: (**a**) Simulated waveforms; (**b**) Experimental waveforms.



(**a**) (**b**)

Figure 17. Waveforms of gate signals and drain-source voltages: (**a**) Simulated waveforms; (**b**) Experimental waveforms.



(**a**) (**b**)

Figure 18. Waveforms of input current and leakage currents: (**a**) Simulated waveforms; (**b**) Experimental waveforms.

The waveforms of the gating signals v_{gs1} and v_{gs2} of the switches, output voltage and input voltage are illustrated in Figure 16. The voltage conversion ratio was over 16 times with $V_o = 400$ V and $V_{in} = 24$ V. It was verified that the converter achieved high voltage gain without a very large duty ratio.

Figure 17 illustrates the waveforms of the gating signals and the switch voltages v_{ds1} and v_{ds2}. The maximum switch voltage was slightly more than 50 V. The switch voltage stress was much lower than the output voltage 400 V. Clearly, the switches of the proposed converter had low voltage stress.

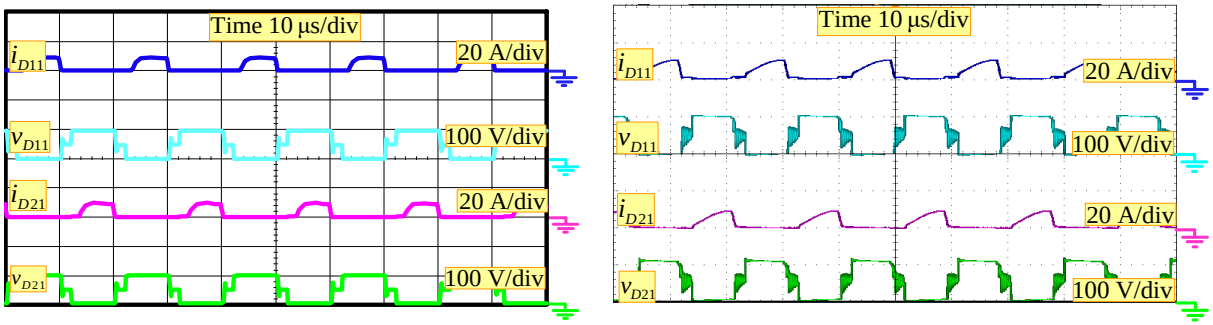


Figure 19. Current and voltage waveforms of the regenerative diodes: (**a**) Simulated waveforms; (**b**) Experimental waveforms.

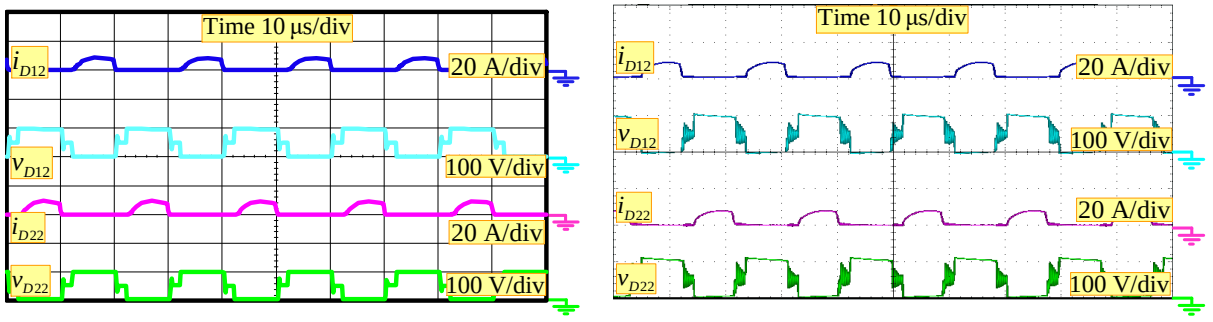


Figure 20. Current and voltage waveforms of the voltage-doubler diodes: (**a**) Simulated waveforms; (**b**) Experimental waveforms.

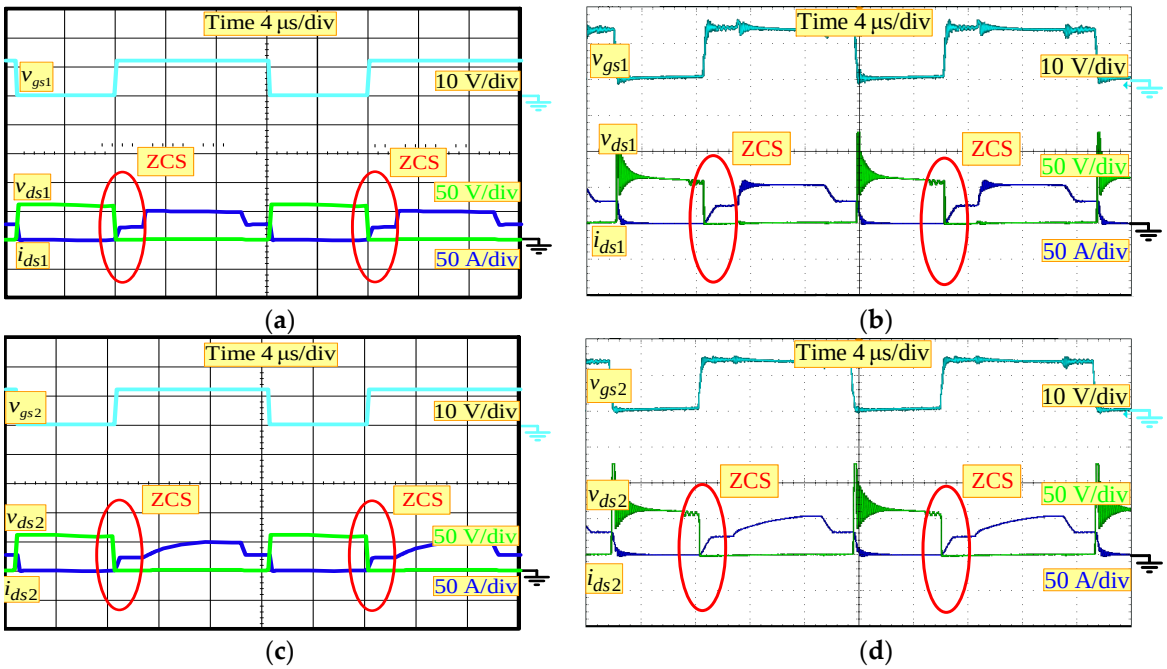


Figure 21. ZCS soft-switching waveforms of the switches: (**a**,**c**) Simulated waveforms; (**b**,**d**) Experimental waveforms.

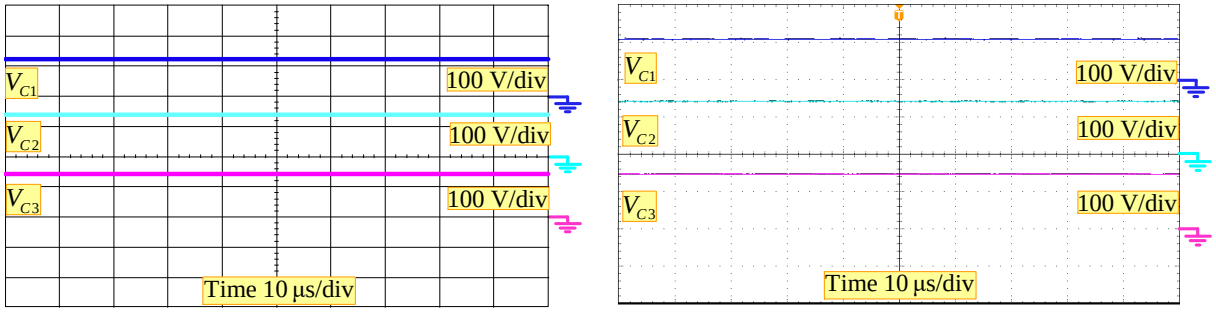


Figure 22. Voltage waveforms of the output capacitors: (**a**) Simulated waveforms; (**b**) Experimental waveforms.

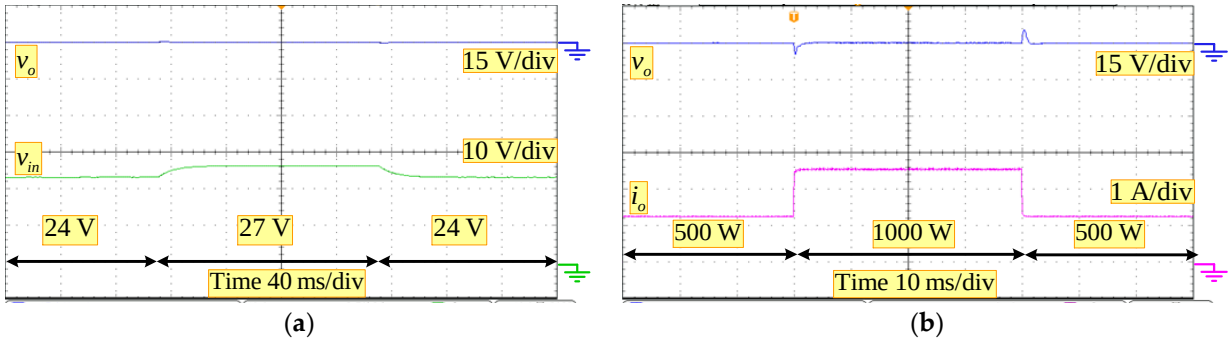


Figure 23. Output voltage response. (**a**) Input voltage variation; (**b**) Load current change.

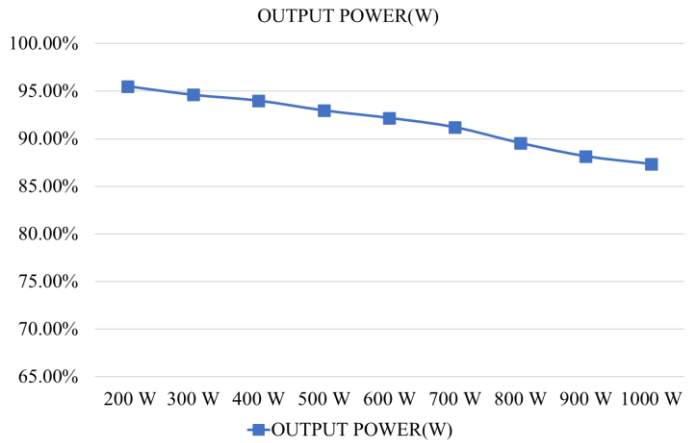


Figure 24. Measured efficiency.

The waveforms of the input current i_{in}, the leakage currents i_{Lk1} and i_{Lk2} are shown in Figure 18. The input parallel structure of two-phase shares the input current to reduce the current stress of power devices. On the other hand, the ripple currents of i_{Lk1} and i_{Lk2} were almost the same, with an amplitude of 49 A. The current ripple cancellation was achieved, due to the interleaved operation, such that the ripple current of i_{in} reduced to only 2 A. It was verified that the interleaved operation could reduce the input current ripple for the parallel input structure.

The current and voltage waveforms of the regenerative diodes D_{11} and D_{21}, as well as those of the voltage-doubler diodes D_{12} and D_{22}, are shown in Figures 19 and 20, respectively. It can be seen that there were no reverse-recovery currents, due to the ZCS turn-off feature. The voltage stresses were equal to 100 V, which was only one-fourth of the output voltage. The measured results agreed with the analyzed results.

Figure 21 shows the switch current and voltage waveforms. The switch currents i_{ds1} and i_{ds2} rose linearly from 0 when each switch began to conduct. The ZCS turn-on performance was achieved to reduce the switching losses.

The voltage waveforms of the output capacitors C_1, C_2 and C_3 are shown in Figure 22. The voltage V_{C1} was slightly more than 100 V and the voltages V_{C2} and V_{C2} were about 150 V, which was in keeping with the results of the analysis. The simulation results were consistent with the experimental results.

Figure 23a shows the output voltage response and the input voltage variation between 24 V and 27 V. On the other hand, the output voltage response and the output current under the step-on and step-off load changes between 500 W and 1000 W are illustrated in Figure 23b. As shown in the figures, the transient ripples of output voltage were clearly very small. The results demonstrated good voltage regulation performance, due to the well-designed controller, for the closed-loop control system.

The measured efficiency of the prototype converter at different output powers is illustrated in Figure 24. The highest efficiency was 95.52% at 200 W, and the efficiency at 1000 W full load was 87.36%.

6. Conclusions

By applying the three-winding coupled-inductor technique, a new high voltage gain interleaved DC–DC converter for renewable energy systems is introduced in this paper. The voltage gain is further extended and the semiconductor voltage stresses are reduced by the voltage multiplier modules. The principle of operation, steady-state analysis, design considerations and controller design are presented. The high voltage conversion ratio is accomplished without a very large duty ratio. The designer can adopt low on-state resistance MOSFETs and low forward voltage drop diodes to reduce the conduction losses, due to their low voltage stresses. With the help of the leakage inductors of the coupled-inductors, the ZCS condition turn-on is intrinsically provided for the switches. The interleaved operation reduces the input current ripple. The leakage energy is recycled to eliminate the voltage spikes on the switches. A performance comparison with other similar converters was carried out to reveal the merits of the introduced converter. Moreover, a closed-loop controller was designed and implemented to ensure effective output voltage regulation. Finally, the simulation and experimental results, using a 1000 W prototype, are provided to validate the derived analysis and to demonstrate the advantages of the presented converter. Thus, the proposed DC-DC converter with high voltage gain and high efficiency is suitable for renewable energy systems.

Author Contributions: This paper was a collaborative work of all the authors. Conceptualization, S.-J.C. and S.-P.Y.; methodology, S.-J.C. and C.-M.H.; software, P.-S.H.; Investigation, S.-J.C. and S.-P.Y.; validation, S.-J.C., S.-P.Y. and P.-S.H.; writing—original draft preparation, S.-J.C.; supervision, C.-M.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Science and Technology Council, Taiwan, under grant No. MOST 111-2637-E-168-002.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Nouri, T.; Nouri, N.; Vosoughi, N. A novel high step-up high efficiency interleaved DC-DC Converter with coupled inductor and built-in transformer for renewable energy systems. *IEEE Trans. Ind. Electron.* **2020**, *67*, 6505–6516. [CrossRef]
2. Tofoli, F.L.; Pereira, D.C.; Paula, W.J.; Junior, D.S.O. Survey on non-isolated high-voltage step-up DC–DC topologies based on the boost converter. *IET Power Electron.* **2015**, *8*, 2044–2057. [CrossRef]
3. Kothapalli, K.R.; Ramteke, M.R.; Suryawanshi, H.M.; Reddi, N.K.; Kalahasthi, R.B. A coupled inductor based high step-up converter for dc microgrid applications. *IEEE Trans. Ind. Electron.* **2021**, *68*, 4927–4940. [CrossRef]
4. Liu, H.; Hu, H.; Wu, H.; Xing, Y.; Batarseh, I. Overview of high-step-up coupled-inductor boost converters. *IEEE Trans. Power Electron.* **2016**, *4*, 689–704. [CrossRef]

5. Azizkandi, M.E.; Sedaghati, F.; Shayeghi, H.; Blaabjerg, F. Two- and three-winding coupled-inductor based high step-up DC-DC converters for sustainable energy applications. *IET Power Electron.* **2020**, *13*, 144–156. [CrossRef]
6. Pereira, A.V.C.; Cavalcanti, M.C.; Azevedo, G.M.; Bradaschia, F.; Neto, R.C.; Carvalho, M.R.S. A novel single-switch high step-up dc–dc converter with three-winding coupled inductor. *Energies* **2021**, *14*, 6288. [CrossRef]
7. Li, W.; Zhao, Y.; Wu, J.; He, X. Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells. *IEEE Trans. Power Electron.* **2012**, *27*, 133–143. [CrossRef]
8. Barbosa, E.A.O.; Carvalho, M.R.S.; Limongi, L.R.; Cavalcanti, M.C.; Barbosa, E.J.; Azevedo, G.M.S. High-gain high-efficiency DC-DC converter with single-core parallel operation switched inductors and rectifier voltage multiplier cell. *Energies* **2021**, *14*, 4634. [CrossRef]
9. Schmitz, L.; Martins, D.C.; Coelho, R.F. Comprehensive conception of high step-up DC-DC converters with coupled inductor and voltage multiplier techniques. *IEEE Trans. Circuits Syst.* **2020**, *67*, 2140–2151. [CrossRef]
10. Alzahrani, A.; Ferdowsi, M.; Shamsi, P. A Family of scalable non-isolated interleaved DC-DC boost converters with voltage multiplier cells. *IEEE Access* **2019**, *7*, 11707–11721. [CrossRef]
11. Andrade, A.M.; Mattos, E.; Schuch, L.; Hey, H.L.; Martions, M.L.D.S. Synthesis and comparative analysis of very high step-up DC-DC converters adopting coupled-inductor and voltage multiplier cells. *IEEE Trans. Power Electron.* **2018**, *33*, 5880–5897. [CrossRef]
12. Nouri, T.; Vosoughi, N.; Hosseini, S.H.; Babaei, E.; Sabahi, M. An interleaved high step-up converter with coupled inductor and built-in transformer voltage multiplier cell techniques. *IEEE Trans. Ind. Electron.* **2019**, *66*, 1894–1905. [CrossRef]
13. Guepfrih, M.F.; Waltrich, G.; Lazzarin, T.B. High step-up DC–DC converter using built-in transformer voltage multiplier cell and dual boost concepts. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 6700–6712. [CrossRef]
14. Tang, Y.; Fu, D.; Wang, T.; Xu, Z. Hybrid switched-inductor converters for high step-up conversion. *IEEE Trans. Ind. Electron.* **2015**, *62*, 1480–1490. [CrossRef]
15. Andrade, J.M.; Coelho, R.F.; Lazzarin, T.B. High step-up DC–DC converter based on modified active switched-inductor and switched-capacitor cells. *IET Power Electron.* **2020**, *13*, 3127–3137. [CrossRef]
16. Salvador, M.A.; Lazzarin, T.B.; Coelho, R.F. High step-up DC-DC converter with active switched-inductor and passive switched-capacitor networks. *IEEE Trans. Ind. Electron.* **2018**, *65*, 5644–5654. [CrossRef]
17. Salvador, M.A.; Andrade, J.M.; Lazzarin, T.B.; Coelho, R.F. Nonisolated high-step-up DC-DC converter derived from switched-inductors and switched-capacitors. *IEEE Trans. Ind. Electron.* **2020**, *67*, 8506–8516. [CrossRef]
18. Duong, T.D.; Nguyen, M.K.; Tran, T.T.; Lim, Y.C.; Choi, J.H. Transformer-less switched-capacitor quasi-switched boost DC-DC converter. *Energies* **2021**, *14*, 6591. [CrossRef]
19. Taghavi, S.S.; Rezvanyvardom, M.; Mirzaei, A.; Gorji, S.A. High step-up three-level soft switching DC-DC converter for photovoltaic generation systems. *Energies* **2023**, *16*, 41. [CrossRef]
20. Rodrigues, J.P.; Mussa, S.A.; Barbi, I.; Perin, A.J. Three-level zero-voltage switching pulse-width modulation DC-DC boost converter with active clamping. *IET Power Electron.* **2010**, *3*, 345–354. [CrossRef]
21. He, L.; Xu, X.; Chen, J.; Sun, J.; Guo, D.; Zeng, T. A plug-play active resonant soft switching for current-autobalance interleaved high step-up DC-DC converter. *IEEE Trans. Power Electron.* **2019**, *34*, 7603–7616. [CrossRef]
22. Eskandari1, R.; Babaei, E.; Sabahil, M.; Ojaghkandi, S.R. Interleaved high step-up zero-voltage zero current switching boost DC-DC converter. *IET Power Electron.* **2020**, *13*, 96–103. [CrossRef]
23. Khorasani, R.R.; Jazi, H.M.; Chaudhuri, N.R.; Sadigh, A.K.; Shaneh, M. An interleaved soft switched high step-up boost converter with high power density for renewable energy applications. *IEEE Trans. Power Electron.* **2022**, *37*, 13782–13798. [CrossRef]
24. Carvalho, M.R.S.; Neto, R.C.; Barbosa, E.J.; Limongi, L.R.; Bradaschia, F.; Cavalcanti, M.C. An overview of voltage boosting techniques and step-up DC-DC converters topologies for pv applications. *Energies* **2021**, *14*, 8230. [CrossRef]
25. Arunkumari, T.; Indragandhi, V. An overview of high voltage conversion ratio DC-DC converter configurations used in DC micro-grid architectures. *Renew. Sustain. Energy Rev.* **2017**, *77*, 670–687. [CrossRef]
26. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Lehmen, B. Step-up DC-DC comprehensive review of voltage-boosting techniques, topologies, and applications. *IEEE Trans. Ind. Electron.* **2017**, *32*, 9143–9178. [CrossRef]
27. Guan, Y.; Cecati, C.; Alonso, J.M.; Zhang, Z. Review of high-frequency high-voltage-conversion-ratio DC-DC converters. *IEEE Trans. Ind. Electron.* **2021**, *2*, 374–389. [CrossRef]
28. Nouri, T.; Hosseini, S.H.; Babaei, E.; Ebrahimi, J. Interleaved high step-up DC-DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell. *IET Power Electron.* **2015**, *8*, 175–189. [CrossRef]
29. He, L.; Liao, Y. An advanced current-autobalance high step-up converter with a multicoupled inductor and voltage multiplier for a renewable power generation system. *IEEE Trans. Power Electron.* **2016**, *31*, 6992–7005.
30. Chen, S.J.; Yang, S.P.; Huang, C.M.; Chou, H.M.; Shen, M.J. Interleaved high step-up DC-DC converter based on voltage multiplier cell and voltage-stacking techniques for renewable energy applications. *Energies* **2018**, *11*, 1632. [CrossRef]
31. Salehi, S.M.; Dehghan, S.M.; Hasanzadeh, S. Interleaved-input series output ultra-high voltage gain DC-DC converter. *IEEE Trans. Power Electron.* **2019**, *34*, 3397–3406. [CrossRef]
32. Chen, S.J.; Yang, S.P.; Huang, C.M.; Chen, Y.H. Interleaved high step-up DC-DC converter with voltage-lift and voltage-stack techniques for photovoltaic systems. *Energies* **2020**, *13*, 2537. [CrossRef]

33. Rahimi, R.; Habibi, S.; Ferdowsi, M.; Shamsi, P. A three-winding coupled inductor-based interleaved high-voltage gain DC-DC converter for photovoltaic systems. *IEEE Trans. Power Electron.* **2022**, *37*, 990–1002. [CrossRef]
34. Venable, D. The K factor: A new mathematical tool for stability analysis and synthesis. *Proc. Powercon* **1983**, *10*, 1–12.