Analysis and Design of a Transformerless Boost Inverter for Stand-Alone Photovoltaic Generation Systems

Zhixiang Yu, Xuefeng Hu, Zhilei Yao, Lezhu Chen, Meng Zhang, and Shunde Jiang

***Abstract*—A novel transformerless boost inverter for stand-alone photovoltaic generation systems is proposed in this paper. The proposed inverter combines the boost converter with the traditional bridge inverter. The switch S_1 not only realizes the boost function but also participates in inverting process. The inverter has a higher voltage gain and good characteristics when the inductor L_1 is operated in discontinuous mode (DCM) and the nonpolarized capacitor can be chosen as bus capacitor, which makes the volume smaller and the service life of the inverter is increased. The inverter consists of five switches in which only two switches are operated at high frequency state and a monopole sinusoidal pulse width modulation (SPWM) strategy is used. Therefore, the modulation strategy of switches is very simple and the switching loss is reduced. The principle of inverter is described in detail and mathematical models are built by small-signal analysis. Finally, the correctness of the theoretical analysis is verified by simulation and experiment.**

***Index Terms*—Boost inverter, discontinuous mode (DCM), monopole sinusoidal pulse width modulation (SPWM), nonpolarized capacitor, photovoltaic generation systems, transformerless.**

I. Introduction

In the last ten years, the photovoltaic (PV) power systems have become very popular among the renewable energy sources[1]−[28]. Normally, the inverter is the key interface between the solar cells and the AC load. However, the output voltage of the PV systems is generally low. Consequently, inverters need to have the ability to boost the output voltage of PV in order to maintain a stable AC voltage for the load [1]−[2].

The traditional voltage source inverter is a step-down inverter. When the input voltage is low, the traditional voltage source inverter is usually added a DC-DC boost circuit at its front stage. So the step-up inverter can be realized by cascading the DC-DC converter and the traditional full bridge inverter [3]. However, due to the large number of switching devices, complex control strategy and higher cost in this two stages inverter. The flyback micro-inverter can step up the input voltage, and isolate the output and the input. However, the volume and cost of the inverter are relatively high due to the existence of transformers. Some single stage boost inverters are studied in [1]−[20], for example: Z source inverter [4]−[5], double Boost inverter [8]−[9], double Cuk integrated inverter [10]−[11], Buck-Boost integrated inverter [12]−[13] and so on. The typical Z source inverter can achieve the function of the boost by using the controlled direct connection of the upper and lower bridge arm power switches. However, it has many disadvantages, such as complex topology, starting shock and oscillation, voltage gain restricted by duty cycle and modulation ratio. The inverter is a combination of two improved Cuk DC converters by input series and output parallel in [10]. By setting the appropriate regulator, the inverter can obtain good dynamic and static performance. However, the inverter requires two independent input power supplies and two independent boost inductors, which leads to low utilization rate of power source and the large volume of the circuit. Moreover, the voltage gain of the inverter circuit is low. The inverter proposed in [11] is composed of an inverting and a non inverting Cuk converter. Due to the inherent up-down voltage capacity of the Cuk converter, the output voltage can be higher or lower than the input voltage. But the inverter has six switches and four switches are operated at high frequency, so it is a challenge to improve the efficiency of the inverter.

A new boost transformerless photovoltaic inverter is proposed in this paper, which integrates boost converter with the traditional full bridge inverter. The inverter has characteristics of high gain, high integration, few power devices and easy to control. Moreover, the proposed inverter adopts monopole sinusoidal pulse width modulation (SPWM) strategy to realize the voltage pumping and the control of output voltage.

II. A Novel Transformerless Step-Up Inverter

A. The Topology of Proposed Inverter

This paper presents a boost transformerless inverter topology,

Manuscript received July 15, 2019; revised September 4, 2019; accepted September 12, 2019. Date of publication December 30, 2019; date of current version November 19, 2019. This work was supported by the National Natural Science Foundation (51577002), Top-notch Personnel Foundation of the Anhui Higher Education Institutions of China (gxbjZD13). This paper was presented in part at the 2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Xi'an, China, June 2019.

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Digital Object Identifier 10.24295/CPSSTPEA.2019.00029

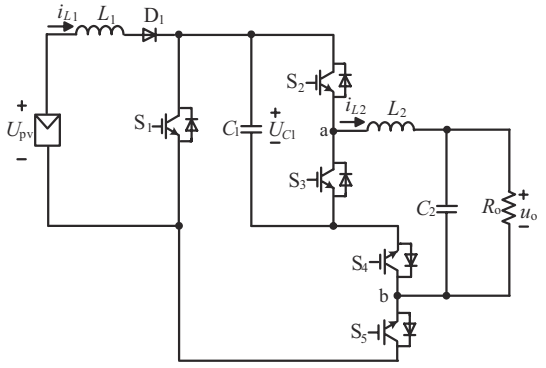

Fig. 1. The configuration of proposed inverter.

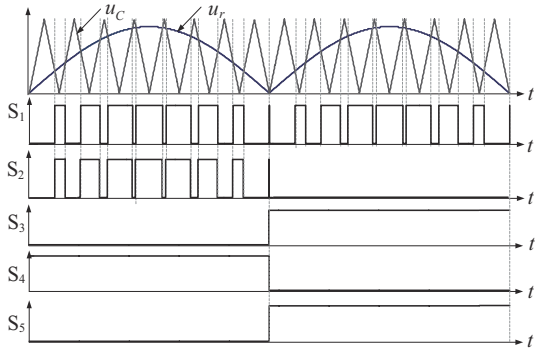

Fig. 2. The modulation of power switches.

as shown in Fig. 1. The topology consists of five power switches S_1~S_5, two energy storage components, inductance L_1 and capacitance C_1, load resistor R_O, filter inductance L_2, filter capacitor C_2, diode D_1. The body diode of the power switches S_1~S_5 is respectively called D_{S1}~D_{S5}. It can be seen that the proposed inverter is integrated with boost converter and the traditional full bridge inverter by sharing the power device S_1. The DC power source is supplied to the inductor L_1 through S_1 and the voltage ripple of capacitor C_1 is smaller in the steady state. The diode D_1 compel the energy to flow from the DC power source to the load. In order to simplify circuit analysis, the assumptions are as follows:

① The filter inductor L_2 is large enough and its current is essentially constant in one switching period. ② All power switches, diodes, inductors and capacitors are ideal components, that is, the effect of parasitic parameters is not considered. ③ The capacitors C_1 and C_2 are large enough to keep U_{C1} and U_{C2} constant during a switching period.

B. Analysis of Operational Principle

The power switches of the inverter are based on monopole SPWM and the modulation strategy is shown in Fig. 2. The SPWM signal used by the switch S_1 is generated by the comparison of the absolute value of the sine wave as modulation wave with the triangle wave as the carrier wave. The control signal of the switch S_2 is the same as that of the S_1 when it works in the positive half cycle of sine wave. While it is turned off in the negative half cycle of the sine wave.

TABLE I
SWITCHING SEQUENCE OF PROPOSED INVERTER

	S_1 /D_{S1}	S_2 /D_{S2}	S_3 /D_{S3}	S_4 /D_{S4}	S_5 /D_{S5}
Mode I	1/0	1/0	0/0	1/0	0/0
Mode II	0/0	0/0	0/1	1/1	0/1
Mode III	0/0	0/0	0/1	1/0	0/0
Mode IV	1/0	0/0	1/0	0/0	1/0
Mode V	0/0	0/0	1/0	0/1	1/1
Mode VI	0/0	0/0	1/0	0/1	1/0

The proposed inverter operates in discontinuous current mode of boost inductor. Table I shows the switching sequence of the proposed inverter in one switching cycle. There are six operating modes in one switching cycle. The six operating modes of the circuit are shown in Fig. 3. The mode I, II and III operate in the positive half period of the output voltage. While the mode IV, V and VI operate in the negative half cycle. The respective analysis is as follows and the key waveforms of the proposed inverter in discontinuous mode (DCM) are shown in Fig. 4.

The power switches S_1 and S_2 operate at high frequency in the positive half cycle. So they are in the alternating state of turn-on and turn-off. The power switches S_3 and S_5 are in turn-off state and the power switch S_4 is conducted. The circuit has six modes of operation.

Mode I [t_0~t_1] The equivalent circuit is shown in Fig. 3(a). At $t = t_0$, the switches S_1, S_2, S_4 and diode D_1 are turned on. While switch S_3 and S_5 are turned off. At this moment, the input DC power U_{in} charges the inductor L_1 through the diode D_1 and the power switch S_1. The inductance current i_{L1} increases linearly. The capacitor C_1 charges the inductor L_2 and supplies power to the R_O through switches S_2 and S_4.

$$i_{L1}(t) = \frac{U_{in}}{L_1}(t - t_0) + i_{L1}(t_0) \tag{1}$$

Mode II [t_1~t_2] The equivalent circuit is shown in Fig. 3(b). At $t = t_1$, the switch S_4 and diode D_{S3} are turned on. Switches S_1, S_2, S_3 and S_5 are turned off. At this moment, the U_{in} and L_1 charge C_1 through the D_1 and D_{S4}. The i_{L2} can not change suddenly at the load terminal. So L_2 continues to charge R_O through D_{S3}. At the moment of t_2, i_{L1} is linearly reduced zero.

$$i_{L1}(t) = \frac{U_{in} - U_{C1}}{L_1}(t - t_1) + i_{L1}(t_1) \tag{2}$$

Mode III [t_2~t_3] The equivalent circuit is shown in Fig.3(c). At $t = t_2$, the switch S_4 is still turned on. Switches S_1, S_2, S_3 and S_5 are turned off. At this moment, there is no charging loop because the inductance current i_{L1} is zero. The inductor L_2 continues to charge the load R_O through the body diode D_{S3} until t_3 and the mode III ends.

$$i_{L1}(t) = 0 \tag{3}$$

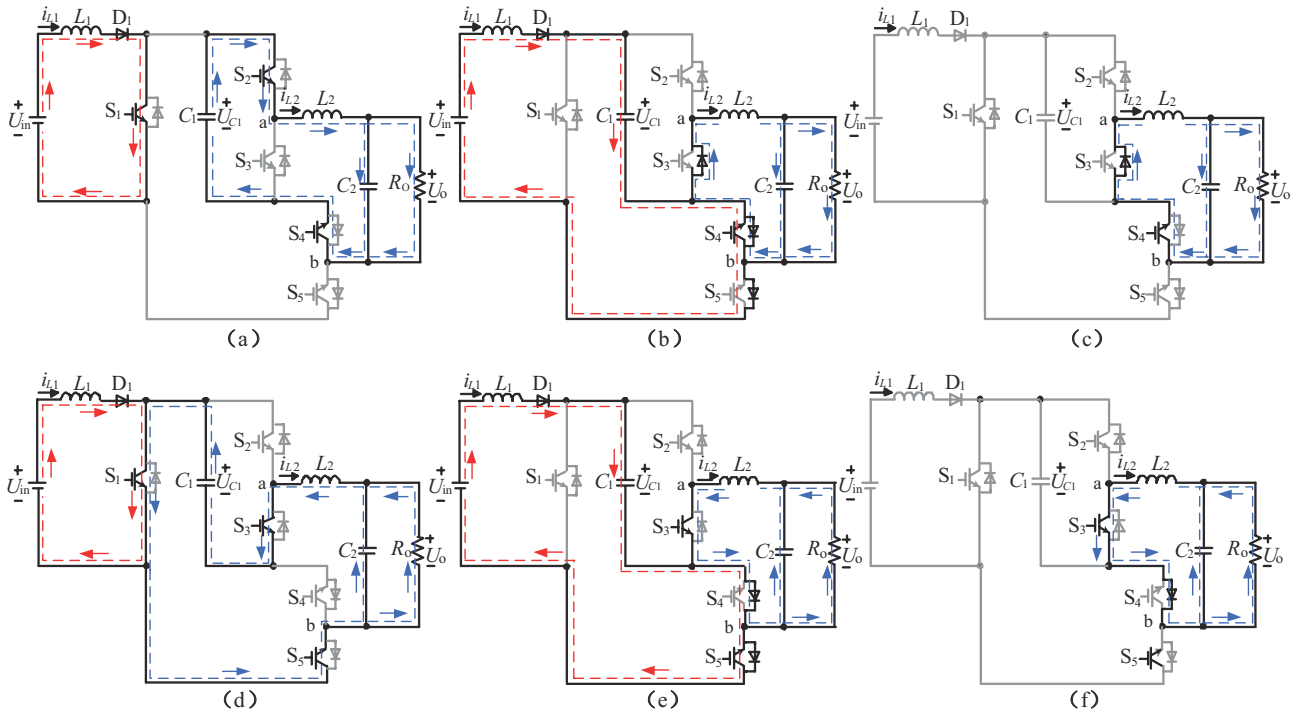

Fig. 3. Equivalent modal diagram of circuit. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

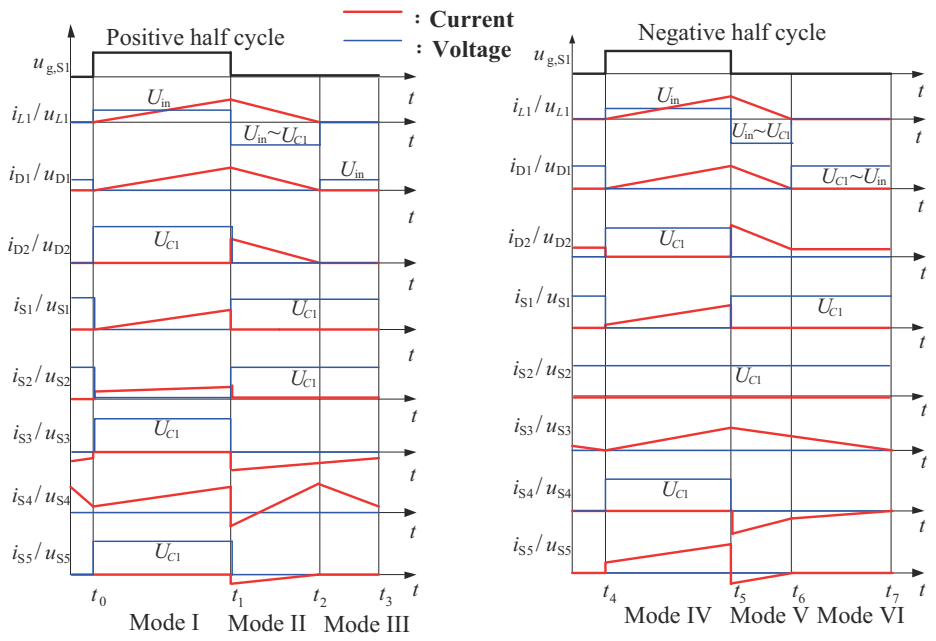

Fig. 4. The key waveforms of the proposed converter in DCM operation.

Mode IV [t_4~t_5] The equivalent circuit is shown in Fig. 3(d). At $t = t_4$, switches S_1, S_3 and S_5 are turned on. While S_2 and S_4 are turned off. At this moment, U_{in} charges L_1 through the diode D_1 and the switch S_1. The i_{L1} increases linearly. The capacitor C_1 charges the inductor L_2 and supplies power to the R_O through switches S_1, S_3 and S_5. At $t = t_5$, the mode IV ends.

$$i_{L1}(t) = \frac{U_{in}}{L_1}(t - t_4) + i_{L1}(t_4) \tag{4}$$

Mode V [t_5~t_6] The equivalent circuit is shown in Fig. 3(e). At $t = t_5$, switches S_3 and S_5 are turned on while switches S_1, S_2 and S_4 are turned off. At this moment, the input power U_{in} and L_1 charge C_1 through D_1 and D_{S4}. The i_{L2} can not change suddenly at the load terminal, so the inductance L_2 continues to charge R_O through S_3 and D_{S4}. At the moment of t_6, the i_{L1} is linearly reduced zero and the mode V ends.

$$i_{L1}(t) = \frac{U_{in} - U_{C1}}{L_1}(t - t_5) + i_{L1}(t_5) \tag{5}$$

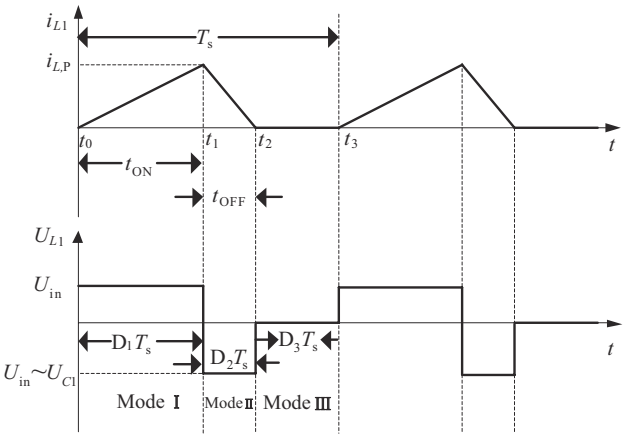

Fig. 5. The current and voltage waveform of inductance in DCM.

Mode VI [t_6~t_7] The equivalent circuit is shown in Fig. 3(f). At $t = t_6$, switches S_3 and S_5 are still turned on. Switches S_1, S_2 and S_4 are turned off. At this moment, there is no charging loop because the inductance current i_{L1} is zero. L_2 continues to charge R_O through S_3 and D_{S4} until t_7 and the mode VI ends.

$$i_{L1}(t) = 0 \tag{6}$$

III. Voltage Gain and Parameters of the Proposed Inverter

A. Analysis of Voltage Gain

From the above analysis, one can see that the duty cycle d_i of the signal S_1 in each carrier period varies. Assuming that the duty ratio of S_1 is d_i in i carrier cycle. The m is the modulation ratio. According to the regular symmetry sampling rule in [21], the duty cycle can be expressed as (7).

$$d_i = m\sin\omega t_i \tag{7}$$

Since the inductance L_1 of the inverter operates in DCM, the i_{L1} reaches the maximum value I_{LP} at the moment of t_1 and drops to zero when the time is t_2. The current i_{L1} remains zero between the time of t_2 and t_3. As you can see from Fig. 5, the formula can be obtained as follows: $d_i' = (t_2 - t_1)/T_S$, $d_i + d_i' < 1$.

According to the voltage second balance of inductor L_1, the following equation can be expressed as:

$$U_{in} d_i T_S = (U_{C1} - U_{in}) d_i' T_S. \tag{8}$$

If the loss of all components in this circuit is neglected, the input power is equal to the output power and thus the formula can be obtained as:

$$U_{in} I_{in} = (U_{om}/\sqrt{2})^2/R_O. \tag{9}$$

where U_{om} is amplitude of the output voltage of the inverter.

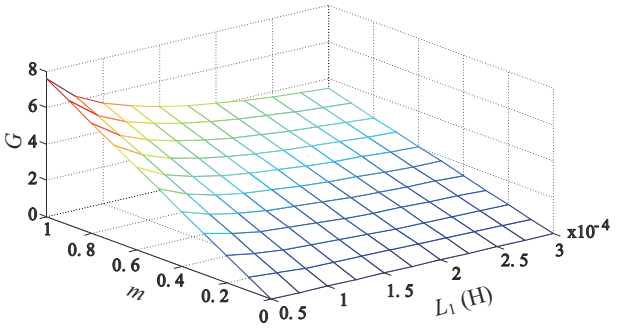

Fig. 6. Diagram of voltage gain G and L_1, m.

It can be expressed as: $U_{om} = mU_{C1}$. Since the input average current is equal to the inductance average current, the following equations can be written as:

$$I_{in} = I_{L1}, \tag{10}$$

and the average value of i_{L1} can be obtained as:

$$I_{L1} = (d_i + d_i')I_{LP}/2. \tag{11}$$

According to (8)~(11), the equations of the input voltage and the DC bus voltage can be derived as:

$$\frac{U_{C1}}{U_{in}} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{4d_i^2 T_S R_O}{L_1 m^2}}\right). \tag{12}$$

The d_i is taken as the valid value and the voltage gain can be expressed as:

$$G = \frac{U_{om}}{U_{in}} = \frac{m}{2}\left(1 + \sqrt{1 + \frac{2T_S R_O}{L_1}}\right). \tag{13}$$

Fig. 6 shows the three-dimensional relationships of voltage gain G versus inductance L_1 and modulation ratio m when f_S = 20 kHz, R_O = 100 Ω are given. As can be seen from Fig. 6, the G increases when the m increases or the L_1 decreases.

B. Range of Modulation Ratio m

The range of modulation ratio m is discussed based on the open-loop condition. According to (8), the d_i' can be obtained as:

$$d_i' = \frac{U_{in} d_i}{U_{C1} - U_{in}}. \tag{14}$$

Because $d_i + d_i' < 1$, the duty cycle d_i can be expressed as:

$$d_i < \frac{1}{\frac{U_{in}}{(U_{C1} - U_{in})} + 1}. \tag{15}$$

According to (7), $\sin\omega t_i \in (0\ \ 1)$, the range of modulation ratio m can be derived as:

$$m < \frac{1}{\frac{U_{\text{in}}}{(U_{C1} - U_{\text{in}})} + 1}. \tag{16}$$

When the intermediate variable U_{C1} is represented by an independent variable m. According to (16), the range of modulation ratio m can be derived as:

$$m < \frac{U_{\text{om}}}{U_{\text{om}} + U_{\text{in}}}. \tag{17}$$

C. The Value of Boost Inductor

In order to ensure the inverter is operated in DCM, the critical inductance of the boost inverter is derived firstly.

When the boost inductor works in DCM, the inductance current is exactly zero at the start and at the end of each switching cycle. The average current of inductance is equal to half of the variation of inductance current. It is assumed that the threshold inductance is L_{C}. According to (10) and (11), the following equation can be expressed as:

$$I_{\text{in}} = I_{L_{\text{C}}} = I_{L,\text{P}}/2. \tag{18}$$

The formula between current and voltage is as follows:

$$I_{L,\text{P}} = U_{\text{in}} d_i T_{\text{S}}/L_{\text{C}}. \tag{19}$$

According to (9), (18) and (19), the following equation can be derived as:

$$U_{\text{in}} d_i T_{\text{S}}/(2L_{\text{C}}) = m^2 U_{C1}^2/(2R_{\text{O}} U_{\text{in}}). \tag{20}$$

The critical inductance L_{C} can be obtained as:

$$L_{\text{C}} = U_{\text{in}}^2 d_i T_{\text{S}} R_{\text{O}}/U_{\text{om}}^2. \tag{21}$$

As we can see from (21), L_{C} is related to input voltage, load and modulation ratio. In order to ensure the inductor current is always discontinuous throughout the entire range of U_{in}. The value of the inductor should be less than L_{C}. The three-dimensional image of the inductance L_{C} is shown in Fig. 7, in which $d_i = 0.7$, $f = 20$ kHz, $U_{\text{om}} = 155$ V.

D. Design of the Bus Capacitor

During the operation of the boost inverter, the design of the capacitor mainly considers the voltage stress and the maximum acceptable voltage ripple across it. The capacitor is charged and discharged continuously with the change of the power switch state. The relation between the charge quantity and the capacitance value is satisfied as follow:

$$\Delta Q = C\Delta U_{C1} = I_C \Delta T. \tag{22}$$

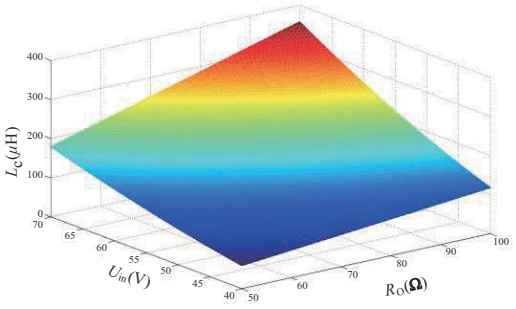

Fig. 7. Three-dimensional image of the threshold inductance L_{C}.

In a switching cycle, ΔQ is the quantity of charge during charging or discharging process of capacitors. ΔU_{C1} is the value of the capacitor voltage ripple. I_C is the average current of capacitor during charging or discharging process. ΔT is the charging time or discharging time. Therefore, the value of the capacitor can be selected according to (23), in which P_{O} represents the output power.

$$C_1 \geqslant \frac{P_{\text{O}} d_i}{(U_{C1} - U_{\text{in}})\Delta U_{C1} f_{\text{S}}} \tag{23}$$

In order to ensure the performance of the inverter, the value of capacitor voltage ripple is limited to 1% of U_{C1}. Thus, the value of C_1 should be greater than 15 μF. The capacitor value of the inverter is selected for 47 μF.

E. Design of Filter Inductor and Capacitor

The design method of filter inductance and capacitor is K low-pass filter in proposed inverter refer to the design in reference [22]. This design method can be expressed as: $K = R^2 = L/C$, $R = (0.5\text{–}0.8)R_{\text{O}}$.

The cut-off frequency f_{C} is increased by 10 times, which is the carrier frequency f_{S}. And then:

$$L = \frac{R}{2\pi f_{\text{C}}} \tag{24}$$

$$C = \frac{1}{2\pi f_{\text{C}} R}. \tag{25}$$

It is calculated that the value of L_2 is 3.7 mH and the value of C_2 is 1.3 μF. Therefore, the value of filter inductance and filter capacitor is respectively 3 mH and 10 μF in proposed inverter.

IV. Inverter Modeling and Controller Design

A. Inverter Modeling

This paper builds a state space averaged model to obtain a linearized model of the proposed inverter. In addition, designing a suitable controller to achieve good steady-state performance and dynamic characteristics by small-signal analysis. To simplify the analysis, following assumptions are made. Components including capacitors and inductors are ideal

devices, regardless of the effects of parasitic parameters and the initial conditions of elements are zero. Inductor currents (i_{L1}, i_{L2}) and capacitor voltages (U_{C1}, U_{C2}) are considered as state variables x.

$$x = \begin{bmatrix} i_{L1} & i_{L2} & U_{C1} & U_{C2} \end{bmatrix}^T \tag{26}$$

The input voltage (U_{in}) is selected as the input variable u, and the output voltage (U_O) is the output variable y, and the state space equation can be written:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases}. \tag{27}$$

The expressions for the state variables during three operating modes are given in Table II.

For easier analysis, the duty ratio weighting factor of the converter mode I is D_1 ($D_1 = d_i$), the duty ratio weighting factor of the mode II is D_2 ($D_2 = d_i'$), and the duty ratio weighting factor of the mode III is D_3 ($D_3 = 1 - d_i - d_i'$). By using the average state space method, the coefficient matrixes A, B and C can be calculated by the following formulas:

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{D_1}{L_2} & -\dfrac{1}{L_2} \\ \dfrac{D_2}{C_1} & -\dfrac{D_1}{C_1} & 0 & 0 \\ 0 & \dfrac{1}{C_2} & 0 & -\dfrac{1}{RC_2} \end{bmatrix} \tag{28}$$

$$B = \begin{bmatrix} D_1 + D_2 & 0 & 0 & 0 \end{bmatrix}^T \tag{29}$$

$$C = [0 \;\; 0 \;\; 0 \;\; 1]. \tag{30}$$

Perturbations in the steady-state values of state variables and the duty cycle are as follows:

$$\begin{cases} x = X + \hat{x} \\ d_1 = D_1 + \hat{d}_1 \\ d_2 = D_2 + \hat{d}_2 \\ u = U + \hat{u} \\ y = Y + \hat{y} \end{cases}, \tag{31}$$

where $\hat{x}$, $\hat{d}_1$, $\hat{d}_2$, $\hat{u}$, $\hat{y}$ are the state variable x, the duty cycle d_1, the duty cycle d_2, the input voltage u, and the disturbance component near the y static operating point. Substituting (31) into (8), the relationship between $\hat{d}_1$ and $\hat{d}_2$ can be obtained as follow:

$$\hat{d}_2 = \frac{U_{in}\hat{d}_1 - D_2\hat{U}_{C1}}{U_{C1} - U_{in}}. \tag{32}$$

TABLE II
EXPRESSIONS FOR INDUCTOR VOLTAGES AND CAPACITOR CURRENTS OF THE INVERTER IN THE POSITIVE HALF CYCLE

	Mode I D_1T_S	Mode II D_2T_S ($i_{L1} > 0$)	Mode III D_3T_S ($i_{L1} = 0$)
U_{L1}	U_{in}	$U_{in} - U_{C1}$	0
U_{L2}	$U_{C1} - U_{C2}$	$-U_{C2}$	$-U_{C2}$
i_{C1}	$-i_{L2}$	i_{L1}	0
i_{C2}	$i_{L2} - U_{C2}/R_o$	$i_{L2} - U_{C2}/R_o$	$i_{L2} - U_{C2}/R_o$

Substituting (31), (32) into (27) and writing $\hat{d}_2$ in terms of $\hat{d}_1$ and neglecting higher order terms, small-signal AC model represented in matrix form is obtained as:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\hat{u} + E\hat{d} \\ \hat{y} = C\hat{x} \end{cases}, \tag{33}$$

where the coefficient matrixes A, B, E and C can be calculated by the following formulas:

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{D_1}{L_2} & -\dfrac{1}{L_2} \\ \dfrac{D_2}{C_1} & -\dfrac{D_1}{C_1} & \dfrac{D_2 i_{L1}}{C_1(U_{in} - U_{C1})} & 0 \\ 0 & \dfrac{1}{C_2} & 0 & -\dfrac{1}{RC_2} \end{bmatrix} \tag{34}$$

$$B = [0 \;\; 0 \;\; 0 \;\; 0]^T \tag{35}$$

$$E = \begin{bmatrix} 0 & \dfrac{U_{C1}}{L_1} & -\dfrac{i_{L2}}{C_1} + \dfrac{U_{in} i_{L1}}{C_1(U_{C1} - U_{in})} & 0 \end{bmatrix} \tag{36}$$

$$C = [0 \;\; 0 \;\; 0 \;\; 1] \tag{37}$$

Based on the small signal model given by (33) and the control (d) to output voltage (U_O) transfer function $G_p(s)$ is obtained as follow:

$$G_P(s) = \left.\frac{y(s)}{d(s)}\right|_{U(s)=0} = \left.\frac{U_O(s)}{d(s)}\right|_{U(s)=0} = C(SI - A)^{-1}E \tag{38}$$

Using the parameters given in Table III, the transfer function $G_p(s)$ can be obtained as (39).

$$G_P(s) = \frac{\hat{U}_O(s)}{\hat{d}(s)} = \frac{4.68 \times 10^9 S + 1.673 \times 10^{12}}{S^3 + 7 \times 10^3 S^2 + 5.88 \times 10^7 S + 2.36 \times 10^{10}} \tag{39}$$

B. Controller Design

In addition, it is necessary to design a suitable controller

TABLE III
PARAMETERS OF INVERTER CIRCUIT

Experimental variable	Value
DC input voltage U_{in}	45~70 V
AC output voltage u_O	110/50 V(Hz)
Switching frequency f_S	20 kHz
Rated power P_O	200 W
DC boost inductor L_1	110 μH
DC bus capacitor C_1	47 μF
Switch S_1~S_5	BSM100GB60DLC
Diode D_1	RHRG3060
Filter inductance L_2	3 mH
Filter capacitor C_2	10 μF

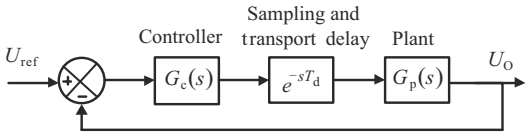

Fig. 8. Voltage control block diagram.

to achieve a good steady-state performance and dynamic characteristics. PR controller is advantageous in tracking sinusoidal signals as it provides a high gain at grid frequency, thereby eliminating the steady state error [23]. Fig. 8 shows the block diagram representation of the voltage control loop including the PR controller $G_c(s)$. As shown in Fig. 8, these delays are added and incorporated into the control loop as e^{-sT_d}, where $T_d = 0.75\ T_s$. To minimize the steady state error at grid frequency, PR controller is tuned to grid frequency of 50 Hz. This ensures high loop gain at the grid frequency. The transfer function is as follow:

$$T_c(s) = \frac{S^2 + \zeta_z \omega S + \omega^2}{S^2 + \zeta_p \omega S + \omega^2}, \tag{40}$$

where ω is the required frequency, ζ_z and ζ_p are the damping coefficients [24].

The controller gain depends on the ratio of the damping coefficients. For a steady state error of 0.1%, values of ζ_z and ζ_p are obtained as 1 and 0.5 respectively.

The Bode plot of $G_p(s)$ and the open loop gain $G(s) = G_c(s) \times e^{-sT_d} \times G_p(s)$ are shown in Fig. 9. It can be seen that the gain is high at resonant frequency, which is the grid frequency and hence, the steady state error is negligible at grid frequency.

V. SIMULATION AND EXPERIMENTAL VERIFICATIONS

In order to verify the correctness of the feasibility and theoretical analysis of the proposed boost inverter in this paper, the simulation is carried out firstly. Then, an experimental prototype taking DSP320F2812 as core controller is built to verify the performance of inverter. The specific parameters are shown in Table III. Fig. 10 shows the external view of the prototype.

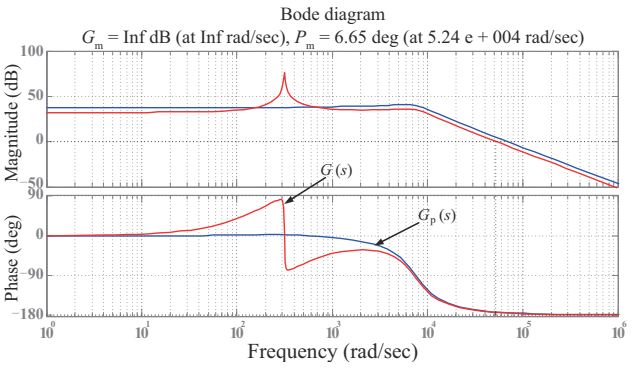

Fig. 9. Bode plots of the transfer functions $G_p(s)$ and $G(s)$.

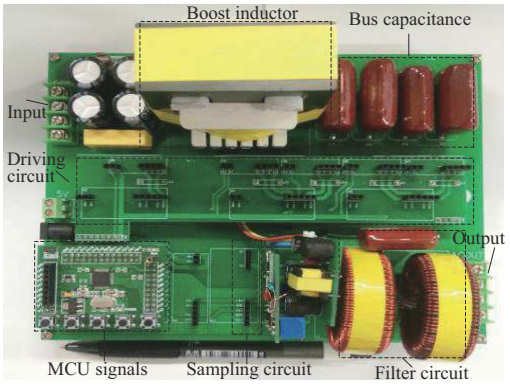

Fig. 10. The external view of the proposed inverter.

The modulation ratio m is 0.7 and the input voltage U_{in} is 45 V. The waveforms of the inverter are shown in Fig. 11. Fig. 11(a) shows the driving signals of all switches. Fig. 11(b) shows the output voltage of inverter and the current of input inductor L_1. Fig. 11(c) shows the DC bus voltage u_{C1} and the output voltage across the load. The current through the filter L_2 and output current are shown in Fig. 11(d). Fig. 12 is experimental waveform of the voltage stress for power devices. The measured efficiency under different input voltage are shown in Fig. 13. The performance comparison with the single stage topologies in [25]–[26] is presented in Table IV.

VI. CONCLUSIONS

A transformerless boost inverter topology for stand-alone photovoltaic generation systems is proposed in this paper, which can work in a wide input voltage range. The integrated boost inverter can be derived from a boost converter and a full bridge inverter by multiplexing the switch of basic boost converter. In the proposed inverter, only one power device is operated at high frequency in a line frequency cycle, the other one is operated at high frequency in half cycle, and the rest switches are all operated in low frequency of 50 Hz. In addition, values of the boost inductor L_1 and the bus capacitor C_1 can be designed to be very small so that the volume and the cost of the circuit are significantly reduced. The operating principle and steady-state characteristics of the inverter are analyzed in detail when the input inductor current is designed in DCM. The correction of the theoretical analysis is proved by

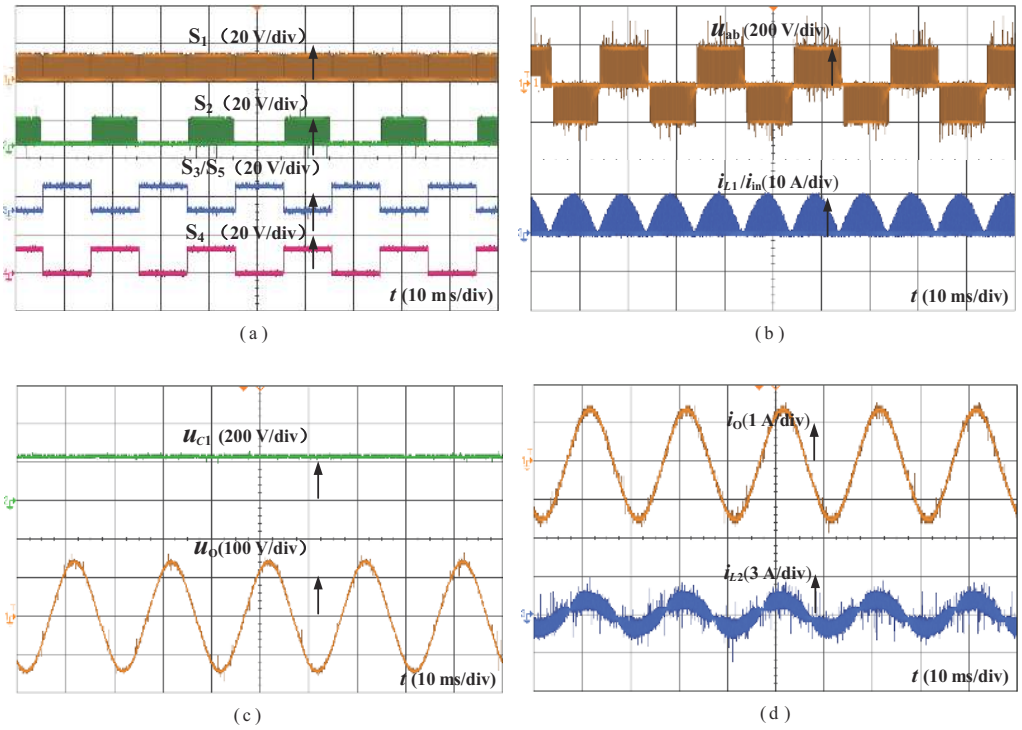

Fig. 11. Experimental waveforms. (a) $u_{g,S1}$~$u_{g,S5}$. (b) u_{ab}, i_{L1}/i_{in}. (c) u_{C1}, u_O. (d) i_O, i_{L2}.

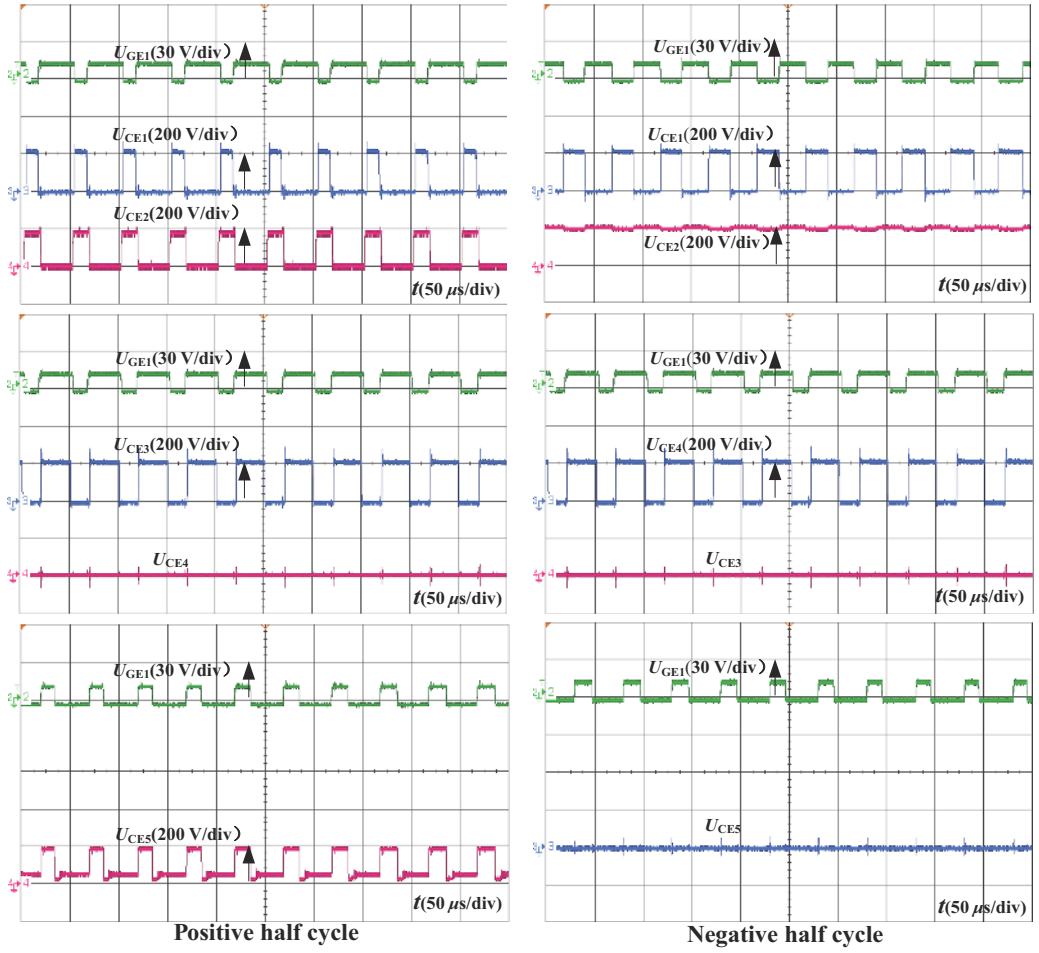

Fig. 12. Experimental waveforms of the power switches.

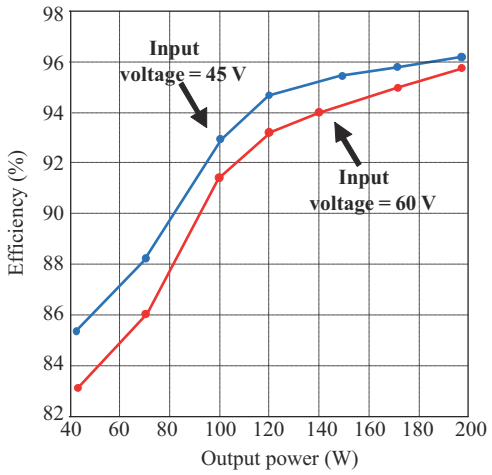

Fig. 13. The efficiency curves for different conditions.

TABLE IV
COMPARISON OF SINGLE-STAGE INVERTER TOPOLOGIES

Topology	Components & Devices				THD (%)	Max.eff (%)
	S	D	L	C		
[25]	4	3	3	2	4	91.3
[26]	6	0	2	2	–	92.6
Proposed	5	1	2	2	1.8	96.2

the experimental waveforms.

REFERENCES

[1] Q. Yang, W. X. Huang, Y. W. Hu, *et al.*, "A new type single stage boost inverter," in *Transactions of China Electrotechnical Society*, vol. 26, no.4, pp.122–127, 2011.

[2] L. Q. Wang, B. N. Zhu, and X. F. Sun, "A single stage isolated type Sepic inverter," in *Transactions of China Electrotechnical Society*, vol. 31, no. 18, pp. 75–82, 2016.

[3] L. Zhang, X. B. Ruan, and X. Y. Ren, "The control method of the front stage DC converter in the two stage inverter," in *Proceedings of the CSEE*, vol. 35, no. 3, pp. 660–670, 2015.

[4] F. Z. Peng, "Z-source inverter," in *IEEE Transcations on Industry Applications*, vol. 39, no. 2, pp. 504–510, 2003.

[5] X. Q. Guo and R. He, "Leakage current reduction of Z-source four-leg inverter for transformerless PV system," *Applied Power Electronics Conference and Exposition (APEC)*, pp: 380–383, 26–30 March 2017.

[6] E. S. Asl, E. Babaei, M. Sabahi, *et al*, "New half-bridge and full-bridge topologies for switched-boost inverter with continuous input current," in *IEEE Transcations on Industrial Electronics*, vol. 65, no. 4, pp. 3188–3197, 2018.

[7] F. A. A. Meinagh, E. Babaei, and H. Tarzamni, "Modified high voltage gain switched boost inverter," in *IET Journals & Magazines*, vol. 10, no. 13, pp.1655–1664, 2017.

[8] R. Hugo, B. Beatriz, and P. Andre, "Single-stage DC-AC converter for photovoltaic system," in *Proceedings ECCE*, pp. 604–610, Sept., 2010.

[9] K. Jha, S. Mishra, and A. Joshi, "High-quality sine wave generation using a differential boost inverter at higher operating frequency," in *IEEE Transcations on Industry Applications*, vol. 51, no. 1, pp.373–384, 2015.

[10] L. Q. Wang and X. Wang, "A novel single-stage non-isolated dual Cuk inverter," *Proceedings of the CSEE*, vol. 34, no. 6, pp. 846–854, 2014.

[11] P. K. Chamarthi, M. Rajeev, and V. Agarwal, "A novel single stage zero leakage current transformer-less inverter for grid connected PV systems," in *Proceedings PVSC*, pp. 1–5, June, 2015.

[12] L. Qin, M. Hu, D. C Lu, Z. Feng, and Y. Wang, "Buck-boost dual-leg-integrated step-up inverter with low THD and single variable control for single-phase high-frequency AC microgrids," in *IEEE Transcations on Power Electronics*, vol. 33, no. 7, pp. 6278–6291, 2018.

[13] A. Alexander and S. Keyue, "High-gain single-stage boosting inverter for photovoltaic applications," in *IEEE Transcations on Power Electronics*, vol. 31, no. 5, pp. 3550–3558, 2016.

[14] B. Zhao, A. Abramovitz, R. Ma, and Y. Huangfu, "High gain single stage buck-boost inverter," in *Proceedings ICEMS*, pp. 1–5, 2017.

[15] T. Sreekanth, N. L. Narasamma, M. K. Mishra, "A high gain grid connected single stage inverter system with reactive power control,"in *Proceedings ICIT*, pp.358–363, 2017.

[16] V. K. Bussa, A. Ahmad, R. K. Singh, and R. Mahanty, "Single-phase high-voltage gain switched LC Z-source inverters," in *IET Journals & Magazines*, vol. 11, no. 5, pp.796–807, 2018.

[17] X. Guo, "A novel CH5 inverter for single-phase transformerless photovoltaic system applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1197–1201, Oct. 2017.

[18] T. Sreekanth, N. Lakshminarasamma, and M. K. Mishra, "Coupled inductor-based single-stage high gain DC–AC buck–boost inverter," in *IET Power Electronics*, vol. 9, no. 8, pp.1590–1599, 2016.

[19] X. F. Hu, P. H. Ma, B. B. Gao, *et al*, "An integrated step up inverter without transformer and leakage current for grid-connected photovoltaic system," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9814–9827, Oct. 2019.

[20] Z. Yu, X. Hu, M. Zhang, L. Chen, and S. Jiang, "A transformerless boost inverter for stand-alone photovoltaic generation systems," *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Xi'an, China, 2019, pp. 570–575.

[21] C. Sun, J. Lin, and Z. N. Zhu, "Research on SPWM combined boost DC/AC converter," in *Electrotechnical Application*, No. 6, pp.10–12, 2001.

[22] L. G. Zhang and Z. Z. Liu, "Research and design of LC filter for SPWM inverter power supply," in *Design of Electronic Engineering*, vol. 22, no. 6, pp.172–174, 2014.

[23] D. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," in *IEEE Transcations Power Electronics*, vol. 18, no. 3, pp. 814–822, May 2003.

[24] V. Gautam, Ashok kumar, and P. Sensharma, "A novel single stage transformer less PV inverter," *2014 IEEE International Conference on Industrial Technology*, pp. 907–912, Feb. 2014.

[25] A. Abramovitz, B. Zhao, and K. M. Smedley, "High-gain single-stage boosting inverter for photovoltaic applications," in *IEEE Transcations on Power Electronics*, vol. 31, no. 5, pp. 3550–3558, May 2016.

[26] Y. Tang, Y. Bai, J. Kan, and F. Xu, "Improved dual boost inverter with half cycle modulation," in *IEEE Transcations on Power Electronics*, vol. 32, no. 10, pp. 7543–7552, Oct. 2017.

[27] X. Guo, N. Wang, J. Zhang, B. Wang, and M. Nguyen, "A novel transformerless current source inverter for leakage current reduction," in *IEEE Access*, vol. 7, pp. 50681–50690, 2019.

[28] H. Wang, W. Wu, S. Zhang, Y. He, H. S. Chung, and F. Blaabjerg, "A modified Aalborg inverter extracting maximum power from one PV array source," in *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 109–118, June 2019.

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