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Analysis and Design of High-Performance Asynchronous Sigma-Delta Modulators With a Binary Quantizer

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Abstract—Asynchronous sigma-delta modulators (ASDMs) are closed-loop nonlinear systems that transform the information in the amplitude of their input signal into time information in the output signal, without suffering from quantization noise such as in synchronous sigma-delta modulators. This is an important advantage with many interesting applications. In contrast with their synchronous counterparts, ASDMs have been underexposed. Both conceptually and analytically, they are quite complex. This paper investigates in detail the analysis, design and circuit-implementation aspects of ASDMs with a binary quantizer. In the ASDM, the amplitude-time transformation is done using an inherent self-oscillation denoted as a limit cycle. The oscillation frequency is addressed as the main design parameter that determines the spectral properties of the ASDMs and the quality of the amplitude-time transformation. Analytical and graphical derivations of the limit cycle frequency are treated. The impact of the filter order and the properties of the nonlinear element are elaborated on. Circuit implementations and the tradeoffs in the design are presented for a first- and a second-order ASDM that target the VDSL front-end specifications. Prototypes are implemented in a digital 0.18- μm 1.8-V CMOS technology. The measured SFDR is 75 dB in a frequency band of 8 MHz for the first-order ASDM, and 72 dB in a band of 12 MHz for the second-order ASDM. The dissipated power is 1.5 mW and 2.2 mW, respectively.

Index Terms—Asynchronous modulation, CMOS, describing function, sigma-delta.

I. INTRODUCTION

ASYNCHRONOUS sigma-delta modulators can be used to convert an analog continuous-time input signal into a continuous-time, discrete amplitude output signal. Through this conversion, the information in the amplitude of the input signal is coded in the pulse widths of the output signal. ASDMs have the same structure as their synchronized counterparts: the well-known sigma-delta modulators (SDMs). However, their description is far more complex than that of SDMs, as the simplification of a linear loop that is excited by an extra, uncorrelated

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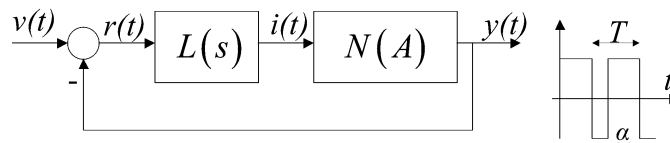


Fig. 1. Block diagram of ASDM and the waveform at the output with period T and duty cycle α/T .

noise source, is not valid here. ASDMs can be described as a closed-loop system (Fig. 1) built with a linear filtering block $L(s)$ and a nonlinear element.

The transfer function of the nonlinear element is denoted as $N(A)$, where A is the amplitude of the input signal for this nonlinear element. In the general case, $N(A)$ can represent any type of nonlinear element. However, of particular interest are nonlinear elements with binary output (single-bit quantizers, nonlinear amplifiers, and binary switches) and especially the quantizer with hysteresis. Due to the hysteresis, the nonlinear function performed by such a quantizer depends on both the sign and the phase of the input signal and introduces an additional degree of freedom in the system design. Furthermore, most asynchronous quantizers employ regenerative circuitry (with a positive feedback) to achieve high speed. Such an implementation may have a hysteresis that can be taken into account in the determination of the system behavior.

ASDMs transform amplitude into time information without an external sampling (clock) signal. That is their most attractive property, because no quantization noise is introduced into the system. In comparison, an external clock is required for the operation of the SDMs, and the input of the quantizer at each clock moment has to be represented by a certain discrete value, thus introducing quantization noise. The output spectra of the two types of modulators are compared in Fig. 2. In the ASDMs the signal's transitions in time depend only on the properties of the input signal of the quantizer: the moment of transition coincides exactly with the moment of crossing the threshold. This internal timing mechanism is described by the unforced periodic oscillations denoted as limit cycles. The accuracy of the amplitude-time transformation depends on the properties of this limit cycle and can be very high, as described later in the paper.

Due to its fully analog nature, the ASDM has a specific application area where pure analog processing is required. Applications are reported in the context of ADSL/VDSL line drivers [3], line driver for optical cables [4], and in UMTS transmitter

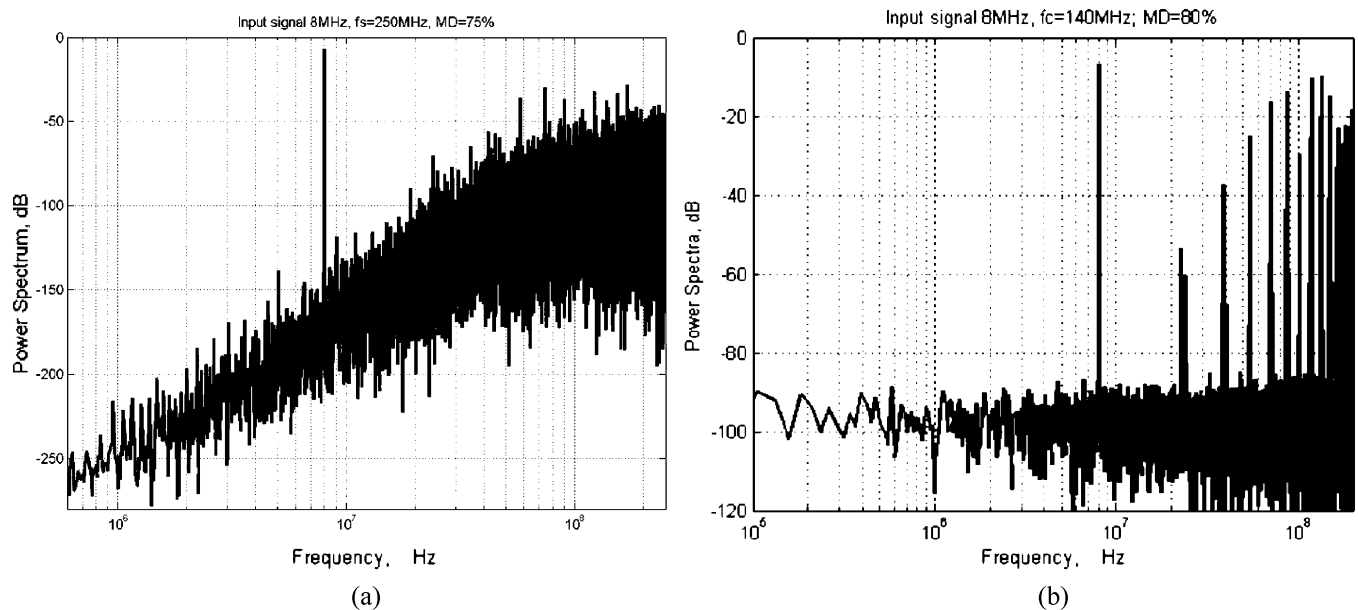


Fig. 2. Comparison of the output power spectrum of (a) standard second-order SDM and (b) second-order ASDM.

architectures [5]. In [2], its combination with an external sampler for the realization of analog to digital conversion is described. The ASDM can be used as a simple but high-precision and low-power alternative for the standard sampled sigma-delta converters for those and other applications that do not functionally require digitalization in time. Due to the equivalence of the low-frequency spectrum of the modulated square wave and the spectrum of the modulating input signal, the reconstruction of the input signal can be achieved with simple low-pass filtering.

The aim of this paper is to investigate the implementation of first- and second-order asynchronous sigma-delta modulators, starting from the theoretical fundamentals. The chosen technology is that of a standard 0.18- μm 1.8-V CMOS process. First, without specifying a particular application, the general performance limitations and the boundaries of operation are established. Second, the VDSL front-end specifications for a spurious free dynamic range (SFDR) of 75 dB in a bandwidth of 12 MHz are chosen as the target circuit performance for the implemented ICs.

The paper is structured as follows. Section II illustrates the application of analytical and graphical methods for the analysis of ASDM. In Section III, the transistor level design is discussed. In Section IV, the measurement results from the implementation of first- and second-order ASDMs are given and analyzed, and finally, in Section V, conclusions are drawn.

II. ANALYSIS OF ASDM

The spectral properties of the ASDM can be determined via an analysis of the existence and the frequency of limit cycle oscillations. These properties have to be evaluated with respect to system parameters like the filter order and the type of nonlinear element.

For a feedback system, the existence of a limit cycle oscillation is determined from the gain-phase relation in the closed loop. The Barkhausen criterion predicts that a closed-loop system is prone to self-oscillation at the frequency at which 360 degrees of

phase shift occurs and the loop gain is 1. When the system employs a nonlinear element, the self-oscillation conditions should be reconsidered. For example, the presence of hysteresis in the binary quantizer operation introduces a frequency-dependent phase shift into the loop. Applying the Barkhausen criterion for a closed-loop system with a negative feedback (which provides 180 degrees of phase shift), the self-oscillations may occur at the frequency for which the linear part and the nonlinear element together are providing another 180 degrees of phase shift. Intuitively, the presence of hysteresis enables limit cycle oscillations in first-order systems. On the other hand, for higher order systems, the hysteresis is not required for self-oscillation, but still often recommended, as will be explained further on. Its impact is taken into account in the following system analysis.

A. Establishment of the Limit Cycle Frequency Via Fourier Series Expansion

The limit cycle frequency for the system shown in Fig. 1 can be derived under the initial assumptions for a zero input signal $v(t) = 0$ and an existence of a square wave output signal $y(t)$ with a 50% duty cycle. Those initial conditions are dictated by the fact that the oscillations that we want to establish are unforced (independent from external driving signals) and the system is symmetric: the output levels and the hysteresis levels have equal offset from the point of symmetry (zero in the ideal case). The time waveforms for a first-order system are shown in Fig. 3. To facilitate the visualization, the system settings are chosen in such a way that $y(t)$ and $i(t)$ are of the same order of magnitude. In practice, the magnitude of $i(t)$ decreases with the increase of the limit cycle frequency and can be significantly lower. The limit cycle frequency can be derived in the following steps. First, the square wave signal $y(t)$ is expanded in a Fourier series:

$$y(t) = \frac{4}{\pi} \sum_{k=1,3,5,\dots}^{\infty} \frac{\sin k\omega_c t}{k} = \frac{4}{\pi} \sum_{k=1,3,5,\dots}^{\infty} \frac{1}{k} \text{Im}(e^{jk\omega_c t}) \quad (1)$$

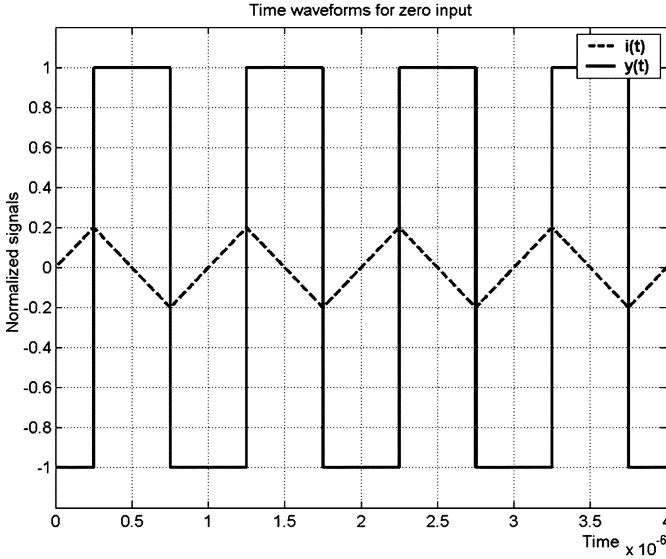


Fig. 3. Time domain waveform of the output signal $y(t)$ and the signal in front of the quantizer $i(t)$.

where the output levels of the quantizer are normalized to $+/-1$ and ω_c is the frequency of the square wave or the limit cycle frequency for zero input signal. The term center frequency is used to denote the limit cycle frequency for a zero input signal.

Second, the input signal $i(t)$ of the nonlinear element is expressed as a time-domain convolution of the filter impulse response and the residue signal $r(t) = v(t) - y(t)$. With $v(t) = 0$, the result is as follows:

$$i(t) = -\frac{4}{\pi} \sum_{k=1,3,5,\dots}^{\infty} \frac{1}{k} \text{Im} [L(jk\omega_c) e^{jk\omega_c t}] \quad (2)$$

where $L(j\omega)$ is the transfer function of the loop filter.

Third, we must take into account that the moments when $i(t)$ crosses the hysteresis values h , $-h$, correspond to the zero crossings of the square wave. That is described with the following relation:

$$\sum_{k=1,3,5,\dots}^{\infty} \frac{1}{k} \text{Im} [L(jk\omega_c)] = +/- \frac{\pi h}{4}. \quad (3)$$

Expression (3) gives a relation between the properties of the linear part of the loop and the quantizer when the system exhibits limit cycle oscillations. The exact frequency of the limit cycle can be determined for a particular filter implementation. As an example, (3) is applied for first- and second-order filters, which can be modeled respectively as follows:

$$L_1(j\omega) = \frac{\omega_p}{j\omega + \omega_p} \quad L_2(j\omega) = \frac{(j\omega + \omega_z)\omega_{p1}\omega_{p2}}{(j\omega + \omega_{p1})(j\omega + \omega_{p2})\omega_z} \quad (4)$$

The DC gain in (4) is normalized to 1 and for the second-order system two different poles and a zero are introduced. The above filter definitions are substituted in (3), allowing us to calculate the limit cycle frequency in the two cases as

$$\omega_{c1} = \frac{\omega_p \pi}{2h} \quad \omega_{c2} = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \frac{\pi}{2h}. \quad (5)$$

From (5) it follows that the limit cycle frequency can be controlled via the hysteresis value and the frequency characteristics

of the filters. The impact of a particular implementation is discussed in detail in the next section. However, beforehand, estimation can be made of the quality of the amplitude-to-time transformation. For that purpose, the behavior of the system is studied when DC or sinusoidal input signals are applied. Again, the behavior is studied via a Fourier series expansion of the output square wave. For DC input with magnitude V normalized to 1 such that $|V| \leq 1$, the mean value of the output square wave is V . This time, the residue signal is a result of the subtraction of two nonzero components: $r(t) = V - y(t)$. Then the Fourier expansion of the square wave is given as

$$y(t) = \frac{2}{\pi} \frac{\pi - \alpha}{2} - \frac{4}{\pi} \sum_{k=1,2,3,\dots}^{\infty} \frac{\text{sinc}k(\pi - \alpha) \text{sinc}k\omega t}{k} \quad (6)$$

where α is the pulse width, $T = 2\pi/\omega$ is the output period, and ω is the instantaneous frequency of the square wave. The term instantaneous frequency is used for the frequency of the limit cycle for an arbitrary instantaneous magnitude V of the input signal. The duty cycle and the frequency are modulated according to the following:

$$\frac{\alpha}{T} = \frac{V+1}{2} \quad \frac{\omega}{\omega_c} = 1 - V^2. \quad (7)$$

The term modulation depth (MD) is defined as the ratio between the amplitude of the input signal and the maximum dynamic range or the full scale (FS) input signal that can be applied to the ASDM. For larger input signals the modulator is overloaded. The time domain waveforms of the output signal $y(t)$ for DC and sinusoidal input signals are shown in Fig. 4.

Of particular interest is the behavior of the system when a sinusoidal signal of the type $v(t) = v_m \cos \mu t$ is applied with $|v_m| \leq 1$. Once again, using the three evaluation steps, the spectral content around the fundamental component of the limit cycle frequency can be derived as [2]

$$y_1(t) = \frac{2}{\pi} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} J_m \left(v_m \frac{\pi}{2} \right) J_{2n} \left(\frac{\omega_c v_m^2}{4\mu} \right) \times \cos m \frac{\pi}{2} \cos (\omega_c t + (2n+m)\mu t) \quad (8)$$

where, in general, $J_p(x)$ denotes a Bessel function of the first kind and order p . From (8), it can be concluded that the frequency position of the Bessel components is a function of the amplitude and the frequency of the input signal and the order of the linear element. An example is shown in Fig. 5 of the output spectrum for the first-order implementation, when a small modulating signal is applied. The input signal with a frequency of 1 MHz and amplitude that corresponds to 10% modulation depth is visible in the left side of the plot.

For zero input signal, the output frequency spectrum contains a single tone at the center frequency of the limit cycle, at 140 MHz. When the sinusoidal input signal is applied, the output is modulated according to (8) and the Bessel components appear around the limit cycle frequency. The Bessel sums are infinite. However, for low modulation depths only the first few terms of (8) that originate close to the limit cycle frequency are distinguishable above the noise floor. Expression (8) can be used for evaluation of the limit cycle frequency that is required

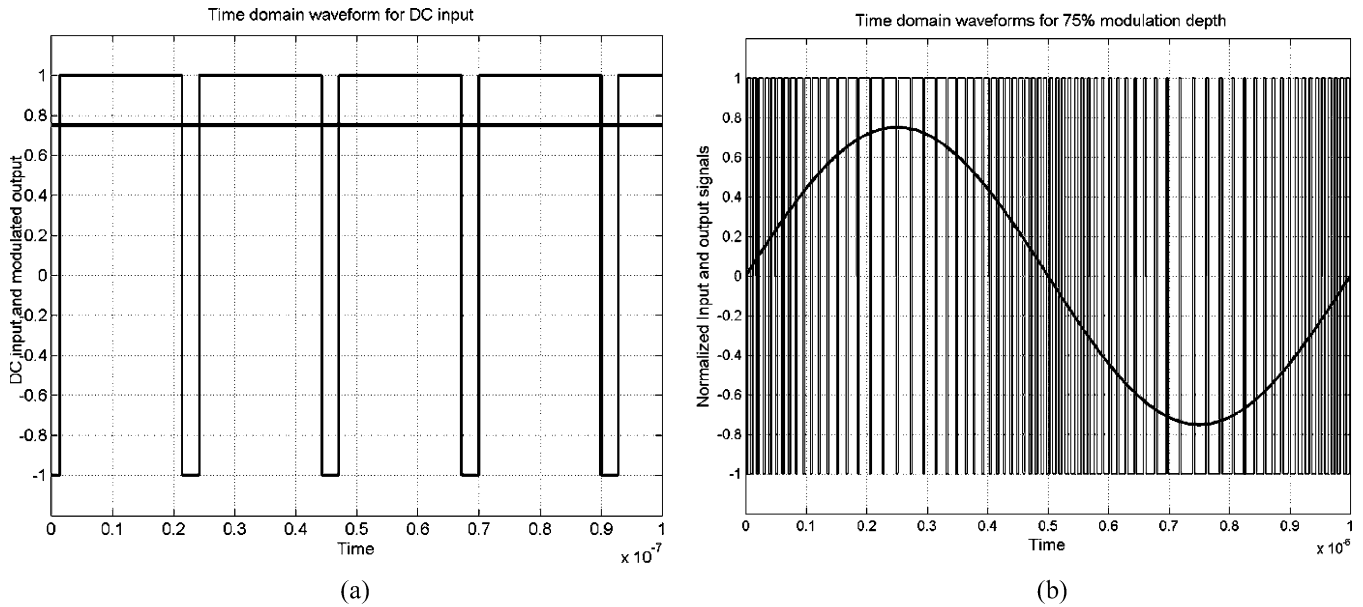


Fig. 4. Time domain waveforms of the output signal $y(t)$ for (a) DC input signal and (b) sinusoidal input signal.

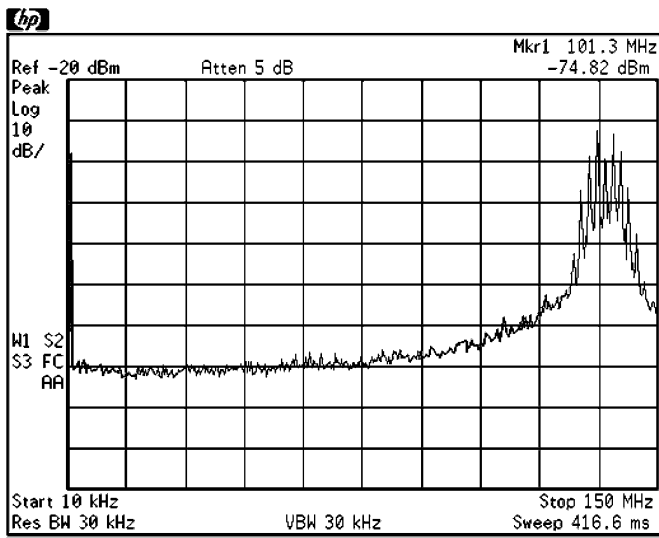


Fig. 5. Measured output spectrum of the first-order ASDM for a 1-MHz test signal and a modulation depth of 10%.

to avoid appearance of Bessel components in the chosen frequency baseband. In Fig. 6, the achievable SFDR in a frequency band that incorporates the third harmonic of the input signal is evaluated for the first- and second-order ASDMs. On the horizontal axis the ratio between the limit cycle center frequency and the input signal frequency (μ) is plotted. This ratio can be perceived as analogous to the oversampling ratio in SDM and shows the minimal center frequency that is required for a certain accuracy of the amplitude-time transformation. For a bandwidth of 8 MHz and a SFDR of 75 dB, it predicts that the center frequency has to be at least 140 MHz for a first-order system.

B. Graphical Evaluation of the System Properties

The solution for the existence and the frequency of the limit cycle oscillation in a nonlinear feedback system can be formalized [1] with the help of the describing function (DF) rep-

resentation of the nonlinear element. The goal of the DF approach is to build a linear approximation of the nonlinear element according to a certain linearization rule and with respect to a preliminary defined input signal, for example bias, sinusoid or Gaussian signal. The quasi-linear approximating functions, which describe the transfer characteristics of the nonlinear element, are named describing functions. The linearization rule implements a criterion for the evaluation of the approximation. The most common criterion used in practice is the minimum mean square difference between the approximated output and the actual output of the nonlinear element. The power of the methods is in the ease with which higher order systems and complex nonlinear functions can be analyzed. However, the accuracy of the solution depends on the linear portion of the closed-loop and on the particular nonlinear function. The results need an experimental verification for each particular case.

The limit cycle oscillations are determined by the equation

$$1 + N(A)L(j\omega) = 0 \quad (9)$$

where $N(A)$ represents the describing function of the nonlinear element. This equation can be interpreted in analogy to the linear case prediction of oscillations given by the Barkhausen criterion. The DF of a binary quantizer with hysteresis is given by

$$N(A, \varphi) = \frac{4}{\pi A} \sqrt{1 - (h/A)^2} - j \frac{4h}{\pi A^2} = \frac{4}{\pi A} e^{-j \sin^{-1}(h/A)} \quad (10)$$

where φ accounts for the argument of (10) and shows that the nonlinear element contributes to phase shift. From (10), it follows that the contribution of the quantizer to the phase delay that is introduced in the loop depends on the ratio between the hysteresis level and the amplitude of the input signal. The DF is normally defined for a single frequency component in front of the nonlinear element. Here, the application of a DF is justified because the frequency of the input signal is significantly lower than the frequency of the limit cycle oscillations. In such a case, the response of the nonlinear element can be approximated as a

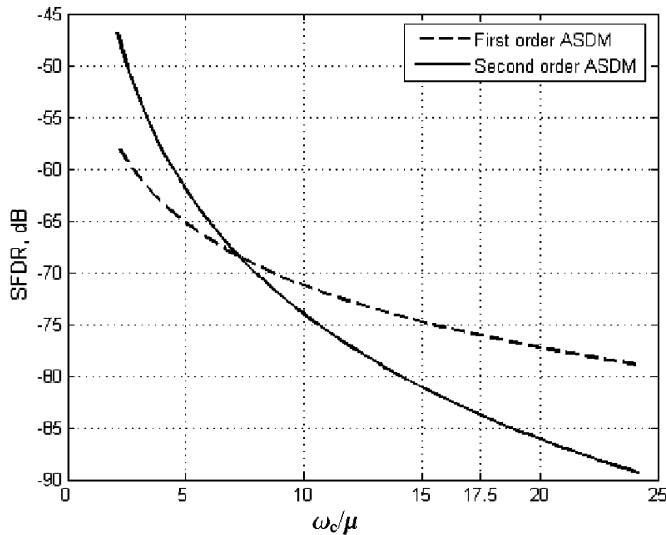


Fig. 6. Estimation for the achievable SFDR for first- and second-order ASDM at 80% MD in a frequency band 3μ . The plot is normalized with respect to the center frequency of the limit cycle.

response to a single frequency component. Equation (9) can be solved graphically for the chosen nonlinear element and filter order. Here, a magnitude-phase plot is used, parameterized with respect to the frequency for the linear element, and with respect to the amplitude of the signal $i(t)$ for $N(A, \varphi)$. The plot for a first-order system is shown in Fig. 7. The limit cycle magnitude and frequency can be determined from the crossing point of the $-1/N(A, \varphi)$ and $L(j\omega)$ curves, as shown in the figure. Due to the hysteresis, the function $-1/N(A, \varphi)$ is complex and thus introduces a phase rotation. In contrast, the DF of a simple binary quantizer is a real function of the amplitude A : $N(A) = 4/\pi A$ and is plotted as a straight line in the magnitude-phase plane.

From Fig. 7, the degrees of freedom for the system parameterization can be established. For example, an increase of the hysteresis value leads to a shift of the curve $-1/N(A, \varphi)$ upwards and results in a decrease in the limit cycle frequency and an increase in the amplitude A of the signal in front of the nonlinear element.

A comparison for the first-order system between the exact solution, described in the previous section, and the graphical evaluation, based on the describing function, showed a negligible deviation of the DF result from the actual values of the limit cycle frequency and amplitude. The DF gives an even better estimation of the system properties when higher order filtering is performed in front of the nonlinear element. The graphical evaluation for the second-order system is shown in Fig. 8. The second-order filter characteristic reaches the 180 degrees phase shift with a very small tangent. In a practical implementation that would mean that if there was no hysteresis in the quantizer, the limit cycle frequency would be determined by the parasitic time delays in the loop. Much better control over the limit cycle frequency can be achieved by introducing a hysteresis.

It should be pointed out that no generalization could be drawn for the accuracy of the application of the DF for other types of nonlinear elements and system configurations.

The main advantage of the DF approach can be seen in the investigation of higher order systems, where more than one limit

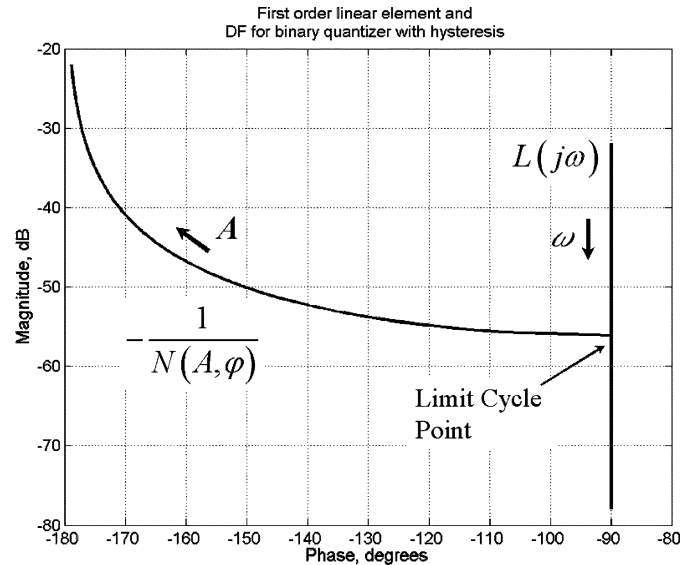


Fig. 7. Graphical determination of limit cycles for a first-order ASDM with a binary quantizer with hysteresis.

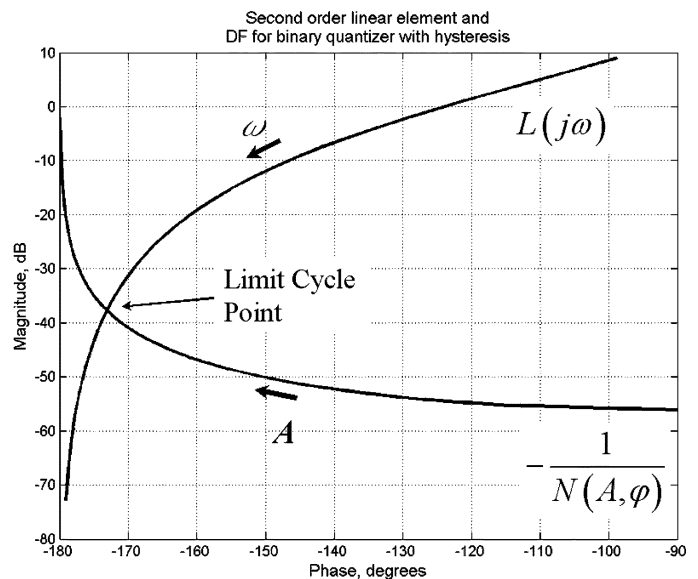


Fig. 8. Graphical determination of limit cycles for a second-order ASDM with binary quantizer with hysteresis.

cycle is possible, i.e., more than one crossing point exists in the magnitude-phase plot. In such a case, the analytical solution becomes laborious without giving further insight into the system properties. The DF approach can easily be extended for the study of multi-bit quantizers and other nonlinear closed-loop systems.

III. TRANSISTOR LEVEL DESIGN

A sufficiently high limit cycle frequency is the main design criterion for the ASDM, because in order to avoid distortion, a significant distance between the baseband of interest and ω_c is needed. For the implemented systems, a ω_c of at least 120 MHz was desired. At system level, ω_c is controlled via the loop filter properties, the gain in the loop, and the hysteresis levels of the quantizer.

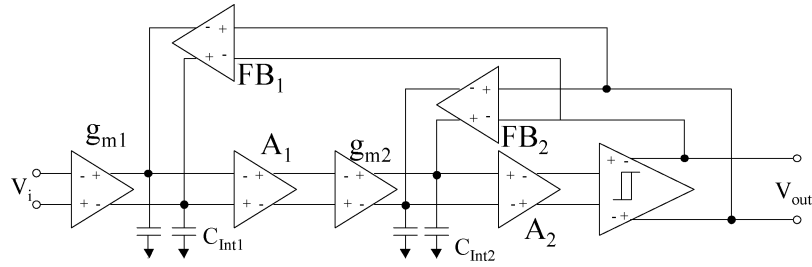
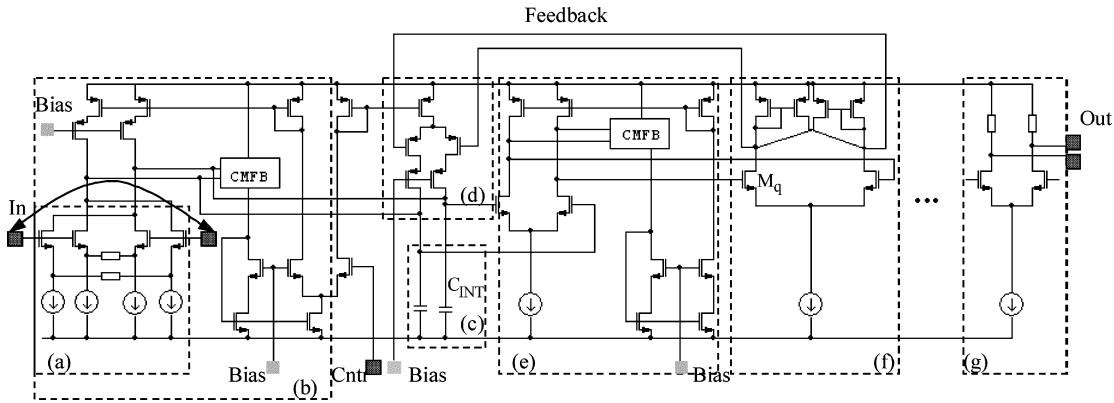


Fig. 9. Block diagram of the second-order ASDM.


 Fig. 10. Circuit schematic of the first-order ASDM. (a) Input $V-I$ converter. (b) Whole G_m stage. (c) Integrating capacitances. (d) Feedback. (e) Broadband amplifier. (f) Quantizer with hysteresis. (g) Output buffer with $50\text{-}\Omega$ driving capability.

However, every transistor implementation introduces additional limitations such as finite bandwidth, nonlinearity and noise, and cost factors like the chip area and power consumption. Next, these factors are discussed for each circuit building block and their impact on the system behavior is evaluated. A differential implementation [6] of a first- and a second-order system can be described with the block diagram shown in Fig. 9. The second-order block diagram reduces to a first-order one, when the blocks with index 2 are omitted. The stages g_{m1} and g_{m2} are transconductors (voltage-to-current converters) that, together with the capacitances C_{int1} and C_{int2} , implement continuous-time integrators. The blocks FB_1 and FB_2 represent the feedback transfer. In practice they are implemented as switched-current sources [Fig. 10(d)]. The switches are controlled by the binary output signal. The blocks A_1 and A_2 are linear gain stages. Their purpose is to decrease the effective hysteresis value and reduce the design requirements for the quantizer with respect to speed and power consumption. In practice, this additional gain in the feed-forward path can be used as an instrument for the realization of a higher ω_c . Expressions (5) can be rewritten for the limit cycle frequency ω_{c1} of the first-order and ω_{c2} of the second-order transistor implementations of the ASDM:

$$\omega_{c1} = \frac{A_1 g_{m1} \pi}{2h C_{Int1}} FB_1 \quad \omega_{c2} = \frac{A_1 A_2 G_{m1} G_{m2} \pi}{2h C_{Int1} C_{Int2}} FB_1 FB_2. \quad (11)$$

Fig. 10 shows the implemented, fully differential circuit schematic of the first-order ASDM. The common-mode feedback (CMFB) circuits and the biasing circuits are omitted for simplicity. The output buffers [only the last stage is shown in Fig. 10(g)] are out of the loop and are only needed to provide

the high driving capability required by the measurement set-up. They were implemented as a chain of matched blocks with separate power supply and $50\text{-}\Omega$ driving capability.

A. Loop Filter (Integrator) Design

A continuous-time G_m - C integrator was chosen for the loop filter implementation due to its speed advantage and low power consumption [7]. The most significant problem in a G_m - C filter implementation is the limited input dynamic range with high linearity. This range is fully determined by the input voltage-to-current ($V-I$) converter, g_{m1} in Fig. 9. For the linearization of the transconductor characteristics, a novel circuit solution [8] based on the combination of local resistive feedback and cross-coupling is used [Fig. 10(a)]. This circuit achieves significant simultaneous suppression of the third- and fifth-order harmonic distortion components in the transconductor characteristics. Thus, very high linearity can be obtained with low power consumption. The input transconductor is the first building block in the modulator chain and also determines the noise performance. The transistor sizes in this stage are significantly up-scaled, so that the flicker noise energy in the baseband is decreased below the noise specifications. The increased transistor sizes also provide for a better matching and consequently for a better differentiability and robustness of the linearization mechanism. In the first-order ASDM, g_{m1} occupies half of the chip area and consumes almost half of the total current.

The second transconductor g_{m2} is inside the closed ASDM loop. There the amplitude information from the input signal is already mainly positioned in the zero crossings (in time) via the

limit cycle oscillations. Thus, inside the loop, the ASDM operation is much less sensitive to amplitude distortion. That leads to a significant decrease in the linearity and noise specifications for the g_{m2} and the gain stages. These are downscaled and altogether consume less than 20% of the total power used in the second-order implementation. However, care is taken that no clipping can occur at any point inside the loop. Clipping would introduce an extra delay in the loop and thus decrease the limit cycle frequency. The gain stages are used to increase ω_c . A requirement for their design is a gain-bandwidth product that exceeds the ASDM bandwidth of operation. The parasitic poles in the gain stages should not change the order of the system. For this design, amplifiers with gain of 15 dB in a band of 300 MHz were used.

The FB_1 and FB_2 blocks have a twofold operation. First, they transfer the output voltage into current that is integrated in C_{int} and second, the feedback signal is scaled in such a way that the maximum dynamic range of the loop corresponds to the maximal linear dynamic range of the input transconductance g_{m1} . The loop has peak performance for about 80% modulation depth. For signals with higher amplitude the loop enters an overload region and the Bessel components rapidly enter the baseband.

B. Asynchronous Quantizer-Comparator With Hysteresis

The quantizer was implemented via a cascade of source-coupled differential pairs with positive feedback [only the first from two identical blocks is shown on Fig. 10(f)]. The static hysteresis value V_H is given by the following equation:

$$V_H = 2 \sqrt{\frac{I_{bias}}{\mu C_{ox} W_q} \frac{\sqrt{\delta} - 1}{\sqrt{1 + \delta}}} \frac{1}{L_q} \quad (12)$$

where the feedback coefficient $\delta = (W/L)_{cc}/(W/L)_{dc}$ is the ratio between the cross-coupled and the diode-connected transistors, I_{bias} is the tail biasing current and $(W/L)q$ is the ratio between the width and the length of the input pair. For $\delta > 1$, the load acts as a negative resistance and hysteresis is introduced [9]. The tradeoff to be solved in this stage is between the power consumption and the switching speed on the one hand, and the minimal V_H and δ on the other. The limit cycle frequency is inversely dependent on the hysteresis (11) and increases with a decrease in the hysteresis value. To achieve higher limit cycle frequencies the hysteresis has to be minimized. The minimal value of V_H that can be implemented is evaluated with respect to the environmental and process corners, so that the regenerative operation of the quantizer is always assured.

C. Performance Limitations and Tradeoffs

The performance of the ASDM is defined as the maximum frequency baseband that can be processed within the linearity specification. On the one hand the performance is determined by the maximum limit cycle frequency that can be achieved. For a design that is robust with respect to process spread and temperature variations, the limit cycle frequency can be pushed higher with higher gain in the feed-forward path. That would result in an increase in the required power consumption. On the other

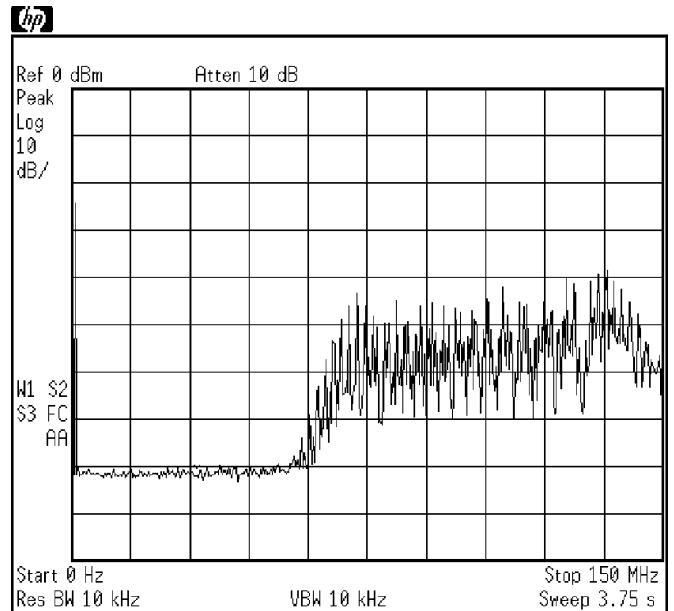


Fig. 11. Measured output spectrum of the first-order ASDM for a 1-MHz test signal and a modulation depth of 50%.

hand, the quality of the Gm - C filter implementation determines the quality of the conversion in the baseband, with respect to SFDR and SNR. Again, the performance can be improved with higher power consumption. The implemented circuit solution tries to resolve these tradeoffs for a bandwidth of 12 MHz dictated by the VDSL front-end specifications.

IV. MEASUREMENT RESULTS

The performance of the manufactured circuits was evaluated via measurements of the spectra of the output signal. Several aspects of the operation of the first-order ($ASDM_1$) and the first-order ($ASDM_2$) modulators are demonstrated and compared. The $ASDM_1$ was designed to operate with a limit cycle frequency of 140 MHz. The spurious tones are below the noise in the frequency band of 0–8 MHz. In Fig. 11, the output spectrum of the first-order ASDM is shown for a modulation depth of approximately 50%.

The Bessel components around the fundamental component of the limit cycle frequency and its multiples occupy a significant part of the output spectrum. However, the spectral purity in the baseband is still within the required accuracy. The spectral purity of the baseband is preserved up to an MD of around 80%. For higher MD, the loop is overloaded and the Bessel components enter the baseband. The loop is dimensioned in such a way that the overload conditions with respect to the input amplitude occur simultaneously with the overload of the first transconductor. The main difference in the performance of $ASDM_1$ and $ASDM_2$ can be seen in the larger frequency band that can be converted with the predefined quality by the second-order loop. The output of both modulators is evaluated after ideal low-pass filtering at 8 and 12 MHz, respectively. The achieved SFDR is plotted versus the frequency of the input signal in Fig. 12. The SFDR with input amplitude at 80% MD is measured in the baseband of each modulator for different frequencies of the input signal. Three regions of operation with respect to the frequency

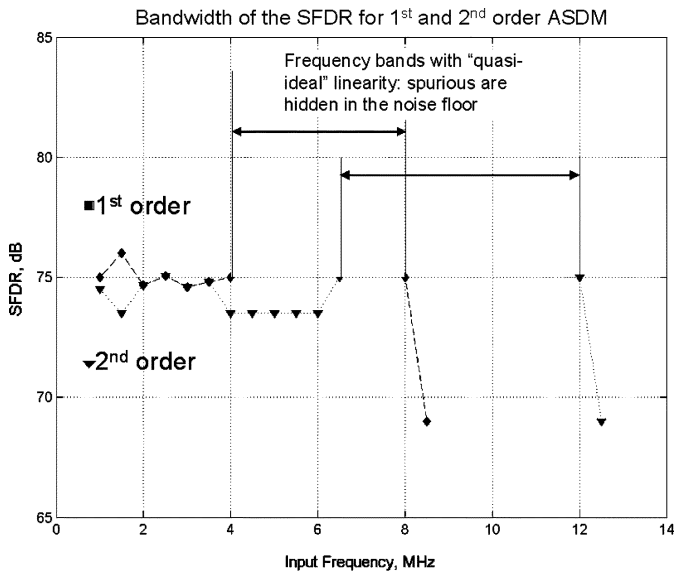


Fig. 12. Measured SFDR with input amplitude at 80% MD in the baseband of each modulator for different frequencies of the input signal.

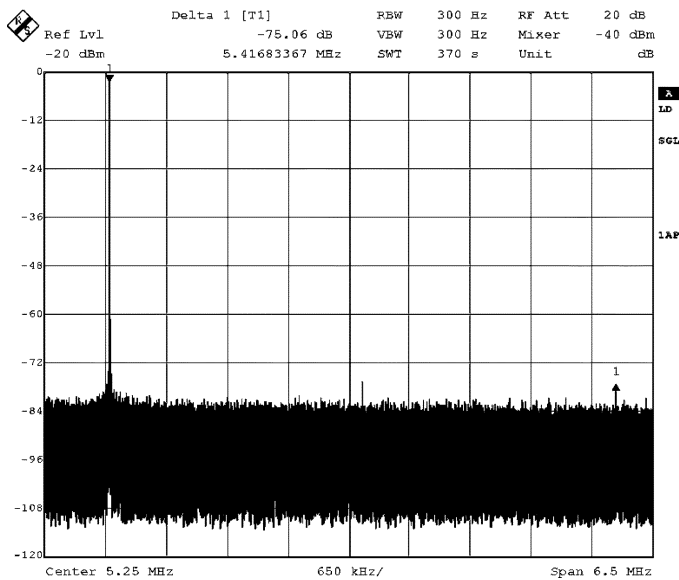


Fig. 13. SFDR, First-order ASDM measured at 80% modulation depth, for a worst case input frequency of 2.7 MHz.

of the input signal can be distinguished. The first one is up to half the baseband (4 and 6 MHz, respectively). For this region, the second- and third-order harmonic distortion components of the input signal fall within the evaluated band. As the input frequency is still low with respect to that of the limit cycle frequency, the performance is mostly determined by the linearity of the first transconductor. In the second region, the loop displays a “quasi-ideal” performance, as there are no Bessel components in the baseband that can be distinguished above the noise floor.

The dynamic range of the measurement set-up was 100 dB and all Bessel components below that value are undetectable. The third region is at the edge of the modulator’s baseband. The Bessel components start to enter the band and the performance rapidly decreases.



Fig. 14. SFDR with respect to the amplitude of the input signal.

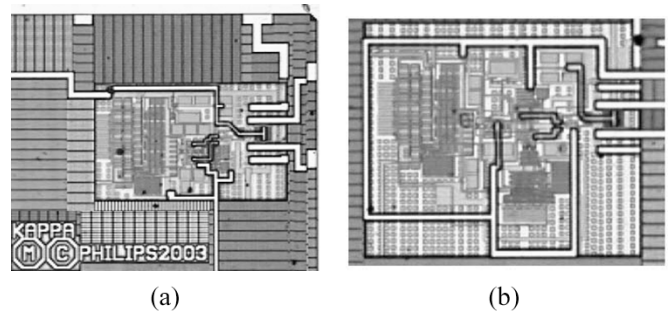


Fig. 15. Chip photographs. (a) First-order ASDM. (b) Second-order ASDM.

TABLE I
SUMMARY OF MEASURED PERFORMANCE

0.18 μ m, 1.8V CMOS	First Order ASDM	Second Order ASDM
Area with (out) buffer	0.040 (0.026) mm ²	0.054 (0.04) mm ²
Centre frequency	140MHz	120MHz
SFDR [0-8/12MHz]	75dB	72dB
SNR [1k-8MHz]	70dB	70dB
Current Consumption	800 μ A	1200 μ A

The measured SFDR for maximum input signal is shown in Fig. 13. For this measurement, a differential input signal of 400 mVpp was used that corresponds to approximately 80% modulation depth. The odd-order harmonic distortion is due to the $V-I$ converter of which the performance starts to degrade for those amplitudes. The odd harmonics that were measured correspond to the simulated levels of -75 dB. However, in the SFDR an even-order component with the same magnitude is visible. It is due to the external transformer used for single ended to differential conversion at the input. Fig. 14 shows the measured dynamic range with respect to the amplitude of the input signal.

The characteristic is linear for both modulators up to amplitudes corresponding to 80% MD. Fig. 15 shows chip photographs of the implemented ASDMs. The measured performance is summarized in Table I.

V. CONCLUSION

Analytical and graphical methods were used for the analysis of limit cycle oscillations in ASDM. Rules were established for the transistor design and the performance limiting factors. A first- and a second-order ASDM were implemented in a standard, digital 0.18- μm CMOS process. The modulators achieve a SFDR of 75 and 72 dB in a bandwidth of 8 and 12 MHz, respectively. Both designs use a quantizer with hysteresis to achieve limit cycle center frequencies of 140 and 120 MHz, respectively. The price of the improved performance for the second-order modulator is a minor increase in the chip area and the circuit complexity. When the application requires a moderate frequency baseband (up to 10 MHz), a high limit cycle frequency is easily implemented, as the performance of both first- and second-order modulators is limited by the linearity of the input $V-I$ stage. In such a case, the use of a first-order modulator is recommended due to the ease of implementation.

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